SIEMENS

IC für Industrie- und Autoelektronik

Industrial and Automotive ICs

Data Book 1993/94

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▼ New type

■ Not for new design

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▼ New type

■ Not for new design

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▼ New type
■ Not for new design
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▼ New type
■ Not for new design
= SMD

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▼ New type
■ Not for new design
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1. Elektrische Prüfungen und Anwendungsschaltung

- Prüffassungen bzw. integrierte Schaltungen müssen beim Stecken oder Ziehen vonEinzelbauelementen oder bestückten Leiterplatten spannungsfrei sein, wenn in den entsprechenden Werksunterlagen nichts anderes angegeben ist. Es ist sicherzustellen, daß die Prüfgeräte und Stromversorgungen keine Spannungsspitzen erzeugen, weder bei betriebsmäßigem Ein- und Ausschalten noch beim Ausfall der Netzsicherung oder beim Ansprechen anderer Sicherungen.
- Bei der Stromversorgung bipolarer integrierter Schaltungen ist immer zuerst die negative Spannung ($-U_S$ bzw. Masse) anzuschließen. Eine Unterbrechung dieses Potentials im Betrieb ist in der Regel nicht zulässig.
- Signalspannungen dürfen an Eingängen der integrierten Schaltungen erst mit oder besser nach den Einschalten der Versorgungsspannung angelegt werden. Sie müssen mit oder möglichst vor dem Abschalten der Versorgungsspannung abgeschaltet werden.
- Stomversorgungen von integrierten Schaltungen sind möglichst nahe an den Versorgungsanschlüssen des ICs abzublocken. Bei bipolaren integrierten Schaltungen ist die Verwendung eines induktivitätsarmen Elektrolytkondensators, zumindest jedoch die Parallelschaltung eines Keramikkondensators von z. B. 100 nF bis 470 nF empfehlenswert.

  Bei integrierten Schaltungen mit hohen Ausgangsströmen muß der nötige Wert des Elektrolytkondensators der Prüf- bzw. Anwendungs-schaltung angepaßt werden. Zu berücksichtigen sind Einschwingverhalten und dynamischer Ausgangswiderstand der Stromversorgungen, Leitungsinduktivitäten im Versorgungs- und Lastkreis und insbesondere induktive Lasten oder Motoren. Beim Abschalten von Leistungsinduktivitäten oder induktiver Lasten muß die gespeicherte Energie, wenn nicht anders angegeben, extern aufgenommen werden (z. B. durch einen Elektrolytkondensator, Dioden, Z-Dioden oder die Stromversorgung). Dabei ist auch ein Abschalten der Versorgungsspannung vor dem Zeitpunkt der Lastab-schaltung zu beachten.
- Integrierte Schaltungen mit Tiefpaßcharakter der Ausgangsstufen (z. B. PNP-Treiber oder PNP/NPN-Endstufen) benötigen in der Regel eine zusätzliche externe Kompensation am Ausgang. Dies gilt insbesondere bei komplexen Lasten. Bei NF-Leistungsverstärkern wird der Ausgang mit dem Boucherot-Glied kompensiert. Bei Brückenschaltungen genügt im Einzelfall die Überbrückung der Last mit einer Kapazität. Je nach Anwendung ist aber auch hier je ein Kondensator von jedem Ausgang gegen Masse zu empfehlen.
- Die Hinweise in den jeweiligen Datenblättern sind zu beachten.

2. Beschreibung der Datenangaben

Grenzdaten

Die Grenzdaten sind absolute Grenzwerte, bei deren Überschreitung auch nur eines Wertes die integrierte Schaltung zerstört werden kann.

Kenndaten

Die Kenndaten umfassen den Streubereich der Werte, die im angegebenen Betriebsbereich von der integrierten Schaltung eingehalten werden.

Unter den typischen Kenndaten werden Mittelwerte angegeben, die fertigungsmäßig erwartet werden. Wenn nicht anders vermerkt, gelten die typischen Kenndaten bei T_A = 25 °C und angegebener Speisespannung.

Funktionsdaten

Im Funktionsbereich werden die in der Schaltungsbeschreibung angegebenen Funktionen erfüllt.

3. Qualität

Qualitätssicherungssystem

Der hohe Qualttätsstandard der integrierten Schaltungen von Siemens ist das Ergebnis eines sorgfältigen Herstellungsprozesses, der in jeder Phase systematisch überwacht wird. Dazu dient ein Qualitätssicherungssystem, das in der Themenschrift "Qualitätssicherung Integrierter Schaltungen" ausführlich beschrieben ist.

1. Electrical Tests and Application Circuit

- The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
- When supplying bipolar integrated circuits with current, the negative voltage (— V_S or GND) has first to be connected. In general, an interruption of this potential during operations is not permissible.
- Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
- Power supplies of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled ceramic capacitor of 100 nF to 470 nF for example.
  Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or applicition circuit. Transient behaviour and dynamic output resistance of the power supplies, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered. When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e. g. by an electrolytic capacitor, diodes, Z-diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.
- ICs with low-pass characteristic of the output stages (e. g. PNP drivers or PNP/NPN end stages), normally need an additional external compensation at the output. This applies particulary to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.
- Observe any notes and instructions in the respective data sheets.

2. Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply $T_A = 25\ ^\circ C$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

3. Quality Assurance System

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure 'Siemens Quality Assurance – Integrated Circuits'

4. Summary of Terms and Symbols in Alphabetical Order

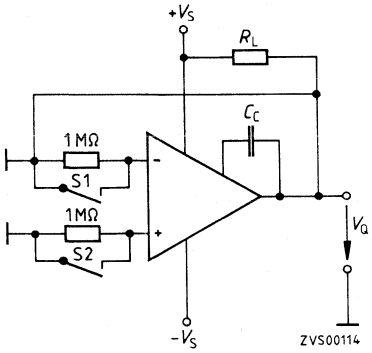
A, B	Indices for limit value
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwith
C	Capacitance
C_i, C_I	Input capacitance
C_{CLK}, $C\varnothing$	Clock capacitor
CLK	Clock
DC	Direct current
D	Differential
f	frequency
Δf	Frequency deviation
FM	Frequency modulation
f_i, f_I	Input frequency
f_q, f_Q	Output frequency
G	Gain
G	giga (10^9)
GND	Ground
Hy	Hysteresis
Hz	Cycles per second (Hertz)
I	Input
I,	Current
I_S	Current consumption
IF	Intermediate frequency
k	kilo (10^3)
K	kelvin
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Modulation factor
MW	Medium wave
N, n	Noise
o	Offset
OSC	Oscillator
P_I P_V	Power dissipation
P_{tot}	Max. perm. power dissipation
pp	Peak-to-peak
Q	Output
Q, Q_B	Q-factor
R	Resistance
$R_{th\ JC}$	Thermal resistance (junction-case)
$R_{th\ SC}$	Thermal resistance (system-case)
$R_{th\ SA}$	Thermal resistance (system-air)
RF	Radio frequency
$\frac{S+N}{N}$	Signal-to-noise ratio
T	Cycle time
T	Temperature
TC	Temperature coefficient
t	Time
T_A	Ambient temperature in operation
T_{stg}	Storage temperature
T_j	Junction temperature
t_H	Hold time
t_I	Input pulse duration
t_n	Instant prior to clock pulse
t_{n+1}	Instant after clock pulse
t_P	Average pulse transit time
t_{pd}	Pulse delay time
t_{PHL}	HL pulse transit time
t_{PLH}	LH pulse transit time
t_{pI}	Input pulse duration
t_{pQ}	Output pulse duration
t_{pR}	reset pulse duration
t_{pS}	Set pulse duration
t_{pCLK}	Clock pulse duration
t_{pZ}	Count pulse duration
t_s	Set-up time
t_T	Signal transition time
t_t	Dead time
t_Q	Output pulse duration
t_{THL}	HL transition time
t_{TLH}	LH transition time
THD	Total harmonic distortion
V	Volt
V, $_v$	Voltage, general
V_{Hy}	Hysteresis voltage
V_i, V_I	Input voltage
V_q, V_Q	Output voltage
V_R	Reserve voltage
V_S	Supply voltage
W	Watt
Z	Impedance
Z	Zener

Selector Guide

Type	Package	Operating Range			Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25$ °C			Page
		Supply Voltage V_S V	Operating Temperature T_A °C	Output Current I_Q mA max.	Input Offset voltage V_{IO} mV min./max.	Input Current I_I µA typ.	Slew Rate SR V/µs typ.	
Single Operational Amplifiers with NPN Input and Open Collector Output								
TAA 762 A	P-DIP-6-1	± 1.5 to ± 18	– 55 to 125	70	± 4	0.3	18	
TAA 762 G	P-DSO-6	± 1.5 to ± 18	– 55 to 125	70	± 4	0.3	18	
TAA 765 A	P-DIP-6-1	± 1.5 to ± 18	– 25 to 85	70	± 5.5	0.5	18	
TAA 765 G	P-DSO-6	± 1.5 to ± 18	– 25 to 85	70	± 5.5	0.5	18	
Dual Operational Amplifiers with NPN Input and Open Collector Output								
TAA 2762 A	P-DIP-8	± 2 to ± 15	– 55 to 125	70	± 4	0.3	0.5	
TAA 2765 A	P-DIP-8	± 2 to ± 15	– 25 to 85	70	± 5.5	0.5	0.5	
Single Operational Amplifiers with PNP Input and Open Collector Output								
TAE 1453 A	P-DIP-6-1	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	20	
TAE 1453 G	P-DSO-6	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	20	
TAF 1453 A	P-DIP-6-1	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	20	
TAF 1453 G	P-DSO-6	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	20	
Dual Operational Amplifiers with PNP Input and Open Collector Output								
TAE 2453 A	P-DIP-8	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	1	
TAE 2453 G	P-DSO-8-1	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	1	
TAF 2453 A	P-DIP-8	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	1	
TAF 2453 G	P-DSO-8-1	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	1	
Quad Operational Amplifiers with PNP Input and Open Collector Output								
TAE 4453 A	P-DIP-14-1	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	1	
TAE 4453 G	P-DSO-14-1	± 2.0 to ± 18	– 25 to 85	100	± 5.5	0.04	1	
TAF 4453 A	P-DIP-14-1	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	1	
TAF 4453 G	P-DSO-14-1	± 2.0 to ± 18	– 55 to 125	100	± 4	0.04	1	

= SMD

Input Current, Input Offset Current

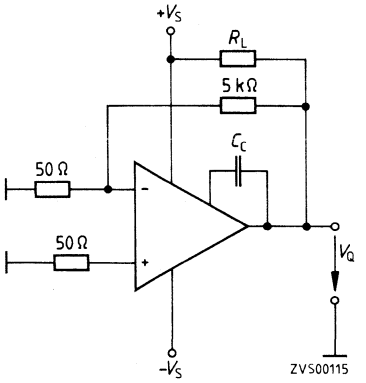


S1 open – S 2 closed: $I_{I-} = \frac{V_Q}{1\ M\Omega}$

S 2 open – S 1 closed: $I_{I+} = \frac{V_Q}{1\ M\Omega}$;

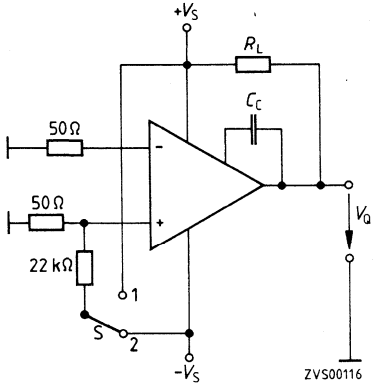
S 1 + S 2 open: I_{IO} approx. $\frac{V_Q}{1\ M\Omega}$

Input Offset Voltage



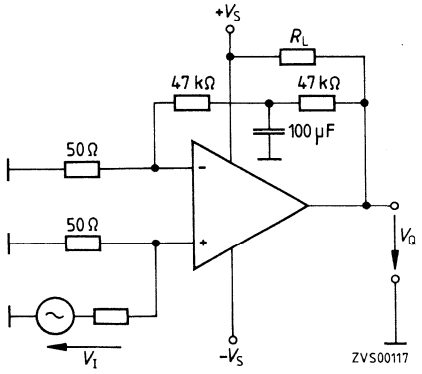
$-V_{IO} = V_{QO}/G_{VO}$; $G_{VO} = 100$; $-V_{IO} = \frac{V_{QO}}{100}$

Output Voltage, Control Range



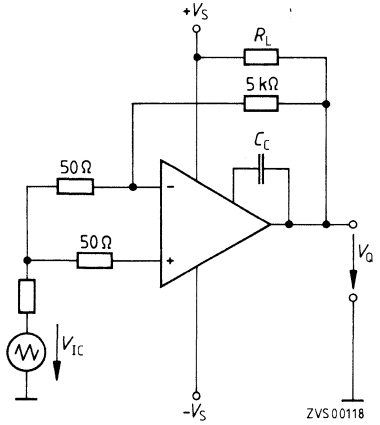
S in position 1: $V_Q = V_{QL}$;
S in position 2: $V_Q = V_{QO}$

Open-Loop Voltage Gain at $f = 1$ kHz

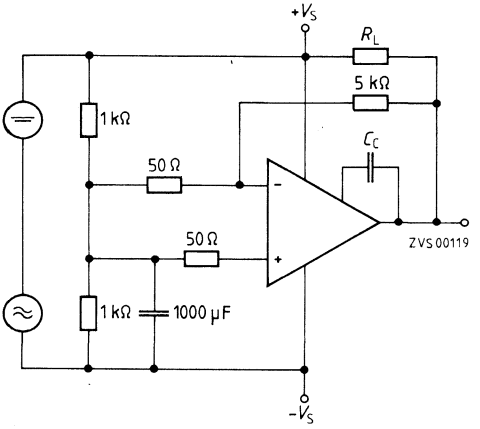


$G_{VO} = 20 \log \frac{V_Q}{V_I}$ [dB]

Common-Mode Rejection



Supply Voltage Rejection



$$G_{VC} = \frac{\Delta V_Q}{\Delta V_{IC}} \; ; \; k_{CMR} = 20 \log \frac{G_{V0}}{G_{VC}} \; [dB] \qquad \frac{\Delta V_{IO}}{\Delta V_S} = \frac{\Delta V_Q}{100 \times \Delta V_S}$$

Preventive measures are implemented in most operational amplifiers, to reduce the risk of interference and failure.

Malfunctions or failure may however arise if several limiting conditions are simultaneously reached (e.g. max. output current, max. T_A, short circuits etc.)

This is also the case if the outputs are subject to high inductive and capacitive loads since inductive loads, flyback voltages and capacitive loads > 1 nF generate extreme current surges.

High capacitive loads (≥ 100 pF) may lead to stability problems in op amps with high slew rates and high output currents (e.g. TAE 2453/TAE 4453).

There are two known remedies for this;

- Limitation of the output current surges **(figure 1, 3, 4)**
- Stronger or additional frequency compensation **(figure 2)**

Not driving the output hard into saturation i.e. setting the quiescent point in the middle of the control range, when the analog output signal is smaller than the possible control range, will also simplify this problem.

The minimum value for frequency compensation capacitance is given in the data book as follows:

Generator resistances > 10 kΩ
Stray capacitances < 5 pF at the summing point
Loads < 100 pF

In other cases it may be necessary to use a stronger frequency compensation and/or a forward compensation from the input to the output (see TAA 762, test circuit 2 and **figure 1**).

For precision applications or open-loop operations, we recommend that both inputs on the PC board be protected by a guard ring and that the leads running to the inputs be manufactured with a shielded litz wire.

Shields of this kind are also recommended for applications with low input currents (or extremely high feedback resistance).

They prevent parasitic currents from occurring on the PC board – a phenomenon which might arise owing to soiled surfaces, for example.

Figure 1

Improving the stability at high capacitive loads ≥ 100 pF by limiting the surge currents with R.

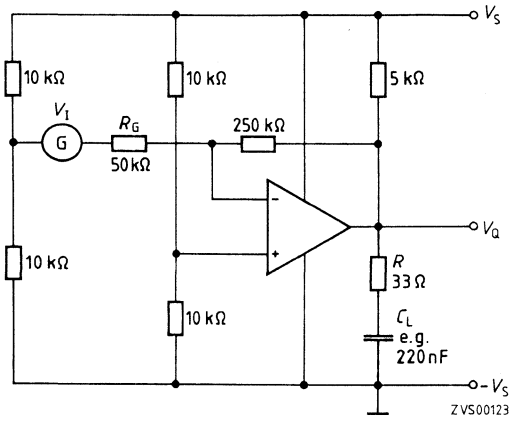


Figure 2

Compensation by means of approx. 220 Ω and 10 nF at input when no compensation point in the op amp is available, e.g. with gain 1, integrators and high capacitive loads.

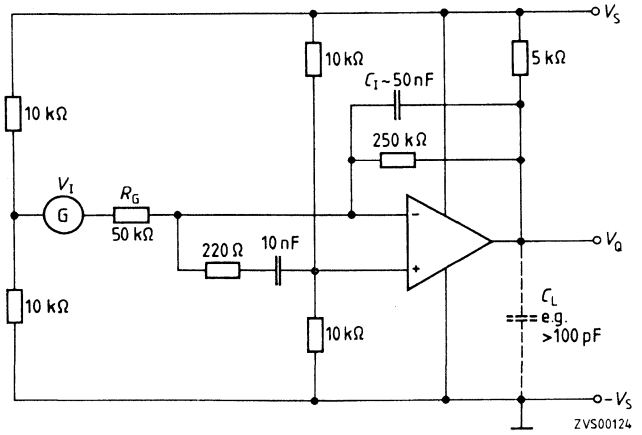
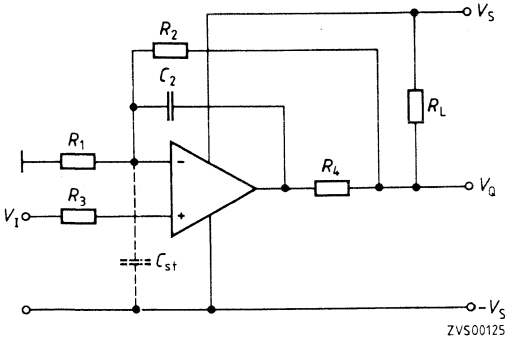


Figure 3

Protecting the inputs and outputs and compensation of the stray capacitance C_{st}



Gain

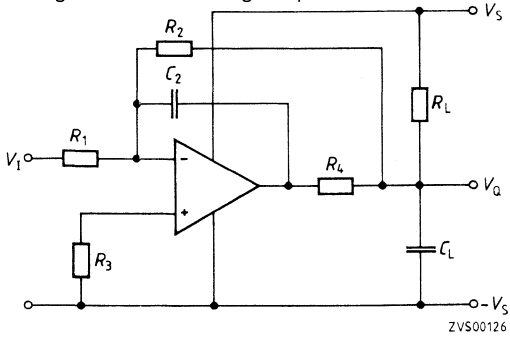
$$G = \frac{R_1 + R_2}{R_1}$$

Compensation

$$C_2 \approx \frac{R_1}{R_2} C_{st}$$

Figure 4

Wiring in the case of large capacitive loads



Gain

$$G = \frac{R_2}{R_1}$$

In figure 4 and 5:

R_3: Input protection; R_4: Output protection;
R_L: Collector resistance (always required for op amps with open collector output).

SIEMENS

Single Operational Amplifiers

TAA 762
TAA 765

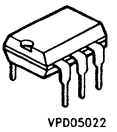
Bipolar IC

Features

- Wide common-mode range
- Large supply voltage range
- Large control range
- Wide temperature range (TAA 762)
- High output frequency compensation
- Open collector output

Applications

- Amplifier
- Comparator
- Level converter
- Driver

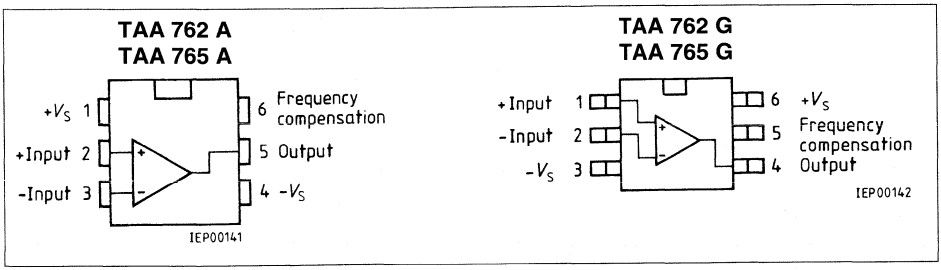


P-DIP-6-1

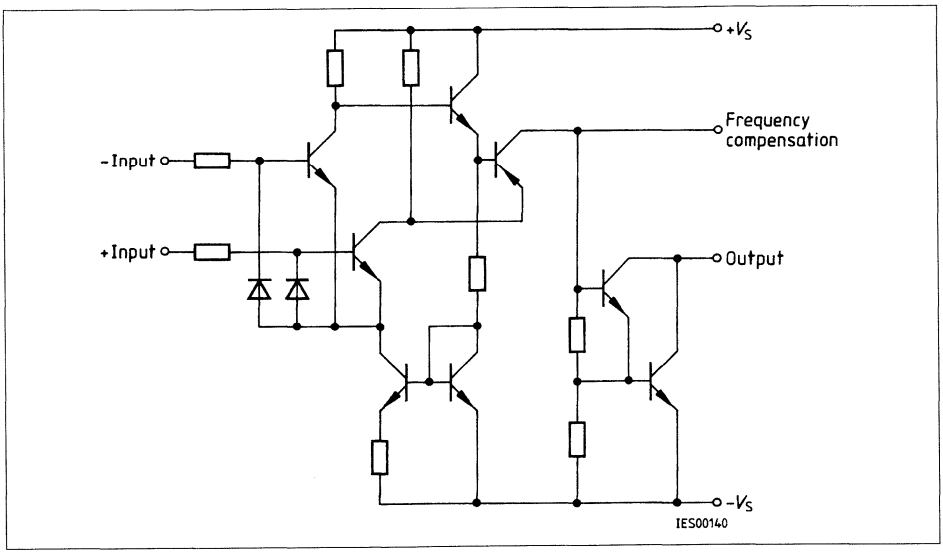
P-DSO-6

Type	Ordering Code	Package
S TAA 762 A	Q67000-A2271	P-DIP-6-1
TAA 762 G	Q67000-A2273	P-DSO-6 (SMD)
S TAA 765 A	Q67000-A524	P-DIP-6-1
S TAA 765 G	Q67000-A599-G403	P-DSO-6 (SMD)

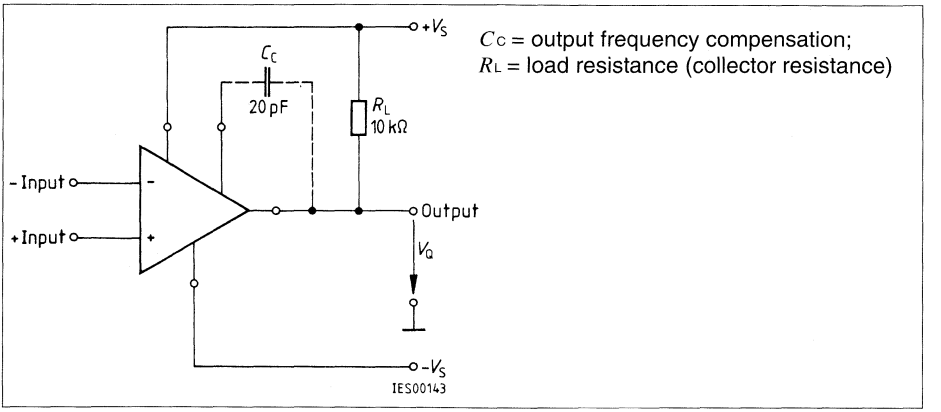
Particularly economic and versatile op amps. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.



Pin Configurations
(top view)



Circuit Diagram



C_C = output frequency compensation;
R_L = load resistance (collector resistance)

Connection Diagram

Absolute Maximum Ratings (TAA 762)

Parameter		Symbol	Limit Values	Unit
Supply voltage		V_S	± 18	V
Output current		I_Q	70	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	– 55 to 125	°C
Thermal resistance				
system – air	TAA 762 A	$R_{th\,SA}$	115	K/W
	TAA 762 G	$R_{th\,SA}$	200	K/W

Operating Range (TAA 762)

Supply voltage	V_S	± 1.5 to ± 18	V
Ambient temperature	T_A	– 55 to 125	°C

Characteristics (TAA 762)
$V_S = \pm 5$ V to ± 15 V; $R_L = 2\,k\Omega$,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current	I_{IO}	– 100	± 50	100	– 300	300	nA
Input current	I_I		0.3	0.7		1.0	µA
Control range							
$V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		– 14	14.8	– 14	V
$R_L = 620\,\Omega$, $V_S = \pm 15$ V	$V_{Q\,pp}$	14.9		– 12.5	14.8	– 12	V
$V_S = \pm 15$ V, $f = 100$ kHz	$V_{Q\,pp}$		± 10				V
Input impedance $f = 1$ kHz	Z_I		200				kΩ
Open-loop voltage gain							
$f = 1$ kHz	G_{V0}	85	87		80		dB
$R_L = 10\,k\Omega$, $f = 1$ kHz	G_{V0}		92				dB
$f = 1$ MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			1		5	µA

Characteristics (TAA 762) (cont'd)
$V_S = \pm 5$ V to ± 15 V; $R_L = 2\,k\Omega$,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.3	1.5		1.5	nA/K
Slew rate of V_Q for non-inverting operation (**test circuit 1**)	SR		9				V/µs
Slew rate of V_Q for inverting operation (**test circuit 2**)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5\,k\Omega$	V_n		3				µV

Characteristics (TAA 762)
$V_S = \pm 2$ V; $R_L = 2\,k\Omega$

Input offset voltage $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 70	 0.2	70 0.5	– 200	200 0.8	nA µA
Open-loop voltage gain $f = 1$ kHz	G_{V0}	80			75		dB

Absolute Maximum Ratings (TAA 765)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system – air TAA 765 A	$R_{th\ SA}$	115	K/W
TAA 765 G	$R_{th\ SA}$	200	K/W

Operating Range (TAA 765)

Supply voltage	V_S	± 1.5 to ± 18	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristics (TAA 765)

V_S = ± 5 V to ± 15 V; R_L = 2 kΩ, unless otherwise specified

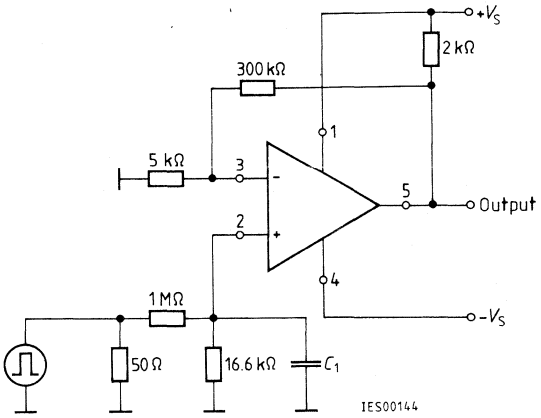
Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = – 25 to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption	I_S		1.5	2.5		2.5	mA
Input offset voltage R_G = 50 Ω	V_{IO}	– 5.5		5.5	– 7	7	mV
Input offset current	I_{IO}	– 200	± 80	200	– 300	300	nA
Input current	I_I		0.5	0.8		1.0	µA
Control range							
V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14	14.8	– 14	V
R_L = 620 Ω, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 12.5	14.8	– 12	V
V_S = ± 15 V, f = 100 kHz	$V_{Q\,pp}$		± 10				V
Input impedance f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain							
f = 1 kHz	G_{V0}	80	85		80		dB
R_L = 10 kΩ, f = 1 kHz	G_{V0}		90				dB
f = 1 MHz	G_{V0}		43				dB
Output reverse current	I_{QR}			10		20	µA

Characteristics (TAA 765) (cont'd)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -25$ to $85\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	200		200	µV/V
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6	25		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{VIO}		0.3	1.5		1.5	nA/K
Slew rate of V_Q for non-inverting operation (test circuit 1)	SR		9				V/µs
Slew rate of V_Q for inverting operation (test circuit 2)	SR		18				V/µs
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5\,k\Omega$	V_n		3				µV

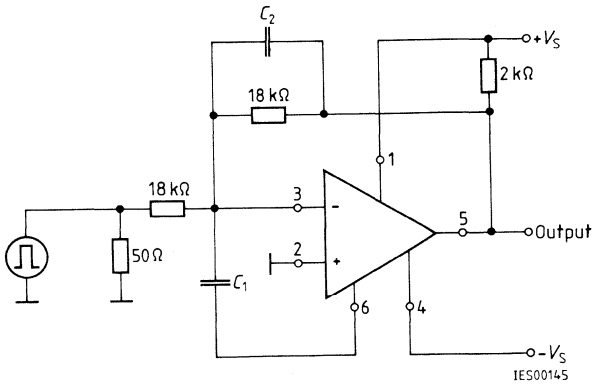
Characteristics (TAA 765)
$V_S = \pm 2\,V$; $R_L = 2\,k\Omega$

Input offset voltage $R_G = 30\,\Omega$	V_{IO}	– 6		6	– 7.5	7.5	mV
Input offset current	I_{IO}	– 150		150	– 200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain $f = 1\,kHz$	G_{V0}	75			75		dB



C_1 for min. overshoot (approx. 22 pF)

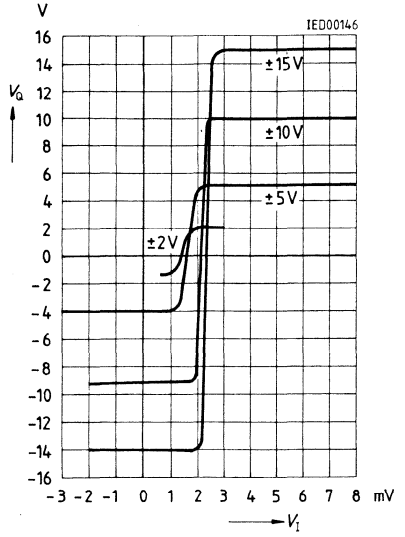
Test Circuit 1 for Slew Rate (non-inverting operation)



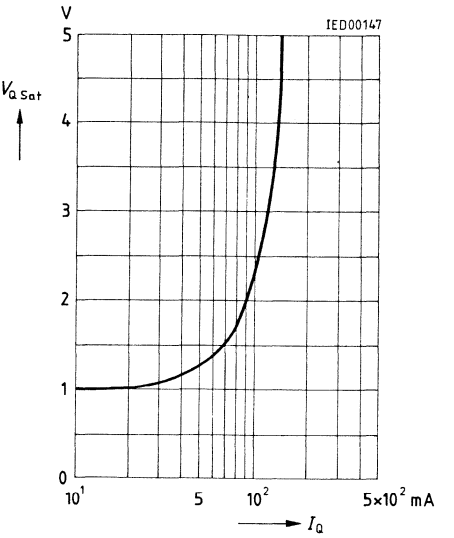
C_2 causes a frequency-dependent compensation to reduce rise times (approx. 390 pF)
C_1 for min. overshoot (approx. 3.9 pF)

Test Circuit 2 for Slew Rate (inverting operation)

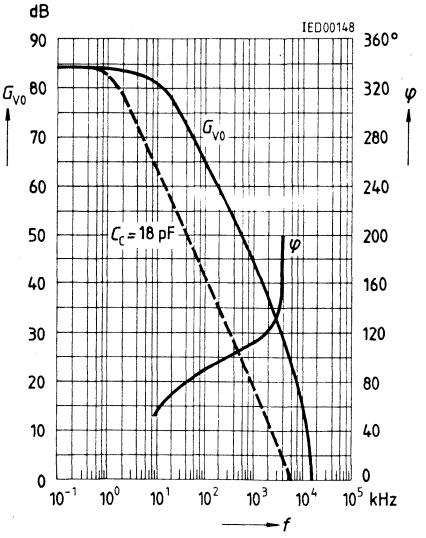
Transfer Characteristic
Output Voltage versus Input Voltage
V_S = parameter, $R_L = 2\,k\Omega$



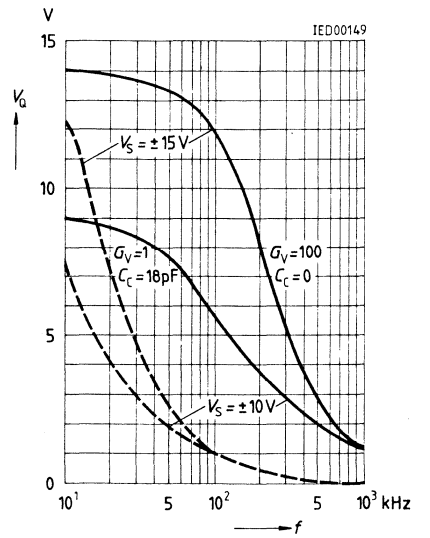
Saturation Voltage versus Output Current
$T_A = 25\,^{\circ}C$



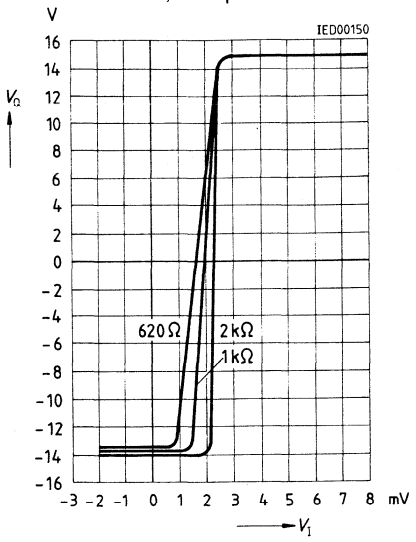
Open-Loop Voltage Gain and Phase versus Frequency
$V_S = \pm 15\,V$; $R_L = 2\,k\Omega$



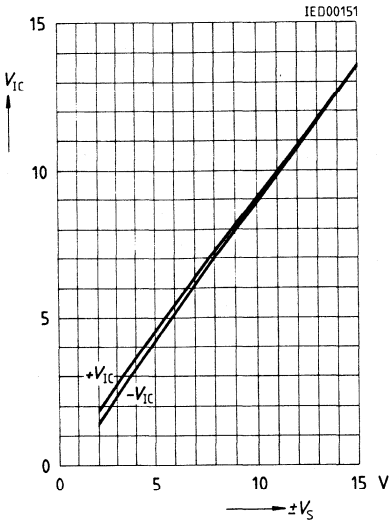
Frequency Dependence of Large Signal Modulation
Output Voltage versus Frequency



Transfer Characteristic
Output Voltage versus Input Voltage
$V_S = \pm 15\,V$; R_L = parameter

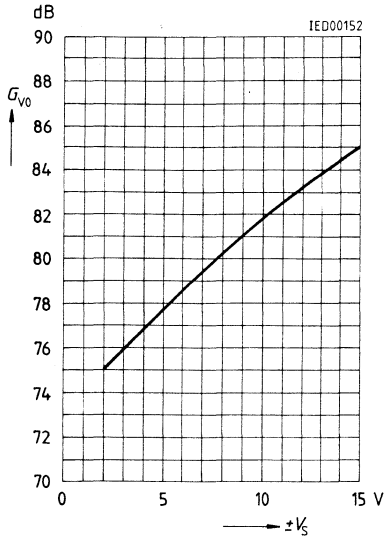


Common-Mode Voltage Range
Common-Mode Input
Voltage versus Supply Voltage

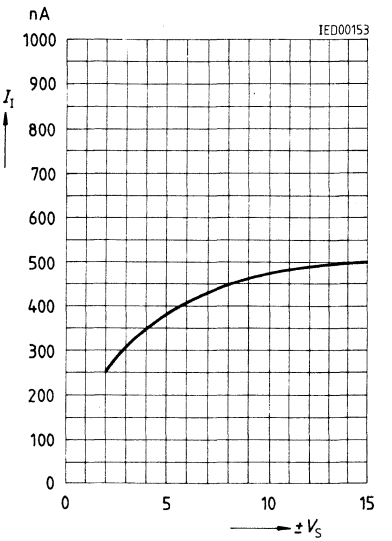


Open-Loop Voltage Gain versus Supply Voltage

$T_A = 25\,^{\circ}C$; $R_L = 2\,k\Omega$

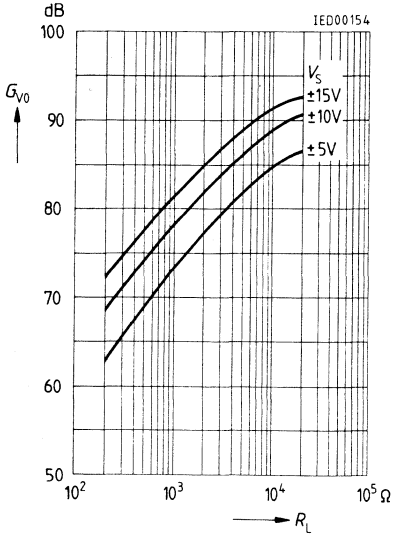


Input Current versus Supply Voltage



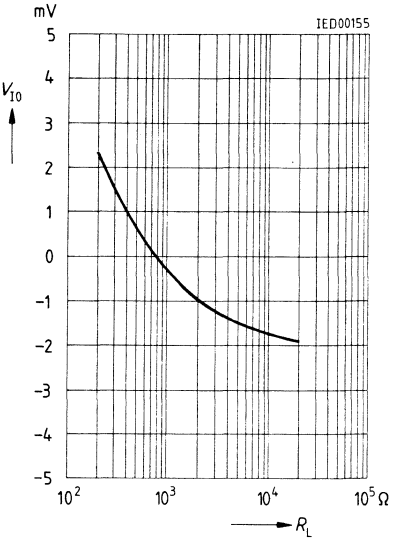
Open-Loop Voltage Gain versus Load Resistance

$T_A = 25\,^{\circ}C$



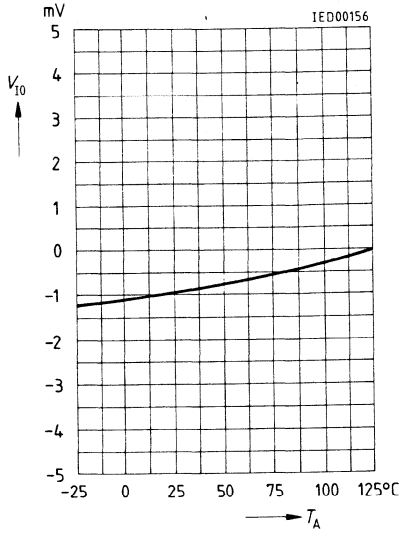
Input Offset Voltage versus Load Resistance

$V_S = \pm 15\,V$



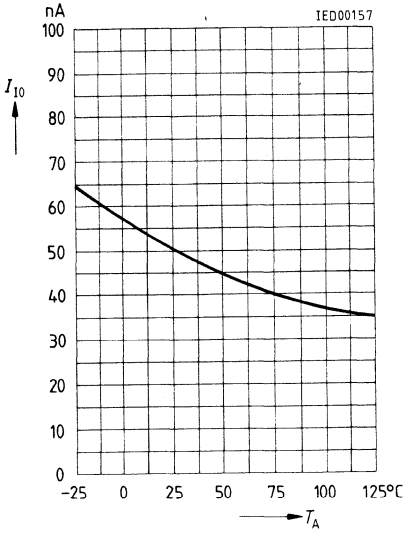
Input Offset Voltage versus Ambient Temperature

$R_L = 2\,k\Omega$, $V_S = \pm 15\,V$



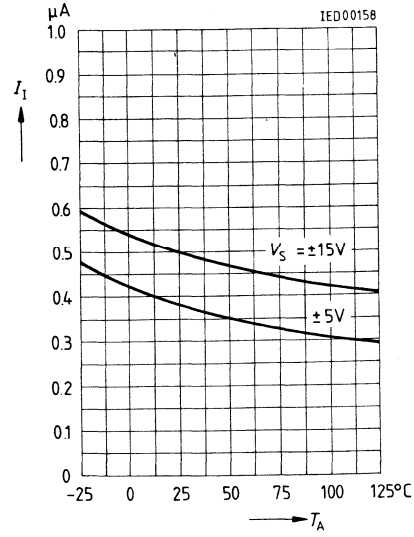
Input Offset Current versus Ambient Temperature

$R_L = 2\,k\Omega$, $V_S = \pm 15\,V$



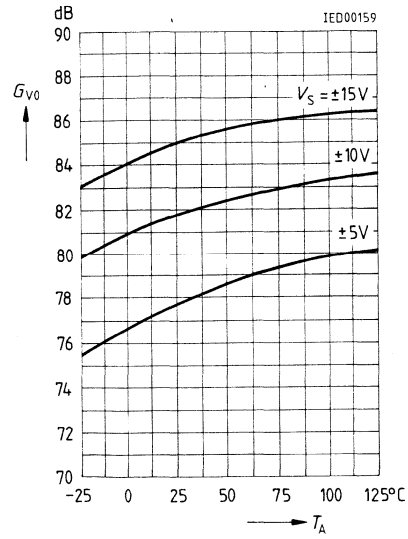
Input Current versus Ambient Temperature

$R_L = 2\,k\Omega$



Open-Loop Voltage Gain versus Ambient Temperature

$R_L = 2\,k\Omega$; $f = 1\,kHz$



SIEMENS

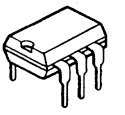
Single PNP Operational Amplifiers

TAE 1453
TAF 1453

Bipolar IC

Features

- PNP input
- Supply voltage range between 3 V and 36 V
- Low current consumption, 0.25 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Wide common-mode range
- Wide operating temperature range (TAF 1453)
- Pin-compatible to TAA 765
- Open collector output



P-DIP-6-1

P-DSO-6

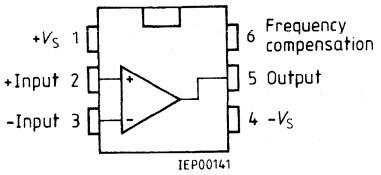
Applications

- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

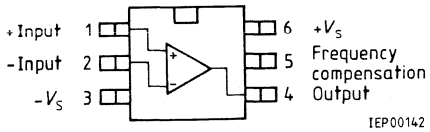
	Type	Ordering Code	Package
S	TAE 1453 A	Q67000-A2017	P-DIP-6-1
S	TAE 1453 G	Q67000-A2106	P-DSO-6 (SMD)
S	TAF 1453 A	Q67000-A2269	P-DIP-6-1
	TAF 1453 G	Q67000-A2209	P-DSO-6 (SMD)

These operational amplifiers are circuits for universal applications having a PNP input differential stage and an open collector output. Apart from one resistor, only active components are used. The integrated regulator provides for all parameters a large degree of independence from the supply voltage.

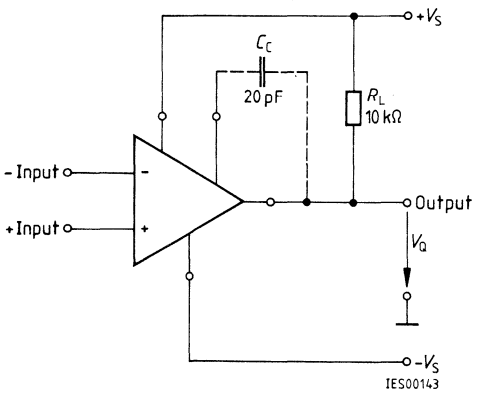
TAE 1453 A
TAF 1453 A



TAE 1453 G
TAF 1453 G



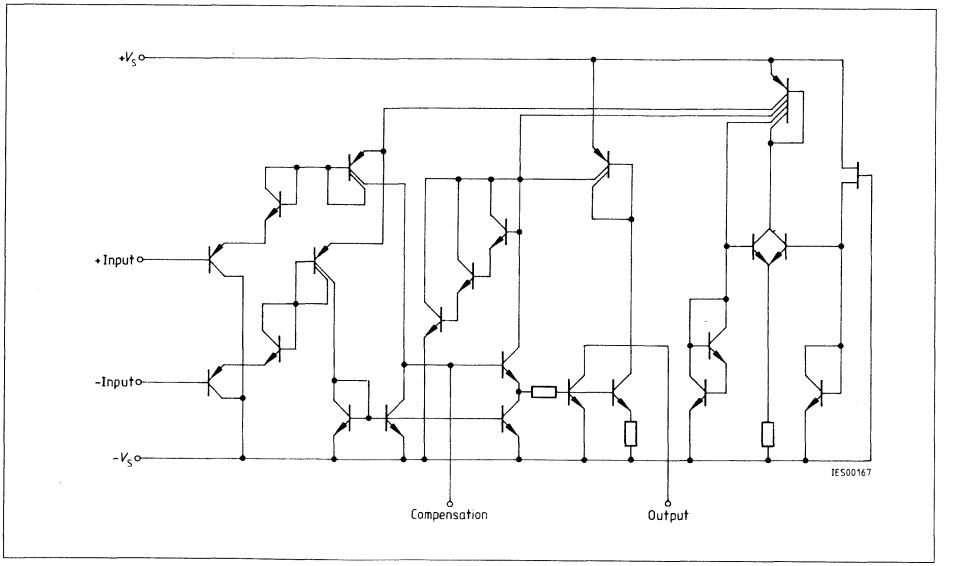
Pin Configuration
(top view)



C_C = output frequency compensation (if required);

R_L = load resistance (collector resistance)

Connection Diagram



Circuit Diagram

Absolute Maximum Ratings (TAE 1453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 150	°C
Thermal resistance system - air TAE 1453 A	$R_{th\,SA}$	135	K/W
TAE 1453 G	$R_{th\,SA}$	200	K/W

Operating Range (TAE 1453)

Supply voltage	V_S	± 2 to ± 18 (± 1.5 V with slightly increased offset voltage)	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristics (TAE 1453)

V_S = ± 5 V to ± 15 V; R_L = 10 kΩ, unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = – 25 to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop current consumption	I_S		0.25	0.4		0.45	mA
Input offset voltage, R_G = 50 Ω	V_{IO}	– 5.5		5.5	– 7	7	mV
Input offset current	I_{IO}	– 15		15	– 100	100	nA
Input current	I_I		40	150		200	nA
Control range							
R_L = 2 kΩ, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.7	14.9	– 14.7	V
R_L = 620 Ω, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.5	14.9	– 14.4	V
R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz	$V_{Q\,pp}$	10		– 10			V
Input impedance, f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain	G_{V0}	78	85		78		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	– V_S – 0.2		V_S – 1.8	– V_S	V_S – 2.0	V

Characteristics (TAE 1453) (cont'd)
$V_S = \pm 5$ V to ± 15 V; $R_L = 10$ kΩ, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -25$ to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Common-mode rejection	k_{CMR}	75	80		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		120	µV/V
Temperature coefficient of I_{IO} $R_G = 50\ \Omega$	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50\ \Omega$	α_{VIO}		6				µV/K
Slew rate for non-inverting operation	SR		20				V/µs
Slew rate for inverting operation	SR		30				V/µs

Characteristics (TAE 1453)
$V_S = \pm 2.5$ V, $R_L = 10$ kΩ

Input offset voltage, $R_G = 50\ \Omega$	V_{IO}	– 6		6	– 7.5	7.5	mV
Input offset current	I_{IO}	– 75		75	– 100	100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain	G_{V0}	70			70		dB

Absolute Maximum Ratings (TAF 1453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system - air TAF 1453 A	$R_{th\ SA}$	135	K/W
TAF 1453 G	$R_{th\ SA}$	200	K/W

Operating Range (TAF 1453)

Supply voltage	V_S	± 2 to ± 18 (± 1.5 V with slightly increased offset voltage)	V
Ambient temperature	T_A	– 55 to 125	°C

Characteristics (TAF 1453)

V_S = ± 5 V to ± 15 V; R_L = 10 kΩ, unless otherwise specified

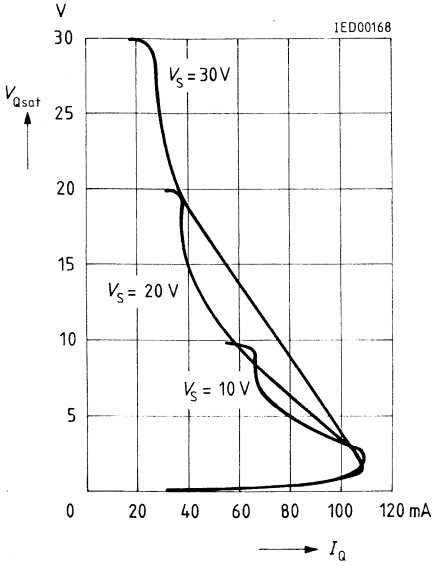
Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = – 55 to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop current consumption (Output in H state)	I_S		0.25	0.35		0.45	mA
Input offset voltage, R_G = 50 Ω	V_{IO}	– 4		4	– 6	6	mV
Input offset voltage Input current	I_{IO} I_I	– 10	 40	10 100	– 75	75 150	nA nA
Control range R_L = 2 kΩ, V_S = ± 15 V R_L = 620 Ω, V_S = ± 15 V R_L = 2 kΩ, V_S = ± 15 V, f = 100 kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9 10		 – 14.7 – 14.5 – 10	 14.9 14.9	 – 14.7 – 14.4	 V V V
Input impedance, f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain	G_{V0}	80	85		75		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S$ – 0.3		V_S – 1.5	$-V_S$	V_S – 1.8	V
Common-mode rejection	k_{CMR}	80	85		75		dB
Supply voltage rejection G_V = 100	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} R_G = 50 Ω Temperature coefficient of V_{IO} R_G = 50 Ω	α_{IIO} α_{VIO}		0.1 6	0.8 25			nA/K µV/K
Slew rate for non-inverting operation Slew rate for inverting operation	SR SR		20 30				V/µs V/µs

Characteristics (TAF 1453)
$V_S = \pm 2.5\,V$; $R_L = 10\,k\Omega$

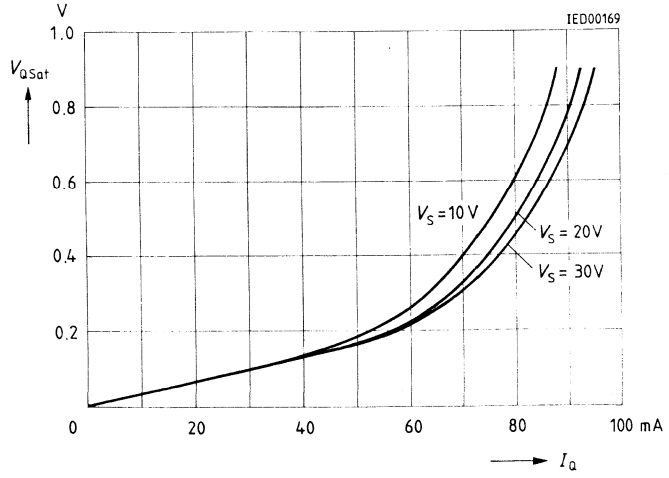
Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -55$ to $125\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset voltage Input current	I_{IO} I_I	– 50	 40	50 100	– 75	75 150	nA nA
Open-loop voltage gain	G_{V0}	75			70		dB

Typical Characteristics of Electrical Parameters

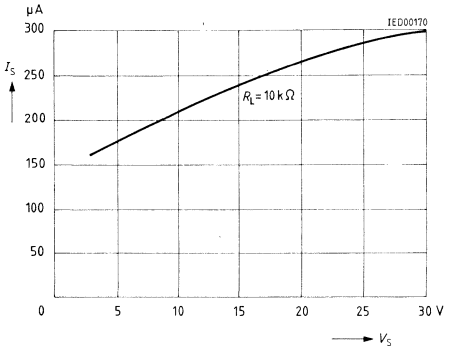
Load Characteristics
Output Saturation Voltage versus Output Current



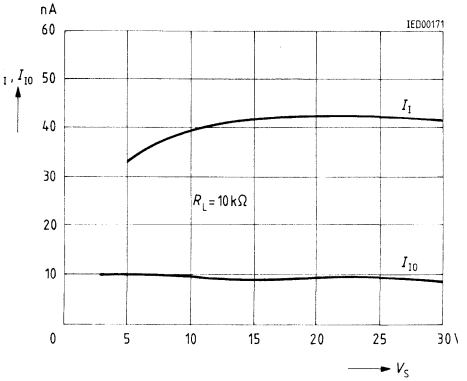
Output Saturation Voltage versus Output Current



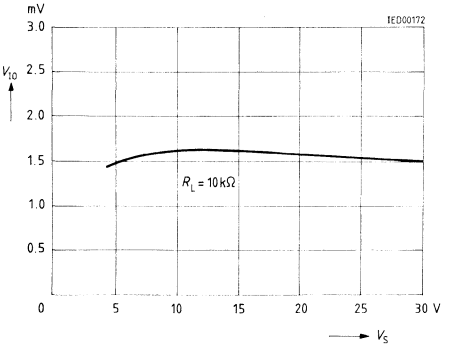
Supply Current versus Supply Voltage



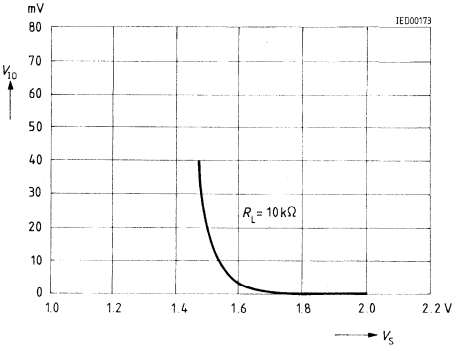
Input Current and Input Offset Current versus Supply Voltage



Input Offset Voltage versus Supply Voltage



V_{IO} Behavior at Low Operating Voltages Input Offset Voltage versus Supply Voltage



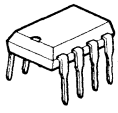
Dual Operational Amplifier

TAA 2762
TAA 2765

Bipolar IC

Features

- Wide common-mode range
- Large supply voltage range
- Wide temperature range (TAA 2762 A)
- High output current
- Large control range
- Internally frequency-compensated
- NPN input with protection diodes
- Open collector output



P-DIP-8

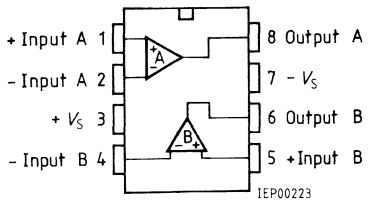
Applications

- Amplifier
- Comparator
- Level converter
- Driver

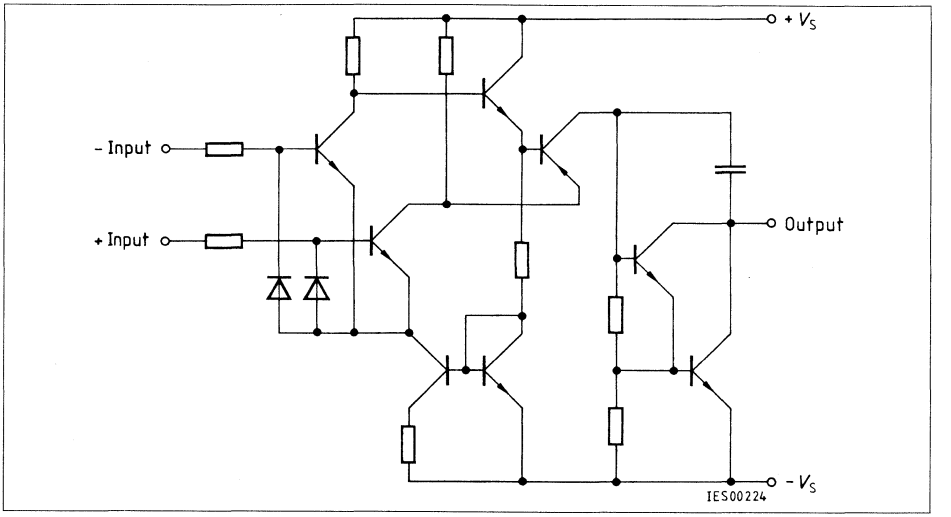
Type	Ordering Code	Package
S TAA 2762 A	Q67000-A2499	P-DIP-8
S TAA 2765 A	Q67000-A1031	P-DIP-8

These op amps are particularly economic and versatile. Owing to their excellent performance qualities they are well suited for a wide scope of applications, as in control engineering, automotive electronics, AF circuits, analog computers, etc.

TAA 2762
TAA 2765



Pin Configuration
(top view)



Circuit Diagram of One Op Amp

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	70	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature Storage temperature range	T_j T_{stg}	150 – 55 to 125	°C °C
Thermal resistance system - air TAA 2762 A/2765 A	$R_{th\,SA}$	100	K/W

Operating Range

Supply voltage		V_S	± 2 to ± 15	V
Ambient temperature	TAA 2762 A TAA 2765 A	T_A T_A	– 55 to 125 – 25 to 85	°C °C

Characteristics (TAA 2762)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -55$ to $125\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 100	± 50 0.3	100 0.7	– 300	300 1.0	nA µA
Control range $V_S = \pm 15\,V$ $R_L = 620\,\Omega$, $V_S = \pm 15\,V$	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 – 14 – 12.5	 14.8 14.8	 – 14 – 12	 V V
Input impedance, $f = 1\,kHz$	Z_I		200				kΩ
Open-loop voltage gain $f = 100\,Hz$ $R_L = 10\,\Omega$, $f = 100\,Hz$	 G_{V0} G_{V0}	 85	 87 92		 80		 dB dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		V_S-2	$-V_S+3$	V_S-3	V
Common-mode rejection	k_{CMR}	80	85			75	dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		1	15		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.3	1.5		1.5	nA/K
Noise voltage (in acc. with DIN 45405; referred to input; $R_S = 2.5\,k\Omega$)	V_n		3				µV
Output saturation voltage $I_Q = 10\,mA$	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation	SR		0.5				V/µs
Slew rate for inverting operation	SR		0.5				V/µs

Characteristics (TAA 2762)

$V_S = \pm 2\,V$, $R_L = 2\,k\Omega$

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -55$ to $125\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 70	 0.2	70 0.5	– 200	200 0.8	nA µA
Open-loop voltage gain; f=100 Hz	G_{V0}	80			75		dB

Characteristics (TAA 2765)

$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -25$ to $85\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		0.5	1.5		1.5	mA
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 5.5		5.5	– 7	7	mV
Input offset current Input current	I_{IO} I_I	– 200	± 80 0.5	200 0.8	– 300	300 1.0	nA µA
Control range $V_S = \pm 15\,V$ $R_L = 620\,\Omega$, $V_S = \pm 15\,V$	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 – 14 – 12.5	 14.8 14.8	 – 14 – 12	 V V
Input impedance, f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain f = 100 Hz $R_L = 10\,\Omega$, f = 100 Hz	 G_{V0} G_{V0}	 80	 85 90		 80		 dB dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range	V_{IC}	$-V_S+2$		$V_S - 2$	$-V_S+3$	$V_S - 3$	V
Common-mode rejection	k_{CMR}	75	83		75		dB
Supply voltage rejection, G_V=100	k_{SVR}		25	100		100	µV/V

Characteristics (TAA 2765) (cont'd)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,°C$			Limit Values $T_A = -25$ to $85\,°C$		Unit
		min.	typ.	max.	min.	max.	
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		1	15		25	µV/K
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.3			1.5	nA/K
Noise voltage (in acc. with DIN 45405, referred to input $R_S = 2.5\,k\Omega$)	V_n		3				µV
Output saturation voltage $I_Q = 10\,mA$	$V_{Q\,sat}$			1			V
Slew rate for non-inverting operation	SR		0.5				V/µs
Slew rate for inverting operation	SR		0.5				V/µs

Characteristics (TAA 2765)
$V_S = \pm 2\,V$, $R_L = 2\,k\Omega$

Parameter	Symbol	Limit Values $T_A = 25\,°C$			Limit Values $T_A = -25$ to $85\,°C$		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 6		6	– 7.5	7.5	mV
Input offset current	I_{IO}	– 150		150	– 200	200	nA
Input current	I_I		0.2	0.6		0.8	µA
Open-loop voltage gain; f=100 Hz	G_{V0}	75			75		dB

Note : For typical performance curves, please refer to the data sheets of TAA 765 and TAA 762.

SIEMENS

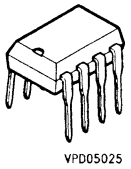
Dual PNP Operational Amplifiers

TAE 2453
TAF 2453

Bipolar IC

Features

- Supply voltage range between 3 V and 36 V
- Low current consumption, 0.8 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (max. 100mA)
- Output virtually short-circuit proof
- Wide common-mode voltage range
- Wide operating temperature range (TAF 2453 A; G)
- Pin-compatible to TBB 1458 B
- The characteristic curves of the electric parameters correspond to those of type TAE 1453 A; G



P-DIP-8

P-DSO-8-1

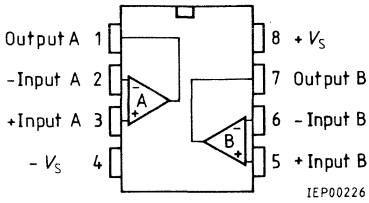
Applications

- Amplifier
- Level converter
- Driver
- Zero voltage switch
- Comparator

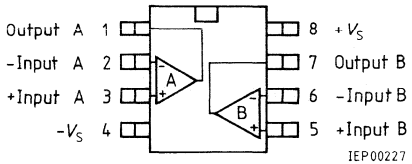
	Type	Ordering Code	Package
S	TAE 2453 A	Q67000-A2107	P-DIP-8
S	TAE 2453 G	Q67000-A2108	P-DSO-8-1 (SMD)
S	TAF 2453 A	Q67000-A2210	P-DIP-8
	TAF 2453 G	Q67000-A2211	P-DSO-8-1 (SMD)

The TAF 2453 / TAE 2453 consists of two independent, frequency-compensated op amps, each having a PNP input differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence from the supply voltage.

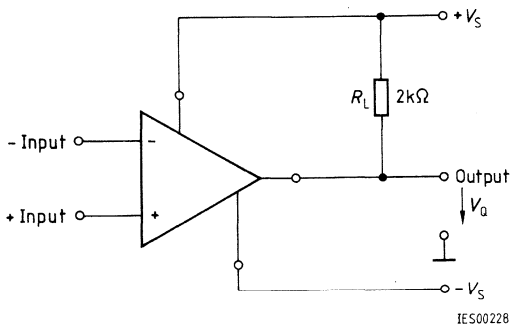
TAE 2453 A
TAF 2453 A



TAE 2453 G
TAF 2453 G

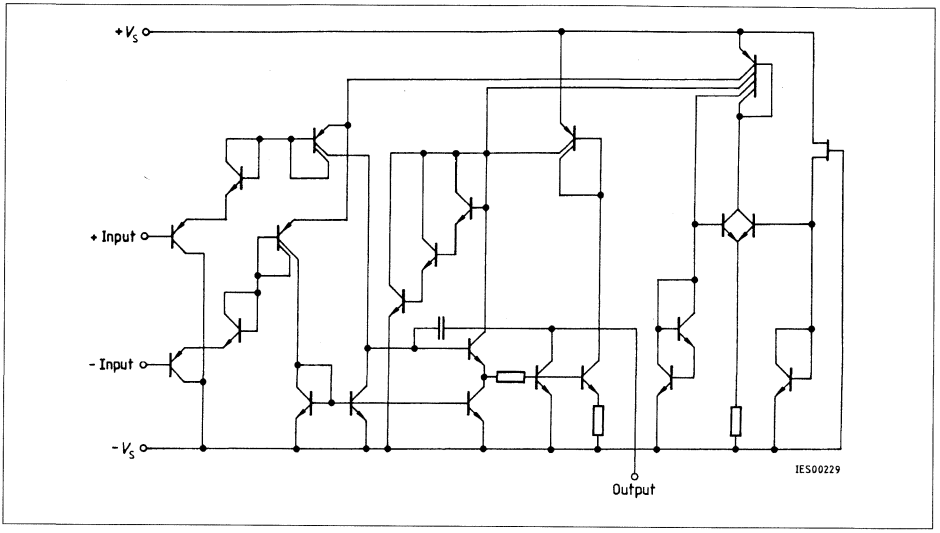


Pin Configurations
(top view)



R_L = load resistance
(collector resistance)

Connection Diagram



Circuit Diagram

Absolute Maximum Ratings (TAE 2453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system – air TAE 2453 A	$R_{th\,SA}$	100	K/W
TAE 2453 G	$R_{th\,SA}$	170	K/W

Operating Range (TAE 2453)

Supply voltage	V_S	± 2 to ± 18 (± 1.5 V with slightly increased offset voltage	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristics (TAE 2453)

V_S = ± 5 V to ± 15 V; R_L = 10 kΩ, unless otherwise specified

		Limit Values T_A = 25 °C			Limit Values T_A = – 25 to 85 °C		
Parameter	Symbol	min.	typ.	max.	min.	max.	Unit
Open-loop supply current consumption, total	I_S		0.8	1.5		1.8	mA
Input offset voltage R_G = 50 Ω	V_{IO}	– 5.5		5.5	– 7	7	mV
Input offset current	I_{IO}	– 15		15	– 100	100	nA
Input current	I_I		40	150		200	nA
Control range							
R_L = 2 kΩ, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.7	– 14.9	– 14.7	V
R_L = 620 Ω, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.5	– 14.9	– 14.4	V
Input impedance f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain R_L = 2 kΩ	G_{V0}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA
Common-mode input voltage range R_L = 2 kΩ	V_{IC}	– V_S – 0.2		V_S – 1.8	– V_S	V_S – 2.0	V
Common-mode rejection R_L = 2 kΩ	k_{CMR}	75	80		75		dB

Characteristics (TAE 2453) (cont'd)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$ min.	typ.	max.	Limit Values $T_A = -25$ to $85\,^\circ C$ min.	max.	Unit
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6				µV/K
Slew rate for non-inverting operation	SR		1				V/µs
Slew rate for inverting operation	SR		1				V/µs

Characteristics (TAE 2453)
$V_S = \pm 2\,V$; $R_L = 10\,k\Omega$

Input offset voltage $R_G = 50\,\Omega$	V_{IO}	– 6		6	– 7.5	7.5	mV
Input offset current	I_{IO}	– 75		75	– 100	100	nA
Input current	I_I		40	150		200	nA
Open-loop voltage gain	G_{V0}	70			70		dB

Absolute Maximum Ratings (TAF 2453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	$\pm V_S$	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 150	°C
Thermal resistance system – air TAF 2453 A	$R_{th\,SA}$	100	K/W
TAF 2453 G	$R_{th\,SA}$	170	K/W

Operating Range (TAF 2453)

Supply voltage	V_S	± 2 to ± 18 ($\pm$ 1.5 V with sligthly increased offset voltage)	V
Ambient temperature	T_A	– 55 to 125	°C

Characteristics (TAF 2453)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 2\,k\Omega$,
unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$ min.	typ.	max.	Limit Values $T_A = -55$ to $125\,^\circ C$ min.	max.	Unit
Open-loop supply current consumption total	I_S		0.8	1.5		1.8	mA
Input offset voltage $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current	I_{IO}	– 10		10	–75	75	nA
Input current	I_I		40	100		150	nA
Control range							
$R_L = 2\,k\Omega$, $V_S = \pm 15\,V$	$V_{Q\,pp}$	14.9		–14.7	14.8	–14.7	V
$R_L = 620\,\Omega$, $V_S = \pm 15\,V$	$V_{Q\,pp}$	14.9		–14.5	14.8	–14.4	V
Input impedance $f = 1\,kHz$	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2\,k\Omega$	G_{V0}	85	87		80		dB
Output reverse current	I_{QR}			1		5	µA
Common-mode input voltage range	V_{IC}	$-V_S$ – 0.3		V_S – 1.5	$-V_S$	V_S – 1.8	V
Common-mode rejection $R_L = 2\,k\Omega$	k_{CMR}	80	85		75		dB
Supply voltage rejection $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.1	0.8		0.8	nA/K
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6	25		25	µV/K
Slew rate for non-inverting operation	SR		1				V/µs
Slew rate for inverting operation	SR		1				V/µs

Characteristics (TAF 2453)
$V_S = \pm 2V$

Parameter	Symbol	Limit Values $T_A = 25\ ^\circ C$			Limit Values $T_A = -55$ to $125\ ^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage $R_G = 50\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 50	 40	50 100	– 75	75 150	nA nA
Open-loop voltage gain $R_L = 2k\Omega$	G_{V0}	75			70		dB

Note: For typical performance curves, please refer to the data sheets of TAE 1453 and TAF 1453.

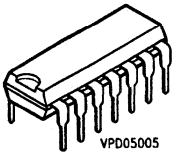
Quad PNP Operational Amplifier

TAE 4453
TAF 4453

Bipolar IC

Features

- Supply voltage range between 3 V and 36 V
- Low current consumption, 1.6 mA typ.
- Extremely large control range
- Low output saturation voltage, almost independent of load current
- Output current up to 70 mA (100 mA max.)
- Output virtually short-circuit proof
- Wide common-mode range
- Wide temperature range (TAF 4453 A; G)
- Pin-compatible to LM 324
- The typical characteristics of the electric parameters correspond to those of the TAE 1453 A; G



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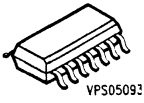


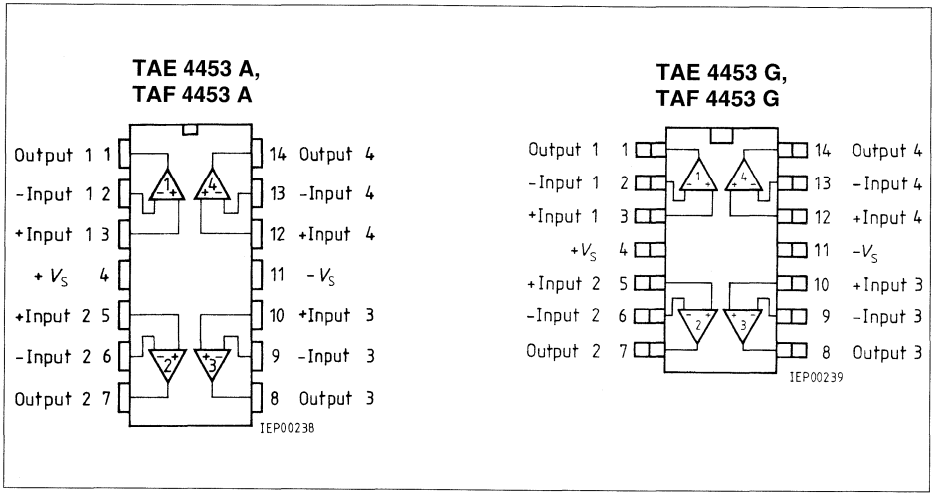
P-DSO-14-1

Applications

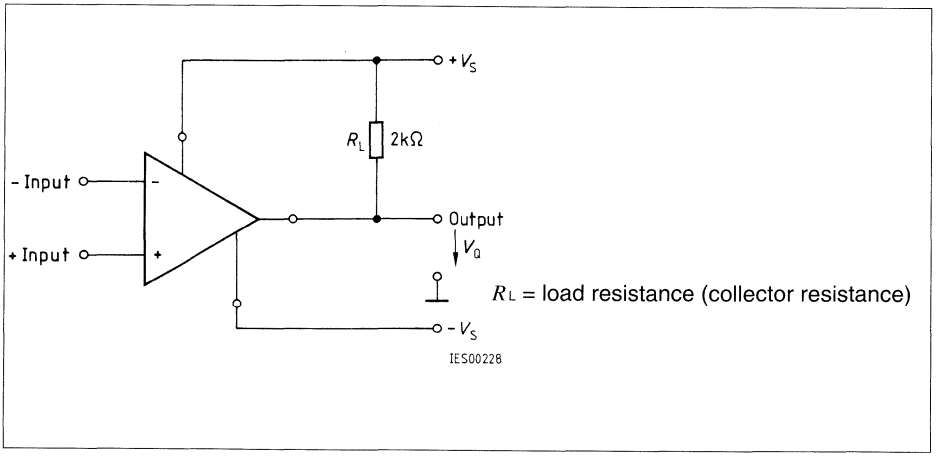
- Amplifier
- Level converter
- Driver
- Offset voltage switch
- Comparator

	Type	Ordering Code	Package
S	TAE 4453 A	Q67000-A2109	P-DIP-14-1
S	TAE 4453 G	Q67000-A2152	P-DSO-14-1 (SMD)
S	TAF 4453 A	Q67000-A2212	P-DIP-14-1
	TAF 4453 G	Q67000-A2213	P-DSO-14-1 (SMD)

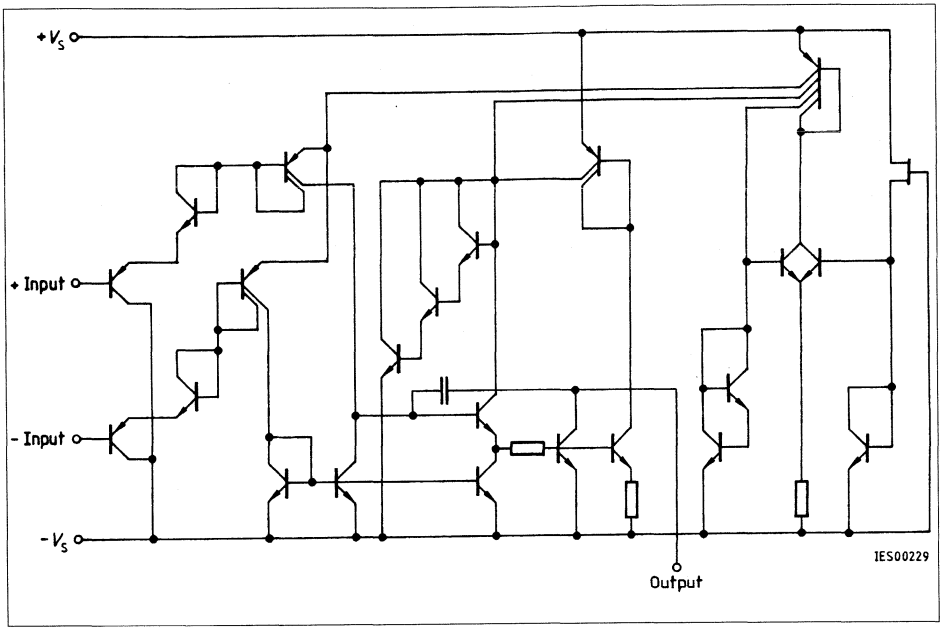
The TAE 4453 / TAF 4453 consists of four independent, frequency-compensated op amps, each having a PNP input, differential stage and an open collector output. The integrated regulator provides for all parameters a large degree of independence of the supply voltage.



Pin Configurations
(top view)



Connection Diagram



Circuit Diagram of One Op Amp

Absolute Maximum Ratings (TAE 4453)

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	± 18	V
Output current	I_Q	100	mA
Differential input voltage	V_{ID}	± V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system – air TAE 4453 A	$R_{th\,SA}$	80	K/W
TAE 4453 G	$R_{th\,SA}$	120	K/W

Operating Range (TAE 4453)

Supply voltage	V_S	± 2 to ± 18 (± 1.5 V with slightly increased offset voltage)	V
Ambient temperature	T_A	– 25 to 85	°C

Characteristics (TAE 4453)

V_S = ± 5 V to ± 15 V; R_L = 10 kΩ, unless otherwise specified

Parameter	Symbol	Limit Values T_A = 25 °C			Limit Values T_A = – 25 to 85 °C		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage, R_G = 50 Ω	V_{IO}	– 5.5		5.5	– 7	7	mV
Input offset current	I_{IO}	– 15		15	– 25	25	nA
Input current	I_I		40	150		200	nA
Control range							
R_L = ± 2 kΩ, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.7	14.9	– 14.7	V
R_L = 620 Ω, V_S = ± 15 V	$V_{Q\,pp}$	14.9		– 14.5	14.9	– 14.4	V
Input impedance, f = 1 kHz	Z_I		200				kΩ
Open-loop voltage gain R_L = 2 kΩ	G_{VO}	80	85		80		dB
Output reverse current	I_{QR}			10		20	µA

Characteristics (TAE 4453) (cont'd)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 10\,k\Omega$, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,°C$			Limit Values $T_A = -25$ to $85\,°C$		Unit
		min.	typ.	max.	min.	max.	
Common-mode input voltage range $R_L = 2\,k\Omega$	V_{IC}	$-V_S$ -0.2		$+V_S$ -1.8	$-V_S$	$+V_S$ -2.0	V
Common-mode rejection $R_L = 2\,k\Omega$	k_{CMR}	75	80		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	µV/V
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.1				nA/K
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6				µV/K
Slew rate for non-inverting operation	SR		1				V/µs
Slew rate for inverting operation	SR		1				V/µs

Characteristics (TAE 4453)
$V_S = \pm 2\,V$

Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	-6		6	-7.5	7.5	mV
Input offset current Input current	I_{IO} I_I	-75	 40	75 150	-100	100 200	nA nA
Open-loop voltage gain; $R_L = 2\,k\Omega$	G_{VO}	70			70		dB

Absolute Maximum Ratings (TAF 4453)

Parameter		Symbol	Limit Values	Unit
Supply voltage		V_S	± 18	V
Output current		I_Q	100	mA
Differential input voltage		V_{ID}	± V_S	V
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	– 55 to 125	°C
Thermal resistance system – air	TAF 4453 A	$R_{th\ SA}$	80	K/W
	TAF 4453 G	$R_{th\ SA}$	120	K/W

Operating Range (TAF 4453)

Supply voltage	V_S	± 2 to ± 18 (± 1.5 V with slightly increased offset voltage)	V
Ambient temperature	T_A	– 55 to 125	°C

Characteristics (TAF 4453)
$V_S = \pm 5\,V$ to $\pm 15\,V$; $R_L = 10\,k\Omega$, unless otherwise specified

Parameter	Symbol	Limit Values $T_A = 25\,^\circ C$			Limit Values $T_A = -55$ to $125\,^\circ C$		Unit
		min.	typ.	max.	min.	max.	
Open-loop supply current consumption, total	I_S		1.6	3.0		3.6	mA
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 10	 40	10 100	– 15	15 150	nA nA
Control range $R_L = 2\,k\Omega$, $V_S = \pm 15\,V$ $R_L = 620\,\Omega$, $V_S = \pm 15\,V$	 $V_{Q\,pp}$ $V_{Q\,pp}$	 14.9 14.9		 – 14.7 – 14.5	 14.8 14.8	 – 14.7 – 14.4	 V V
Input impedance, $f = 1\,kHz$	Z_I		200				kΩ
Open-loop voltage gain $R_L = 2\,k\Omega$	G_{VO}	85	87		80		dB
Output reverse current	I_{QR}			1		5	μA
Common-mode input voltage range $R_L = 2\,k\Omega$	V_{IC}	$-V_S$ – 0.3		$+V_S$ – 1.5	$-V_S$	$+V_S$ – 1.8	V
Common-mode rejection $R_L = 2\,k\Omega$	k_{CMR}	80	85		75		dB
Supply voltage rejection, $G_V = 100$	k_{SVR}		25	100		100	μV/V
Temperature coefficient of I_{IO} $R_G = 50\,\Omega$	α_{IIO}		0.1	0.8		0.8	nA/K
Temperature coefficient of V_{IO} $R_G = 50\,\Omega$	α_{VIO}		6	25		25	μV/K
Slew rate for non-inverting operation	SR		1				V/μs
Slew rate for inverting operation	SR		1				V/μs

Characteristics (TAF 4453)
$V_S = \pm 2$ V

Parameter	Symbol	Limit Values $T_A = 25$ °C			Limit Values $T_A = -55$ to 125 °C		Unit
		min.	typ.	max.	min.	max.	
Input offset voltage, $R_G = 50\,\Omega$	V_{IO}	– 4		4	– 6	6	mV
Input offset current Input current	I_{IO} I_I	– 50	 40	50 100	– 75	75 150	nA nA
Open-loop voltage gain $R_L = 2\,k\Omega$	G_{V0}	75			70		dB

Note: For typical performance curves, please refer to the data sheets of TAE 1453 and TAF 1453.

Selector Guide

Type	Package	Operating Range			Electrical Characteristics $V_S = \pm 15$ V, $T_A = 25$ °C	Page
		Supply Voltage V_S V	Operating Temperature T_A °C	Output current I_Q mA max	Input Offset Voltage ($R_G = 50\,\Omega$) V_{IO} mV min/max	
Threshold Switches						
TCA 105	P-DIP-6-1	30	– 25 to 85	50		
TCA 105 B	P-DIP-6-1	20	– 25 to 85	50		
TCA 105 G	P-DSO-6	30	– 25 to 85	50		
TCA 965 B	P-DIP-14-1	4.75 to 27	– 25 to 85	50		
TCA 965 BG	P-DSO-14-1	4.75 to 27	– 25 to 85	50		
Current-Monitoring IC						
TLE 4951	P-DIP-14-1	4.5 to 32	– 40 to 125	40		
TLE 4951 G	P-DSO-14-1	4.5 to 32	– 40 to 125	40		

= SMD

SIEMENS

Threshold Switch

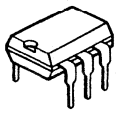
TCA 105

Bipolar IC

3

Features

- Wide range of supply voltage, 4.5 to 30 V
- High output current, 50 mA
- TTL-compatible
- Triggerable with DC signal



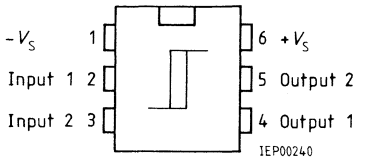
P-DIP-6-1

P-DSO-6

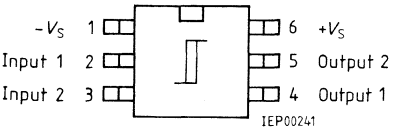
	Type	Ordering Code	Package
S	TCA 105	Q67000-A527	P-DIP-6-1
S	TCA 105 B	Q67000-A587	P-DIP-6-1
S	TCA 105 G	Q67000-A988	P-DSO-6 (SMD)

The TCA 105 contains an oscillator stage, a threshold switch, and two anti-valent output stages. The IC is especially suitable for application in proximity switches, light reflection switches, and other contactless switching applications.

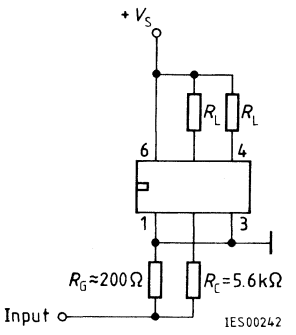
TCA 105, TCA 105 B



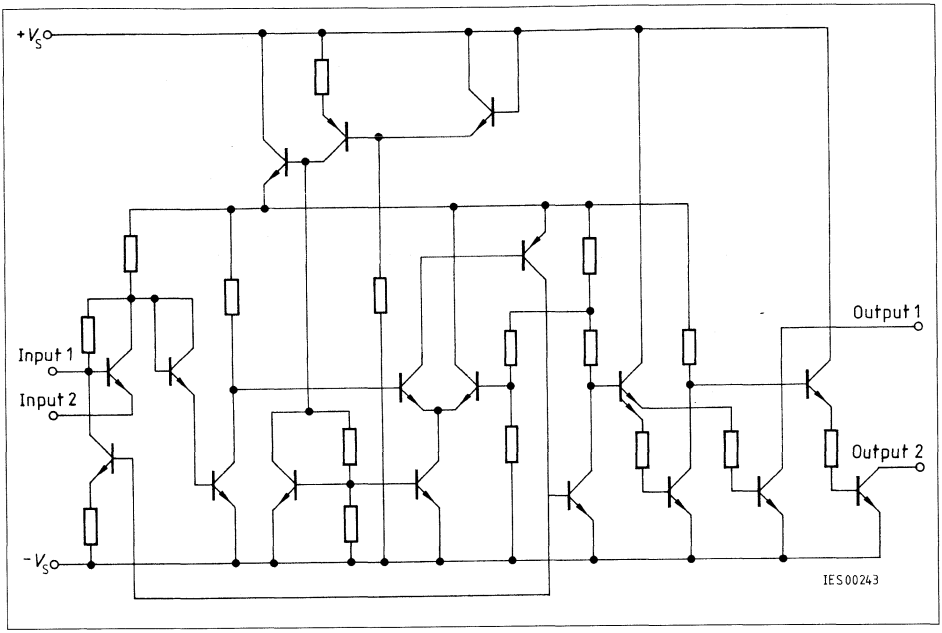
TCA 105 G



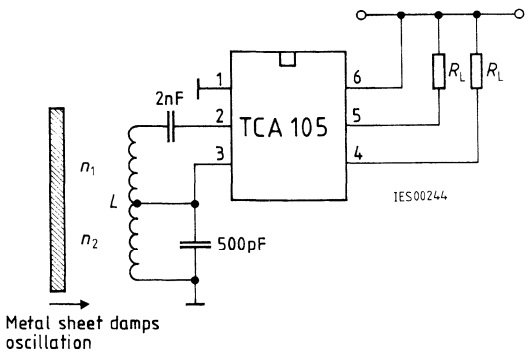
Pin Configuration
(top view)



Test Circuit



Circuit Diagram



Typical dimensioning values:

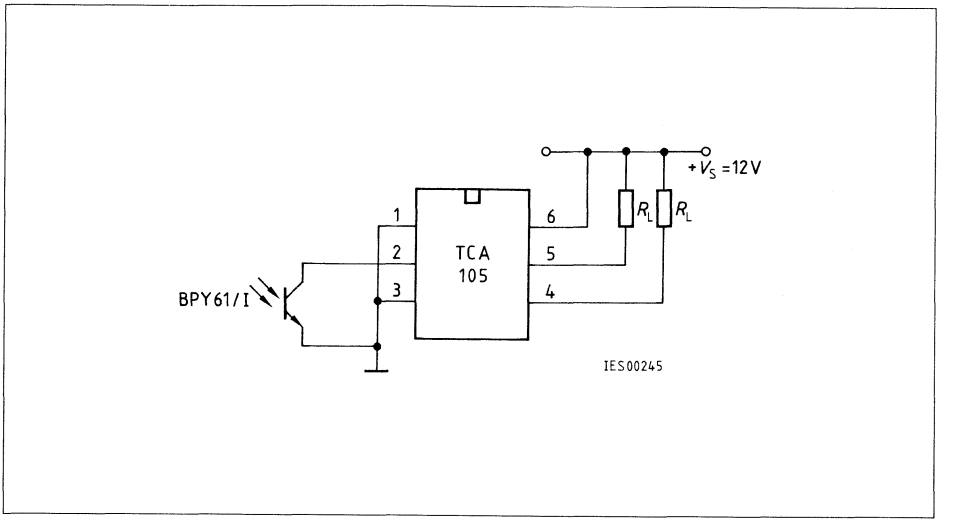
Ferrite pot cores, 9 mm dia.
Ordering code B65935-A-X25
Cu litz wire 12 × 0.04 mm

Slot switch:
Number of turns: $n = 2 \times 25$
Distance between pot core halves: 2.5 to 3.5 mm

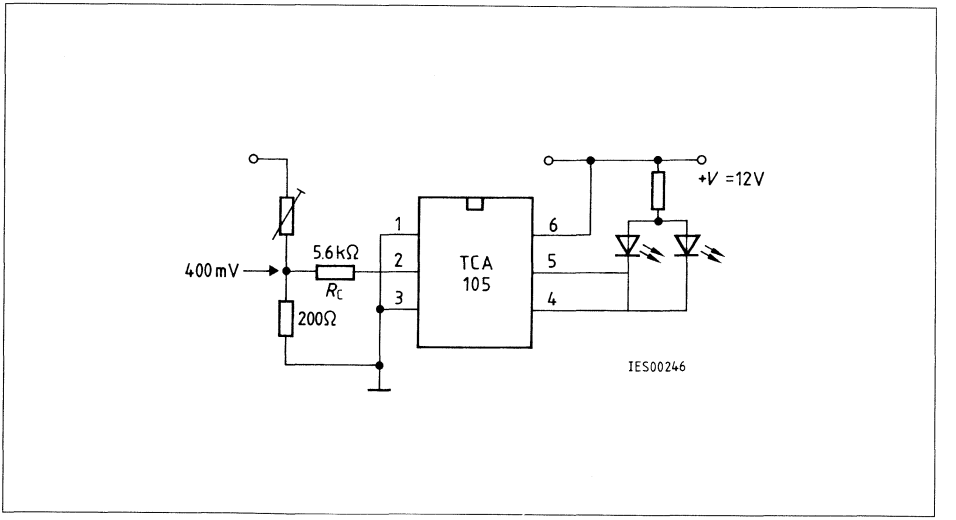
Proximity switch:
Number of turns: $n_1 = 8$, $n_2 = 40$
Distance: 2 to 3 mm

Application Example
Inductive Slot Switch or Proximity Switch

Applications Examples



Light-Operated Switch (switching amplifier for phototransistor BPY 61)



Voltage Monitor

Absolute Maximum Ratings

Parameters	Symbol	Limit Values		Unit
		TCA 105	TCA 105 B	
Supply voltage	V_S	30	20	V
Output voltage (pin 4, pin 5)	V_Q	30	20	V
Output current	I_Q	50	50	mA
Switching frequency	f_S	40	40	kHz
Input voltage	V_I	≥ 0 [1]	≥ 0 [1]	V
Junction temperature	T_j	150	150	°C
Storage temperature range	T_{stg}	– 55 to 125	– 55 to 125	°C
Thermal resistance (system – air)				
TCA 105, TCA 105 B	$R_{th\,SA}$	115	115	K/W
TCA 105 G	$R_{th\,SA}$	200		K/W

Operating Range

Supply voltage	V_S	4.75 to 30	4.75 to 20	V
Ambient temperature	T_A	– 25 to 85	– 25 to 85	°C
Oscillating frequency	f_{OSC}	1 to 4.5	1 to 4.5	MHz

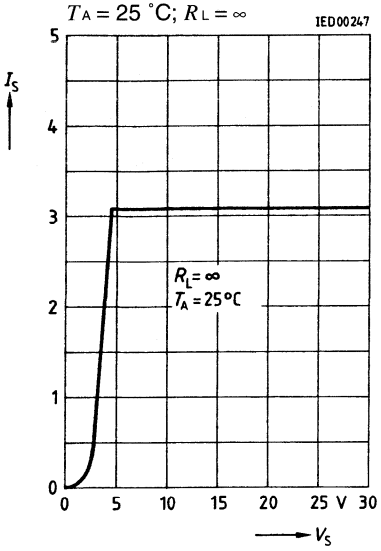
[1] Negative input voltages are not permitted

Characteristics
Static measurement, pins 3 and 1 interconnected
V_S = 12 V, T_A = 25 °C, R_C = 5.6 kΩ

Parameters	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current	I_S		3.4	5	mA
Input threshold voltage with compensation resistor R_C	V_I	300	400	480	mV
Input threshold current	I_I		– 60		µA
Hysteresis	V_{hy}	20	35	50	mV
L-output voltage I_Q = 16 mA	V_{QL}		0.25	0.35	V
H-output voltage	V_{QH}	corresponds to V_S			
Reverse current, V_S = 30 V and/or 20 V	I_{QH}			60	µA
L-output voltage I_Q = 50 mA	V_{QL}		0.7	1.15	V
Switching time in TTL operation I_Q = 16 mA	t		3		µs

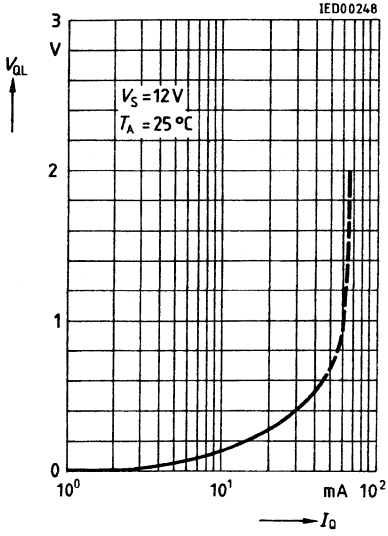
Current Consumption
Supply Current versus
Supply Voltage

$T_A = 25\ ^\circ C$; $R_L = \infty$



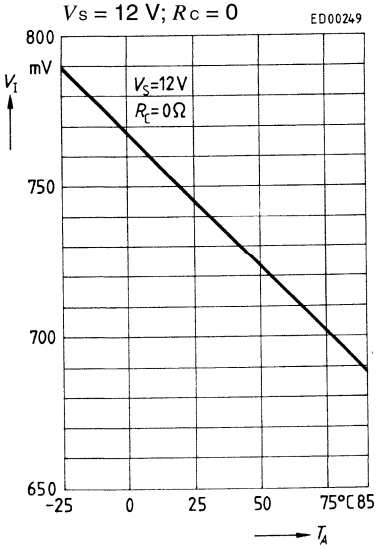
L-Output Voltage versus
Output Current

$T_A = 25\ ^\circ C$; $V_S = 12$ V



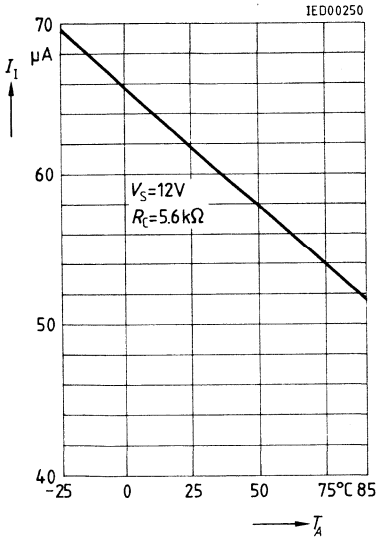
Switching Threshold
Input Voltage versus
Ambient Temperature

$V_S = 12$ V; $R_C = 0$

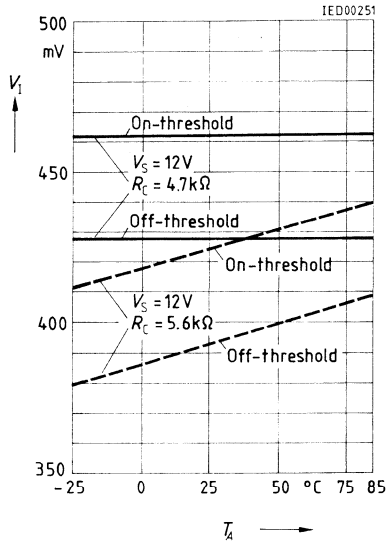


Input Current versus
Ambient Temperature

$V_S = 12$ V; $R_C = 5.6$ kΩ

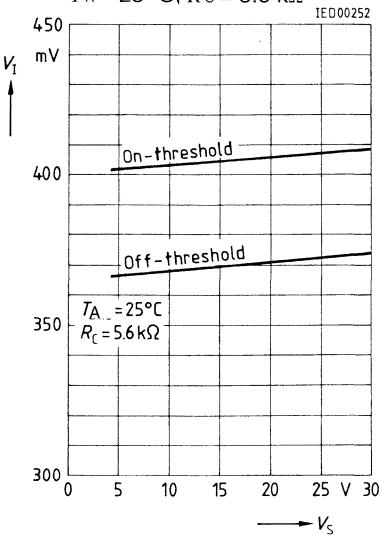


Switching Threshold Input Voltage versus Ambient Temperature



Switching Threshold Input Voltage versus Supply Voltage

$T_A = 25\ ^\circ C$; $R_C = 5.6\ k\Omega$



Window Discriminator

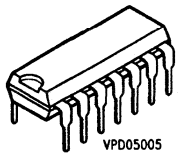
TCA 965 B

Preliminary

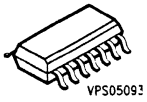
Bipolar IC

Features

- Two window settings
  - direct setting of lower and upper edge voltage (window edges)
  - indirect setting by window center voltage and half window width
- Adjustable hysteresis
- Digital outputs with open collectors for currents up to 50 mA
- Adjustable reference voltage V_{Stab}



P-DIP-14



P-DSO-14-1

Type	Ordering Code	Package
▼ S TCA 965 B	Q67000-A8338	P-DIP-14-1
▼ S TCA 965 BG	Q67000-A8337	P-DSO-14-1 (SMD)

▼ New type

The window discriminator compares an input voltage to a defined voltage window. The digital outputs show whether the input voltage is below, within or above this window.

The TCA 965 B window discriminator is especially suitable as a tracking or compensating controller with a dead band in control engineering and for the selection of DC voltages within a certain tolerance of the required setpoint value in measurement engineering. When it is used as a Schmitt trigger, switching frequencies up to a typical value of 50 kHz are possible.

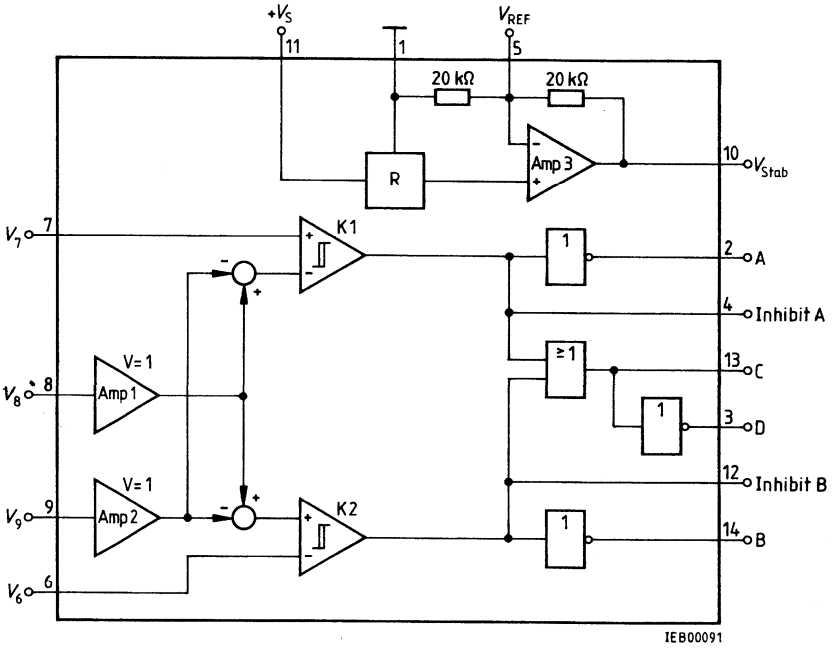
Functional Description

Amplifier Amp 3 increases the voltage of the reference source R to $V_{Stab} = 2 \times V_{REF}$. The amplification factor can be altered by external wiring. With direct setting of the window, the input voltage appears on amplifier Amp 1 (V_8), the upper edge voltage on comparator K2 (V_6) and the lower edge voltage on comparator K1 (V_7).

With indirect setting of the window, the input voltage appears on inputs V_6 and V_7, while the center voltage is connected to amplifier A1 (V_8).

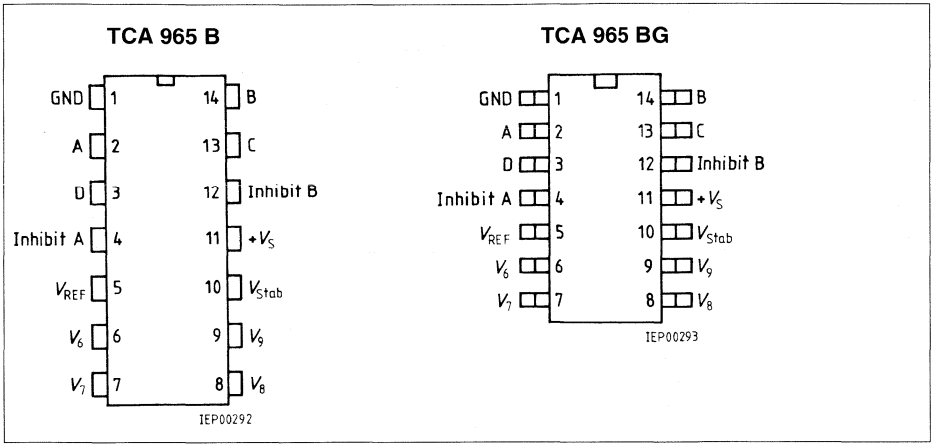
The voltage applied to the input (V_9) of amplifier Amp 2 is subtracted symmetrically from the output voltage of amplifier Amp 1 and added. The comparators switch with hysteresis. The logic gates have open-collector outputs.

If the inhibit input A or B is connected to ground, output A or B will always be high.



Outputs A, B, C, D are open-collector

Block Diagram



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Pin Function in direct setting of window	Pin Function in indirect setting
1	GND	GND	
2	A	Logic output A	
3	D	Logic output D = A @ B (AND)	
4	Inhibit A	Connected to GND: logic output A = HIGH	
5	V_{REF}	Internal V_{REF} = 3 V	
6	V_6	Upper edge voltage	Input voltage $V_{6/7}$
7	V_7	Lower edge voltage	Input voltage $V_{6/7}$
8	V_8	Input voltage	Center voltage
9	V_9	GND	Half window width
10	V_{Stab}	Internal V_{Stab} = 6 V	
11	$+V_S$	Supply voltage	
12	Inhibit B	Connected to GND: logic output B = HIGH	
13	C	Logic output C = A @ B (NAND)	
14	B	Logic output B	

Absolute Maximum Ratings

Maximum ratings for ambient temperature $T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage (pin 11)	V_S		30	V
Difference in input voltage between pins 6, 7, 8	V_I		15	V
Input voltage (pins 6, 7, 8, 9)	V_I		30	V
Output current (pins 2, 3, 13, 14)	I_Q		50	mA
Output voltage (pins 2, 3, 13, 14) independent of V_S	V_Q		30	V
Voltage on V_{REF} (pin 5)	V_R		8	V
Output current of stabilized voltage (pin 10)	I_{10}		10	mA
Inhibit input voltage (pins 4, 12)	V_{IH}		7	V
Junction temperature	T_j		150	°C
Storage temperature	T_{Stg}	– 55	125	°C
Thermal resistance system-air P-DIP-14	$R_{th\,SA}$		80	K/W
P-DSO-14	$R_{th\,SA}$		125	K/W

Operating Range

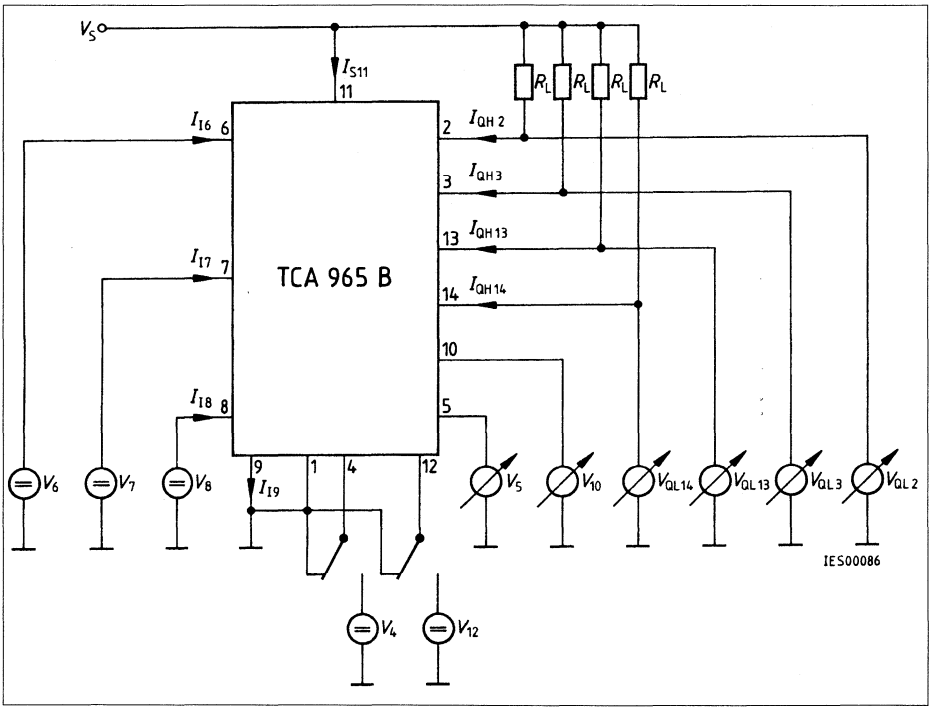
Supply voltage	V_S	4.5	30	V
Ambient temperature	T_A	– 25	85	°C

3

Characteristics
V_S = 10 V; T_A = 25 °C

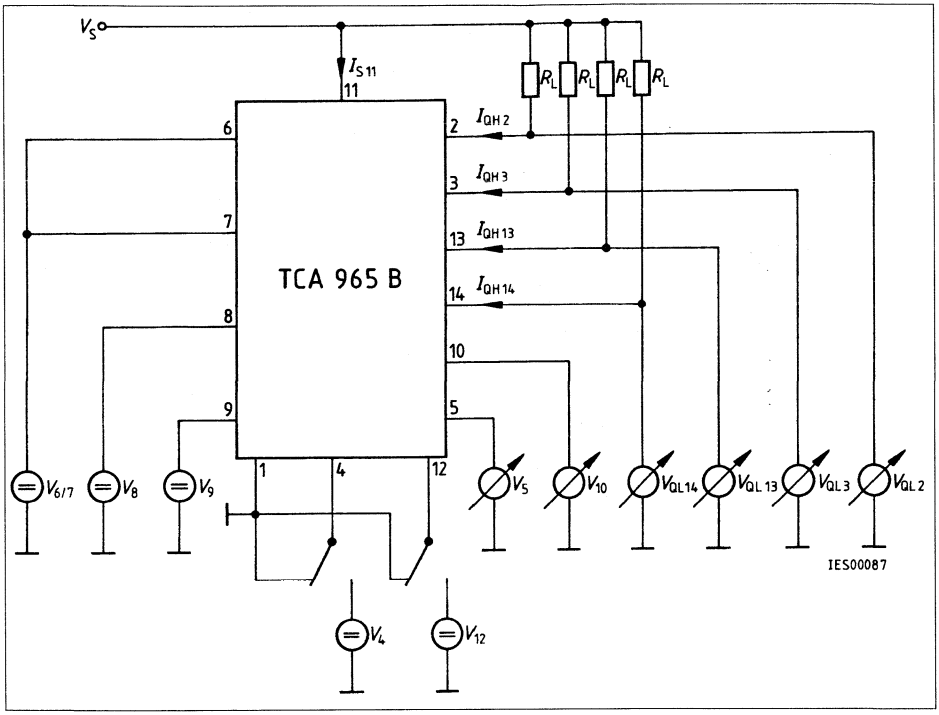
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Ciruit
		min.	typ.	max			
Current consumption	I_S		5	7	mA	V_2, $V_{13} = V_{QH}$	1
Input current (pins 6, 7, 8)	I_I		20	50	nA		1
Input current, pin 9	$-I_I$		400	3000	nA		1
Input offset voltage in direct setting of window	V_{IO}	– 20		20	mV		1
Input offset voltage in indirect setting of window	V_{IO}	– 50		50	mV		2
Input-voltage range on pins 6, 7, 8	V_I	1.5		$V_S - 1$	V	$\Delta V_I < 13$ V	1
Input-voltage range on pin 9	V_I	50		$V_S/2$	mV		2
Differential input voltage	$V_6-(V_8 - V_9)$			13	V		
	$(V_8 + V_9)-V_7$			13	V		
Reference voltage [1]	V_5	2.8	3	3.2	V	$I_{ref} = 0$	
Stabilized voltage on pin 10 [2]	V_{10}	5.5	6	6.5	V	$V_S > 7.9$ V	
TC of reference voltage	αV_5		0.4		mV/K		
Sensitivity of reference voltage to supply-voltage variation	$\Delta V_5/\Delta V_S$		2		mV/V		
Output reverse current	I_{QH}			10	µA		
Output saturation voltage	V_{QL}		100	200	mV	$I_Q = 10$ mA	1
			500	800	mV	$I_Q = 50$ mA	
Hysteresis of window edges	$V_U - V_L$	18	22	35	mV		
Inhibit threshold	$V_{4, 12}$	1		1.8	V		
Inhibit current	$I_{4, 12}$		– 100		µA		
Switching frequency	f_{dir}		20		kHz		1
	f_{ind}		50		kHz		2

1) Range aimed at is 2.85 to 3.15 V
2) Range aimed at is 5.6 to 6.4 V



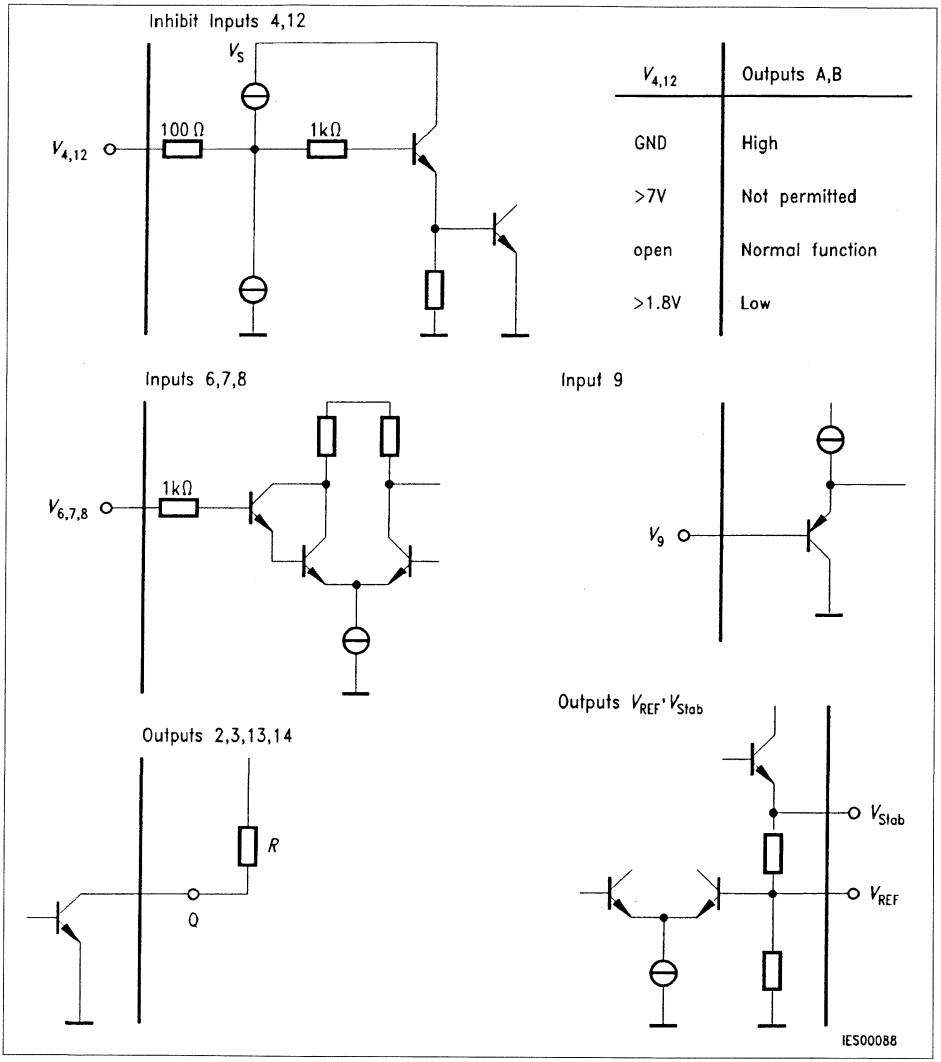
Test Circuit 1

Direct Setting of Window

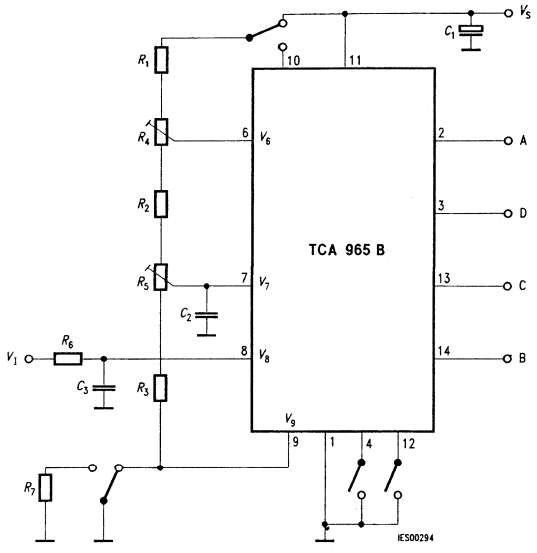


Test Circuit 2

Indirect Setting of Window by Center Voltage and Half Window Width



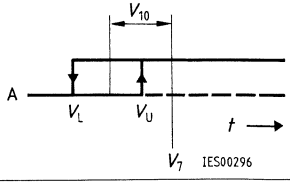
Schematic Circuit Diagrams



To increase the switching frequency, pin 9 may be grounded via R_7 (V_9 approx. 30...40mV).

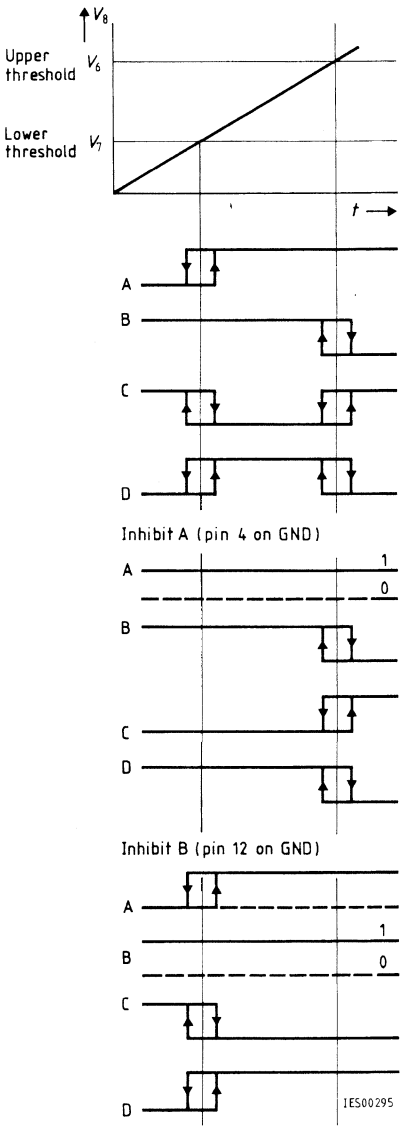
Application Circuit 1: Direct Setting of Lower and Upper Edge Voltages

$V_6 - V_9$ = Upper edge voltage
$V_7 + V_9$ = Lower edge voltage
V_8 = Input voltage

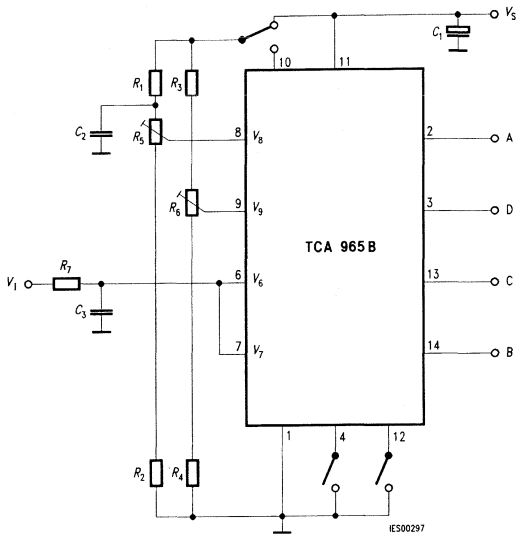


Definition of the Offset Voltage V_{IO}

$$V_{10} = \frac{V_L + V_U}{2} - V_7$$

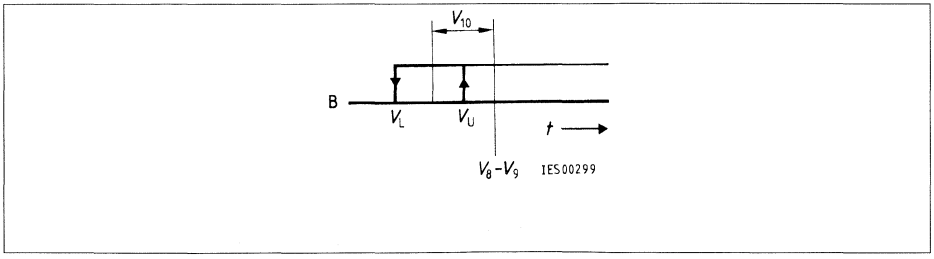


Application Circuit 1: Direct Setting of Lower and Upper Edge Voltages



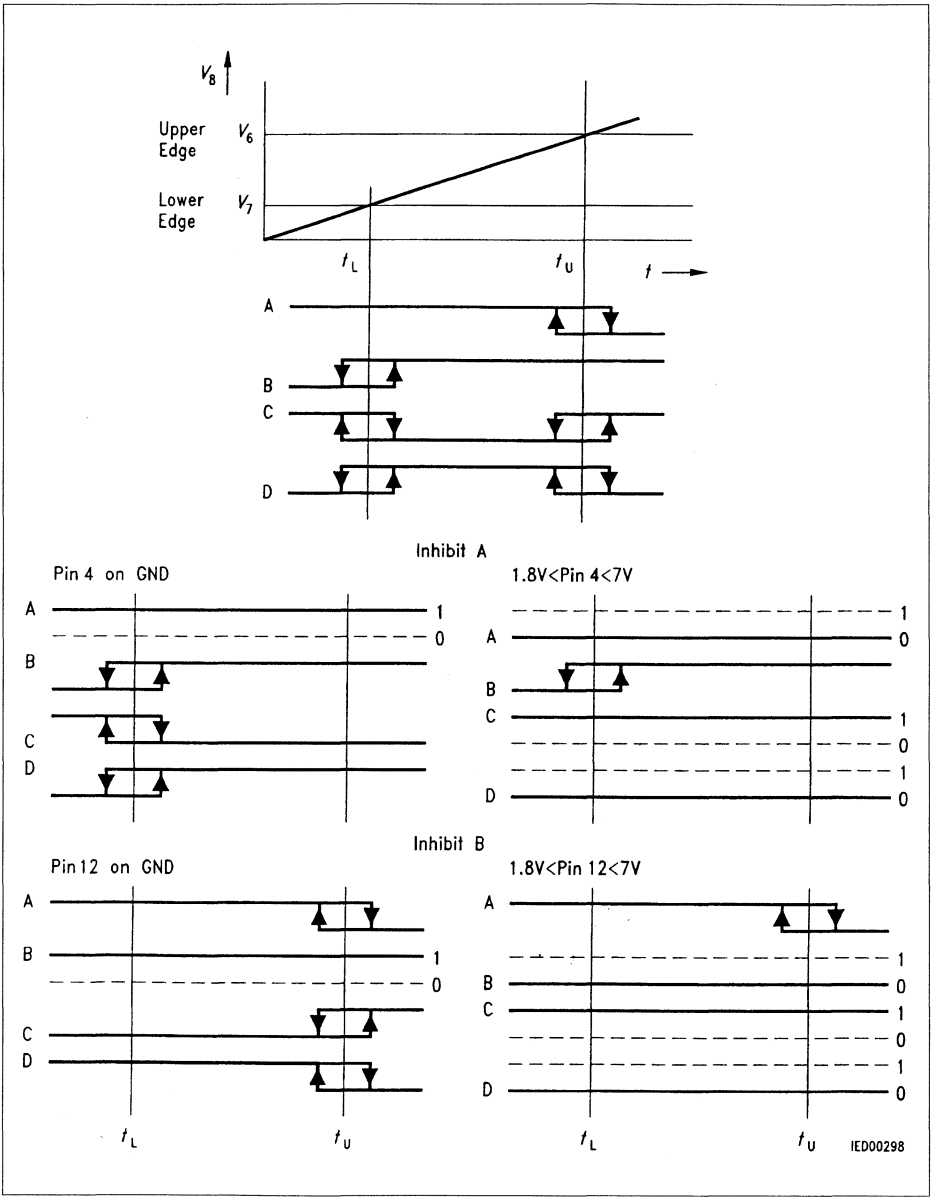
Application Circuit 2: Indirect Setting of Window by Center Voltage and Half-Window Width V

$V_6 = V_7$ = Input voltage
V_8 = Center voltage
V_9 = Half window width

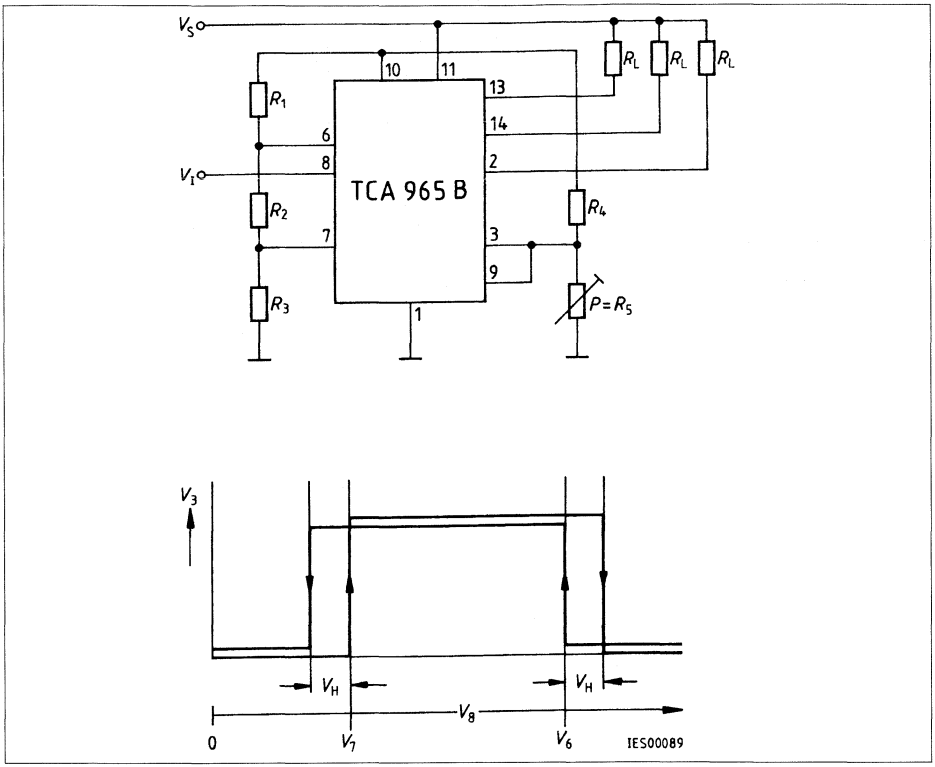


Definition of the Offset Voltage V_{IO}

$$V_{10} = \frac{V_L + V_U}{2} - (V_8 - V_9)$$



Application Circuit 2: Indirect Setting of Window by Center Voltage and Half-Window Width V



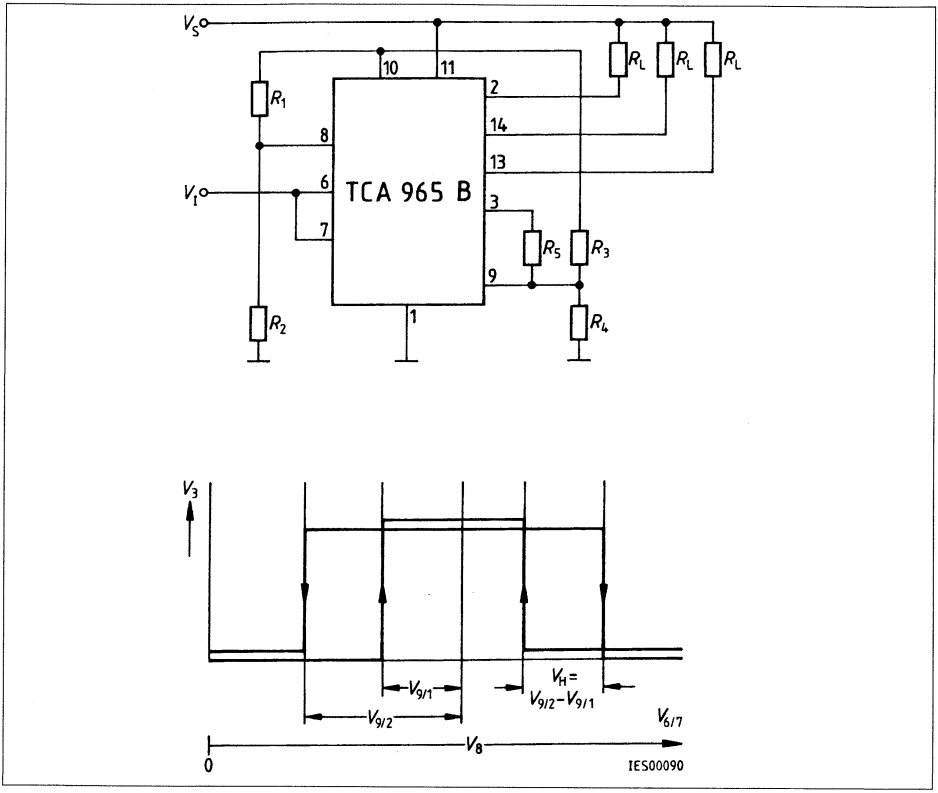
Application Circuit 3

Symmetrically Enlarged Edge Hysteresis in Direct Setting of Window

Calculation of hysteresis V_H

$$V_{11} = V_{10} \frac{R_5}{R_4 + R_5}$$

$$\frac{V_{10}}{R_4 + R_5} + \frac{V_{10}}{R_1 + R_2 + R_3} \leq 10 \text{ mA}$$



Application Circuit 4

Symmetrically Enlarged Edge Hysteresis in Indirect Setting of Window

Calculation of hysteresis V_H

$V_H = V_{9/2} - V_{9/1}$

$$V_{9/1} = V_{10} \frac{R_4 \parallel R_5}{R_3 + R_4 \parallel R_5}$$

$$V_{9/2} = V_{10} \frac{R_4}{R_3 + R_4}$$

Current-Monitoring IC

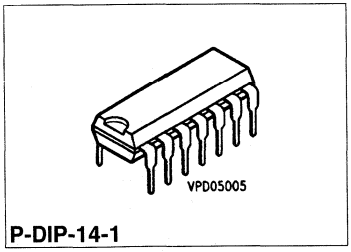
TLE 4951

Preliminary Data

Bipolar IC

Features

- Input currents max 25 µA, protective resistors can be connected in series
- Effective protection against destruction by excessive voltages such as load dump pulses occuring in cars
- Supply voltage range from 4.5 to 32 V
- Input voltage range up to 32 V, independent of supply voltage
- Switching threshold of comparators dependent on supply voltage, corresponding to the characteristic of light bulbs
- Temperature range: – 40 to 125 °C



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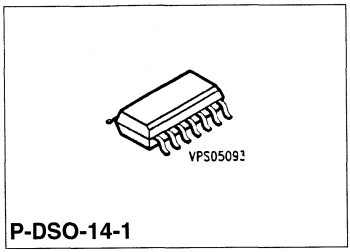


P-DSO-14-1

Applications

Current monitoring of
- light bulbs
- electric motors
- relays
- glow plugs
- circuits

especially suitable for:
- automotive electronics
- industrial plants

	Type	Ordering code	Package
S ■	TLE 4951	Q67000-A8266	P-DIP-14-1
S ■	TLE 4951 G	Q67000-A8267	P-DSO-14-1 (SMD)

■ Not for new design

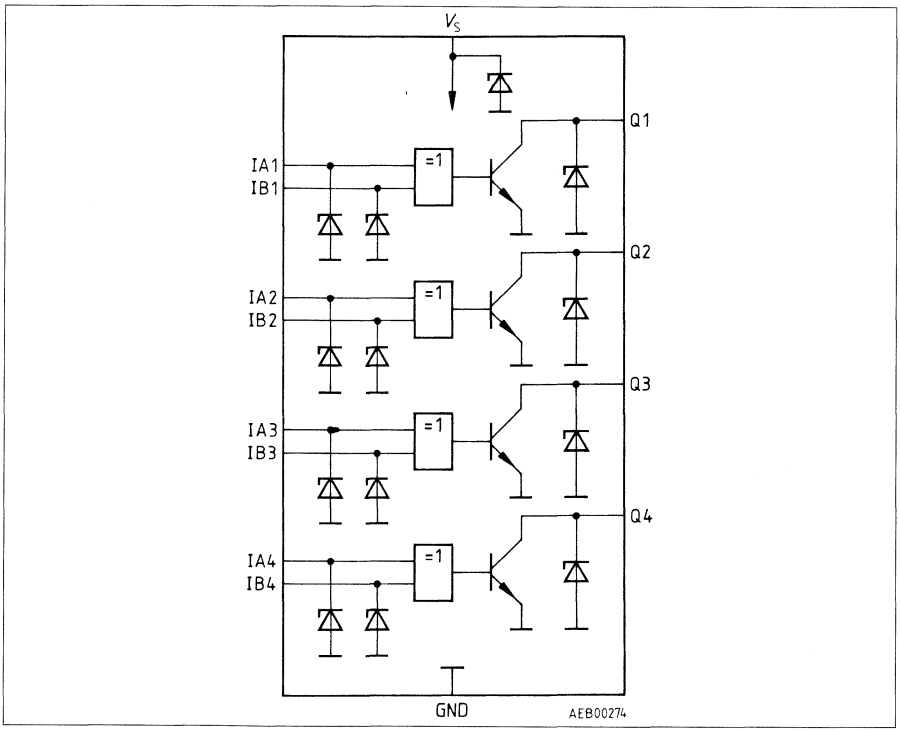
The TLE 4951 is designed to monitor the correct function of circuits, in particular those of light bulbs in cars. The IC comprises four identical comparator stages, the logic function of which corresponds to an exclusive-OR gate. With each comparator, pairs of lamps or single lamps can be monitored by means of the voltage drops across shunt resistors (R_{sh}) in the positive supply line (see **application circuits 1 and 2**).

Due to small differential input currents it is possible to connect protective resistors (R_s) in series. This provides a high degree of **protection against destruction** by interfering voltages occuring in automobiles.

Functional Description

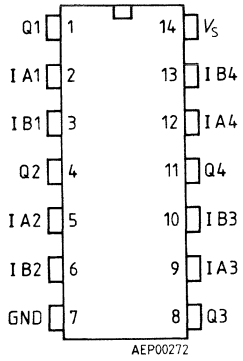
The component incorporates four identical comparator circuits. Each of these functional units has two equivalent inputs and one open-collector output Q. If the voltages differ by more than approx. 15 mV, the switching state changes from H (OFF-state) to L (ON-state).

For an input voltage < 4.5 V at both the inputs, the output can switch to H independently of the differential input voltage. For an input voltage < 2.0 V the output is reliably OFF-state.

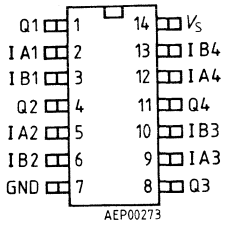


Block Diagram

TLE 4951



TLE 4951 G



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	Output 1
2	IA1	Input A1
3	IB1	Input B1
4	Q2	Output 2
5	IA2	Input A2
6	IB2	Input B2
7	0_S	GND
8	Q3	Output 3
9	IA3	Input A3
10	IB3	Input B3
11	Q4	Output 4
12	IA4	Input A4
13	IB4	Input B4
14	V_S	Supply voltage

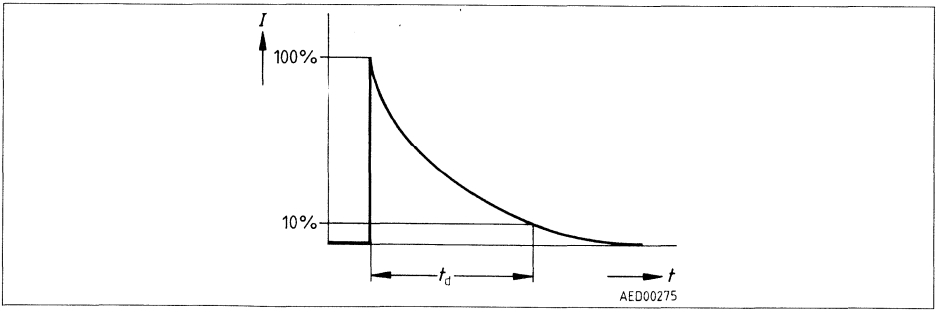
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.5	32	V	
Input voltages	$V_{A, B}$	– 45	45	V	
Output voltage	V_Q	– 0.5	32	V	
Output current	I_Q		40	mA	
Current through protecting structures					
at the supply terminal	I_S	– 600	600	mA	$t_d < 2$ ms
at the outputs Q	I_{SQ}	– 400	400	mA	$t_d < 2$ ms
Thermal resistance					
system - air TLE 4951	$R_{th\,SA}$		75	K/W	
system - air TLE 4951 G	$R_{th\,SA}$		125	K/W [1]	

[1] 75 K/W ceramic substrate

Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	4.5	32	V
Ambient temperature	T_A	– 40	125	°C
Common-mode input voltage range independent of V_S	V_{IC}	4.5	32	V
Differential input voltage	V_{ID}		100	mV



Permissible short-term overvoltages with series resistors R_S:

$+ V(V_{S;Q}) = I_{S;Q} \times R_V(V_{S;Q}) + 32$ V

$- V(V_{S;Q}) = - I_{S;Q} \times R_V(V_{S;Q})$

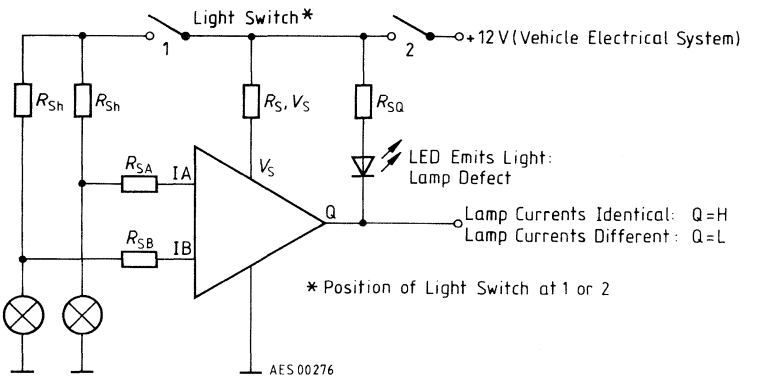
Characteristics

T_A = – 30 to 110 °C; V_S = 10 to 16 V

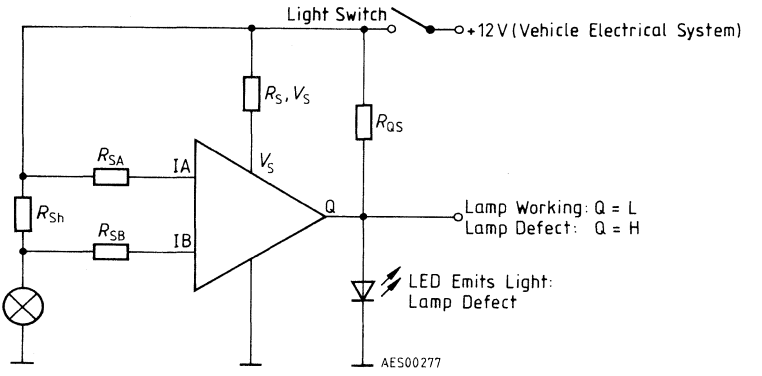
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max			
Current consumption	I_S			3 8	mA mA	Q1 = Q2 = Q3 = Q4 = H Q1 = Q2 = Q3 = Q4 = L	1
Switching threshold							
with $R_{SA, B}$	V_{Diff}[1]	7	14	20	mV	V_S = 13.5 V, R_S = 1 kΩ	2
without $R_{SA, B}$	V_{Diff}[1]	4	8	12	mV	V_S = 13.5 V	1
with $R_{SA, B}$	V_{Diff}	2		14	mV	4.5 V < V_S < 5.5 V, R_S = 1 kΩ	2
without $R_{SA, B}$	V_{Diff}	1.5		8	mV	4.5 V < V_S < 5.5 V	1
Input current	$I_{A, B}$			25	µA	$V_A = V_B$	1
Output saturation voltage	V_{QL}			0.4	V	I_Q = 30 mA	1
Output reverse current	I_{QH}			10		V_{QH} = 32 V	1

[1] $V_{Diff} = |V_A - V_B|$

1. Differential measurement

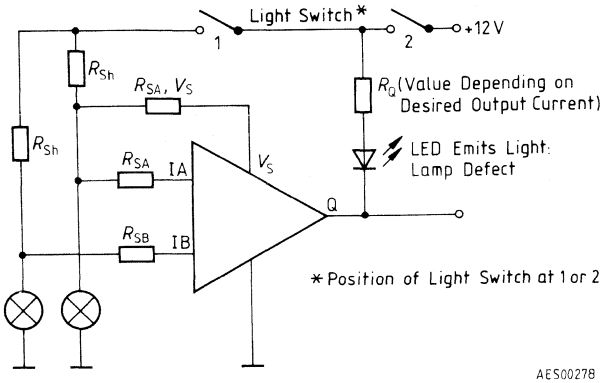


2. Absolute-value measurement



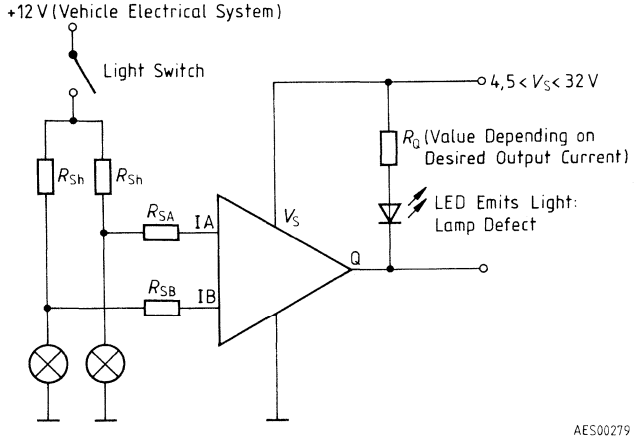
Application Circuits

3. Supply from shunt resistor (function as "1": Differential measurement)



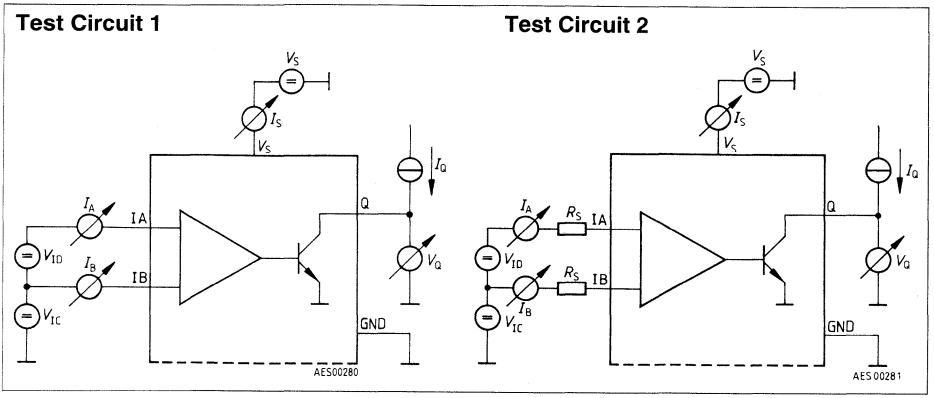
Recommended Protective Resistors: $R_{SA,B}$ = 1kΩ
R_{SA},V_S = 100Ω

4. Voltage supply separated from vehicle electrical system (function as "1": Differential measurement)



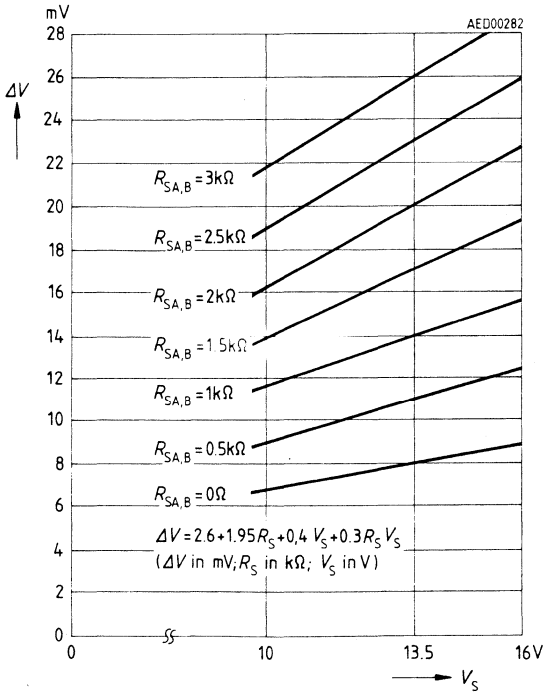
Recommended Protective Resistors: $R_{SA,B}$ = 1kΩ

Applications Circuits (cont'd)



Differential Switching Voltage versus Supply Voltage

Parameters: protective resistors at the inputs $R_{SA,B}$



Type	Package	Operating Range (V)	Temperature Range (°C)	Max. Frequency (kHz)	Undervoltage Shutdown
PWM Control					
TDA 4700	C-DIP-24	10.5 to 30	– 25 to 80	100	●
TDA 4700 A	P-DIP-24	10.5 to 30	0 to 70	100	●
TDA 4714 C	P-DIP-14-1	10.5 to 30	– 25 to 85	100	●
TDA 4716 C	P-DIP-16	10.5 to 30	– 25 to 85	100	●
TDA 4718	C-DIP-18	10.5 to 30	– 25 to 85	100	●
TDA 4718 A	P-DIP-18-1	10.5 to 30	0 to 70	100	●
TDA 4918 A	P-DIP-20-1	10 to 30	– 40 to 85	150	●
TDA 4918 G	P-DSO-20-1	10 to 30	– 40 to 85	150	●
TDA 4919 A	P-DIP-20-1	10 to 30	– 40 to 85	300	●
TDA 4919 G	P-DSO-20-1	10 to 30	– 40 to 85	300	●
Power Factor Controllers					
TDA 4814 A	P-DIP-14-1	11.2 to 17	– 25 to 85	–	●
TDA 4815	P-DIP-20-1	9 to 15	– 40 to 85	300	●
TDA 4815 G	P-DSO-20-1	9 to 15	– 40 to 85	300	●
TDA 4816 G	P-DSO-16-1	11.2 to 17	– 25 to 85	–	●
TDA 4817	P-DIP-8	11.2 to 17	– 25 to 85	–	●
TDA 4817 G	P-DSO-8-1	11.2 to 17	– 25 to 85	–	●
TDA 4818	P-DIP-20-1	9 to 15	– 40 to 85	–	●
TDA 4819	P-DIP-16	9 to 15	– 40 to 85	300	●
5-V Low-Drop Voltage Regulators					
TLE 4258	P-TO220-7-1	6 to 24	– 40 to 150 [1]	–	–
TLE 4260	P-TO220-5-1	6 to 32	– 40 to 150 [1]	–	–
TLE 4260 S	P-TO220-5-2	6 to 32	– 40 to 150 [1]	–	–
TLE 4261	P-TO220-7-1	6 to 32	– 40 to 150 [1]	–	–
TLE 4261 S	P-TO220-7-2	6 to 32	– 40 to 150 [1]	–	–
TLE 4261 G	P-DSO-20-1	6 to 32	– 40 to 150 [1]	–	–
TLE 4262 G	P-DSO-20-1	6 to 32	– 40 to 150 [1]	–	–
TLE 4263 G	P-DSO-20-1	6 to 32	– 40 to 150 [1]	–	–

= SMD

1) T_j = Junction temperature
2) Standby current

Reset Signal	Supply Current (mA) typ.	Driver Outputs	Maximum Output Current (mA)	Standby	Current Limitation	Page
–	12	2	70	–	●	109
–	12	2	70	–	●	109
–	12	2	70	–	●	124
–	12	2	70	–	●	124
–	12	2	70	–	●	109
–	12	2	70	–	●	109
–	12	2	+ 700 – 500	●	●	139
–	12	2	+ 700 – 500	●	●	139
–	12	1	+ 700 – 500	●	●	139
–	12	1	+ 700 – 500	●	●	139
–	5	1	400	●	–	160
–	5	1	500	●	●	174
–	5	1	500	●	●	174
–	5	1	400	●	–	160
–	5	1	400	●	–	193
–	5	1	400	●	–	193
–	5	1	500	●	●	174
–	5	1	500	●	●	174
●	2 [2]	2	750	●	●	205
●	500 µA [2]	1	500	●	●	215
●	500 µA [2]	1	500	●	●	215
●	50 µA [2]	1	500	●	●	225
●	50 µA [2]	1	500	●	●	225
●	50 µA [2]	1	500	●	●	225
●	50 µA	1	200	●	●	238
●	50 µA	1	200	●	●	249

Control ICs for Single-Ended and Push-Pull Switched-Mode Power Supplies (SPMS)

The TDA 47xx family of control ICs for SMPS consists of four basic types that, in line with the particular application, will enable optimal adaptation to the SMPS concept that is called for. These devices include all the important basic functions that are expected of a modern SPMS, such as feed-forward control, soft start, dynamic current limitation, error comparators, reference-voltage source, undervoltage shut-down and push-pull open-collector outputs.

The 4714 C is the most economic version. TDA 4700 A is the version with the widest range of functions.

The following table gives an overview over the four basic types.

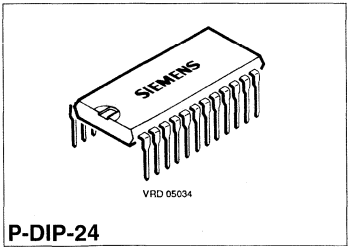
Features	TDA 4700	TDA 4718	TDA 4716	TDA 4714
Undervoltage Protection	●	●	–	–
External Synchronization	●	●	–	–
On-Chip General Purpose OP AMP	●	–	●	–
Overvoltage Protection with Lock-up Option	●	●	●	●
Symmetric Inputs	●	–	–	–
Dynamic Current Limiting	●	●	●	●
Feed-Forward Control	●	●	●	●
Double Pulse Suppression	●	●	●	●
Soft Start	●	●	●	●
V_S Undervoltage Protection	●	●	●	●

Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies (SMPS)

TDA 4700
TDA 4718

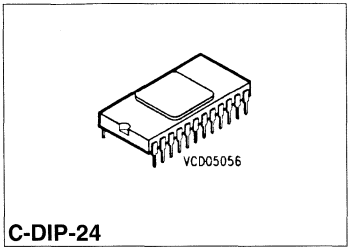
Features

- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter (TDA 4700)
- Push-pull outputs
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression



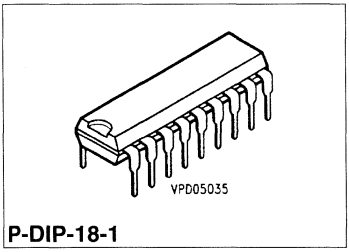
P-DIP-24

Type	Ordering Code	Package	Temp.-Range
TDA 4700	Q67000-Y595	C-DIP-24	– 25 to 85 °C
S TDA 4700 A	Q67000-Y594	P-DIP-24	– 0 to 70 °C
S TDA 4718	Q67000-Y638	C-DIP-18	– 25 to 85 °C
S TDA 4718 A	Q67000-Y639	P-DIP-18-1	– 0 to 70 °C

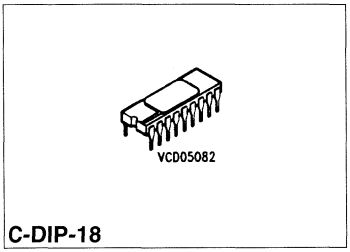


C-DIP-24

These versatile SMPS control ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers, which activate protective functions.

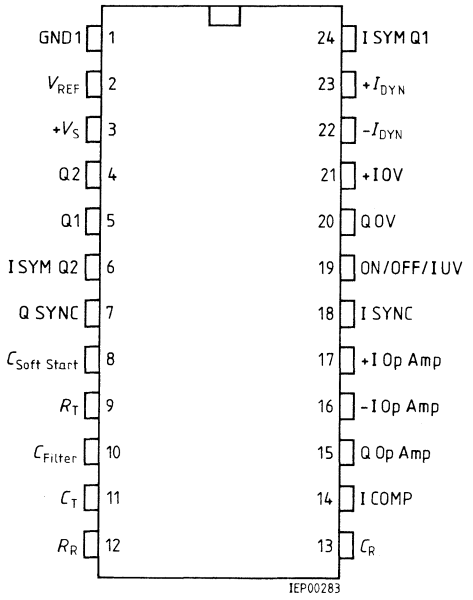


P-DIP-18-1



C-DIP-18

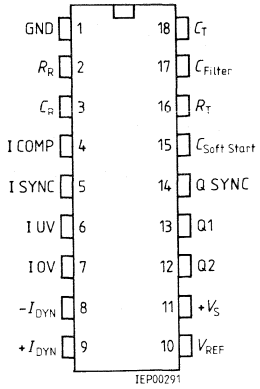
Pin Configuration (TDA 4700)
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2	+ V_{REF}	Reference voltage
3	+ V_S	Supply voltage
4	Q2	Output Q2
5	Q1	Output Q1
6	I SYM Q2	Symmetry Q2
7	Q SYNC	Sync. output
8	$C_{soft\ start}$	Soft start
9	R_T	VCO R_T
10	C_{filter}	Capacitance
11	C_T	VCO C_T
12	R_R	Ramp generator R_R
13	C_R	Ramp generator C_R
14	I COMP	Comparator input
15	Q Op Amp	Operational amplifier output
16	– I Op Amp	Operational amplifier input (–)
17	+ I Op Amp	Operational amplifier input (+)
18	I SYNC	Sync. input
19	ON/OFF/IUV	ON/OFF, undervoltage
20	QOV	Overvoltage output
21	IOV	Overvoltage input
22	– I_{DYN}	Dynamic current limitation (–)
23	+ I_{DYN}	Dynamic current limitation (+)
24	I SYM Q1	Symmetry

Pin Configuration (TDA 4718)
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground 0 V
2	R_R	Ramp generator RR
3	C_R	Ramp generator CR
4	ICOMP	+ Input comparator K2
5	ISYNC	Sync. input
6	IUV	Input undervoltage, ON/OFF
7	IOV	Input overvoltage
8	$-I_{DYN}$	Input dynamic current limitation (-)
9	$+I_{DYN}$	Input dynamic current limitation (+)
10	V_{REF}	Reference voltage
11	$+V_S$	Supply voltage
12	Q 2	Output Q2
13	Q 1	Output Q1
14	Q SYNC	Sync. output
15	$C_{soft\ start}$	Soft start
16	R_T	VCO R_T
17	C_{filter}	Capacitance
18	C_T	VCO C_T

4

Circuit Description

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Phase Comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. The component can be frequency-synchronized, but not phase-synchronized, with the sync input. The duty cycle of the squarewave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active outputs is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1 (TDA 4700; A)

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and + 5 V.

Pulse-Turn-OFF Flipflop

The pulse turn-OFF flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{soft\ start}$ (and also at K2) to a maximum of + 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals which are routed to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, cause the component to switch on again by the soft start.

Comparator K5, K6, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

The K7 common-mode range covers 0 V to + 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry (TDA 4700; A)

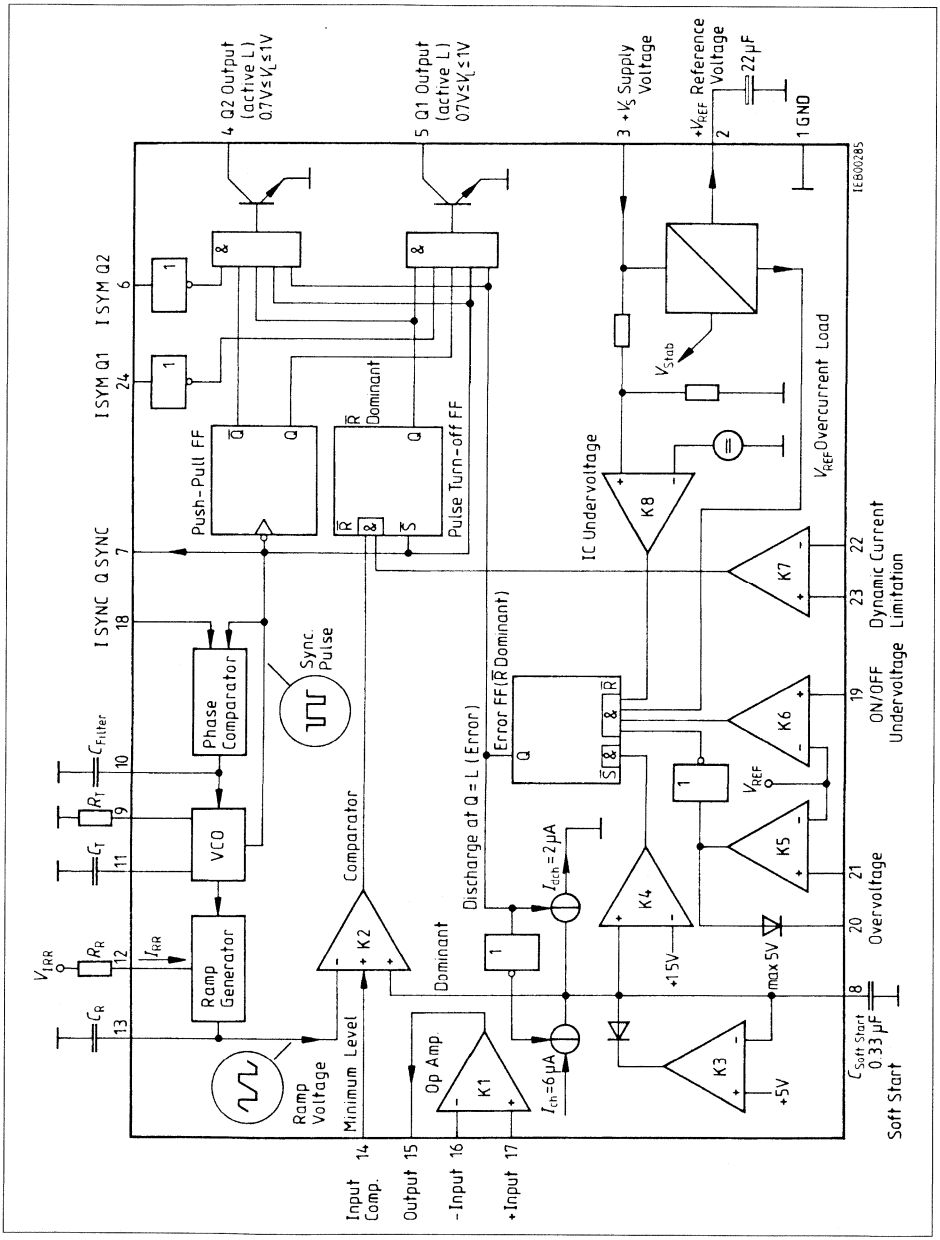
In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

Outputs

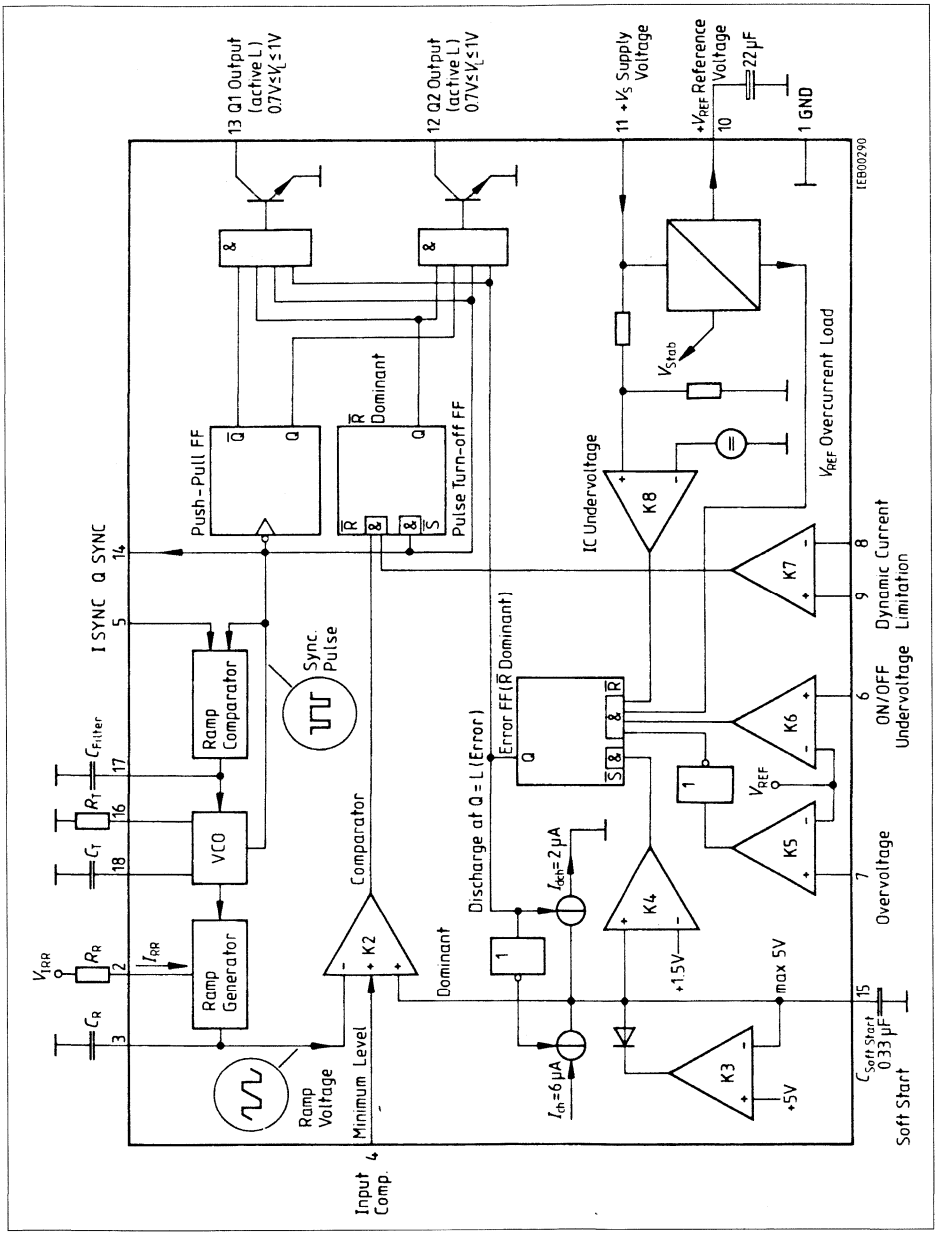
Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.



Block Diagram (TDA 4700)



Block Diagram (TDA 4718)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Condition
Supply voltage	V_S	– 0.3	33	V	
Voltage at Q1, Q2	V_Q	– 0.3	33	V	Q1, Q2 high
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 low
Symmetry 1, 2 TDA 4700; A	V_{SYM}	– 0.3	33	V	
Sync output	$V_{SYNC\ Q}$	– 0.3	7	V	SYNC Q high
	$I_{SYNC\ Q}$	0	10	mA	SYNC Q low
Sync input	$V_{SYNC\ I}$	– 0.3	33	V	
Input C_{filter}	$V_{I\ Cf}$	– 0.3	7	V	
Input R_T	$V_{I\ RT}$	– 0.3	7	V	
Input C_T	$V_{I\ CT}$	– 0.3	7	V	
Input R_R	$V_{I\ RR}$	– 0.3	7	V	
Input C_R	$I_{I\ CR}$	– 10	10	mA	
Input comparator K2, K5, K6, K7	$V_{I\ K}$	– 0.3	33	V	
Output K5	$V_{Q\ K5}$	– 0.3	33	V	
Input op amp TDA 4700; A	$V_{I\ Op\ Amp}$	– 0.3	33	V	
Output op amp TDA 4700; A	$V_{Q\ Op\ Amp}$	– 0.3	V_S - 1 max. 7	V V	
Reference voltage	V_{REF}	– 0.3	V_{REF}	V	
Input $C_{soft\ start}$	$V_{I\ soft\ start}$	– 0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance system – air TDA 4700; A	$R_{th\ SA}$		65	K/W	
TDA 4718	$R_{th\ SA}$		70	K/W	
TDA 4718 A	$R_{th\ SA}$		60	K/W	

Operating Range

Supply voltage	V_S	10.5	30	V	
Ambient temperature TDA 4700 TDA 4718 TDA 4700 A TDA 4718 A	T_A T_A	– 25 0	85 70	°C °C	
VCO frequency	f	40	250000	Hz	
Ramp generator frequency	f_{RG}	40	250000	Hz	

Characteristics

V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
Supply current	I_S	8		20	mA	C_T = 1 nF, f_{VCO} = 100 kHz
Reference						
Reference voltage	V_{REF}	2.35	2.5	2.65	V	0 mA < I_{REF} < 5 mA
Reference voltage change	ΔV_{REF}		8		mV	14 V ± 20 %
Reference voltage change	ΔV_{REF}		15		mV	25 V ± 20 %
Reference voltage change	ΔV_{REF}			15 [1]	mV	0 mA < I_{REF} < 5 mA
Temperature coefficient	TC		0.25	0.4	mV/K	
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA	
Oscillator (VCO)						
Frequency range	f_{VCO}	40		100000	Hz	
Frequency change	$\Delta f/f_{VCO}$		0.5		%	14 V ± 20 %
Frequency change	$\Delta f/f_{VCO}$	– 1		1	%	25 V ± 20 %
Tolerance	$\Delta f/f_{VCO}$	– 7		7	%	ΔR_T = 0, ΔC_T = 0
Fall time sawtooth	t		1		µs	C_T = 1 nF
	t		10		µs	C_T = 10 nF
RC combination	C_T	0.82		47	nF	
VCO	R_T	5		700	kΩ	
Ramp Generator						
Frequency range	f	40		100000	Hz	
Maximum voltage at C_R	V_H		5.5		V	
Minimum voltage at C_R	V_L		1.8		V	
Input current through R_R	I_{RR}	0		400	µA	
Current transformation ratio	I_{RR}/I_{CR}		1/4			
Synchronization						
Sync output	V_{QH}	4			V	I_{QH} = - 200 µA
	V_{QL}			0.4	V	I_{QL} = 1.6mA
Sync input	V_{IH}	2			V	
	V_{IL}			0.8	V	
Input current	$-I_I$			5	µA	

[1] At T_A = 0 to 70 °C, this value falls to max. 5 mV.

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
Comparator K2						
Input current	$-I_{IK2}$			2	µA	
Turn-off delay[1]	$t_{D\,OFF}$			500	ns	
Input voltage	V_{IK2}					for duty cycle
			1.8		V	D = 0
			5		V	D = max.
Common-mode input						
	V_{IC}	0		5.5	V	
Soft Start K3, K4						
Charge current for $C_{soft\ start}$	I_{ch}		6		µA	
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA	
Upper limiting voltage	V_{lim}		5		V	
Switching voltage K4	V_{K4}		1.5		V	
Operational Amplifier K1 (TDA 4700; TDA 4700 A)						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	– 10		10	mV	
Temperature coefficient of V_{IO}	TC	– 30		30	µV/K	
Input current	$-I_I$			2	µA	
Common-mode input voltage range	V_{IC}	0		5	V	
Output current	I_Q	– 3		1.5	mA	
Rise time of output voltage	$\Delta V/\Delta t$		1		V/µs	
Transition frequency	f_T		3		MHz	
Phase at f_T	φ_T		120		deg.	
Output voltage	$V_{Q\,H/L}$	1.5		5.5	V	–3 mA < I < 1.5 mA
Symmetry (TDA 4700; TDA 4700 A)						
Input voltage	V_{IH}	2.0			V	
	V_{IL}			0.8	V	
Input current	$-I_I$			2	µA	

[1] At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
Output Stages Q1, Q2						
Output voltage	V_{QH}			30	V	
	V_{QL}			1.1	V	I_Q = 20 mA
Output leakage current	I_Q			2	µA	V_{QH} = 30 V
ON, OFF, Undervoltage K6						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [1]	$t_{D\,OFF}$		250		ns	
Error detection time [1]	t		50		ns	
Dynamic Current Limitation K7						
Common-mode input voltage range	V_{IC}	0		4	V	
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Turn-OFF delay time [2]	$t_{D\,OFF}$		250		ns	
Error detection time [2]	t		50		ns	
Overvoltage K5						
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V	
Input current	$-I_I$			2	µA	
Output current	$-I_Q$	0		200	µA	$V_{QH\,min}$ = 5 V
Turn-OFF delay time [1]	$t_{D\,OFF}$		250		ns	
Error detection time [1]	t		50		ns	
Supply Undervoltage						
Turn-ON threshold for V_S rising	V_S	8.8		11	V	0 °C<T_A<70 °C
				10.5	V	
Turn-OFF threshold for V_S falling	V_S	8.5		10.5	V	0 °C<T_A<70 °C
				10	V	

[1] At the input: step function $\Delta V = V_{REF} - 100$ mV ⌐→ $V_{REF} + 100$ mV

[2] At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

Characteristics (cont'd)
V_S = 11 to 30 V; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
Input C_{filter}						
Rated voltage for rated frequency	V_R		4		V	
Frequency approx. proportional to voltage within the range	V_R	3		5	V	
Voltage at open sync input	$V_{c\ filter}$		1.6		V	

Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled

   → selection of C_T; selection of $C_R \leq C_T$

2. Determination of the VCO frequency = 2 × output frequency

   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on

   → selection of R_R.

4. Duration of the soft start process

   → selection of $C_{soft\ start}$.

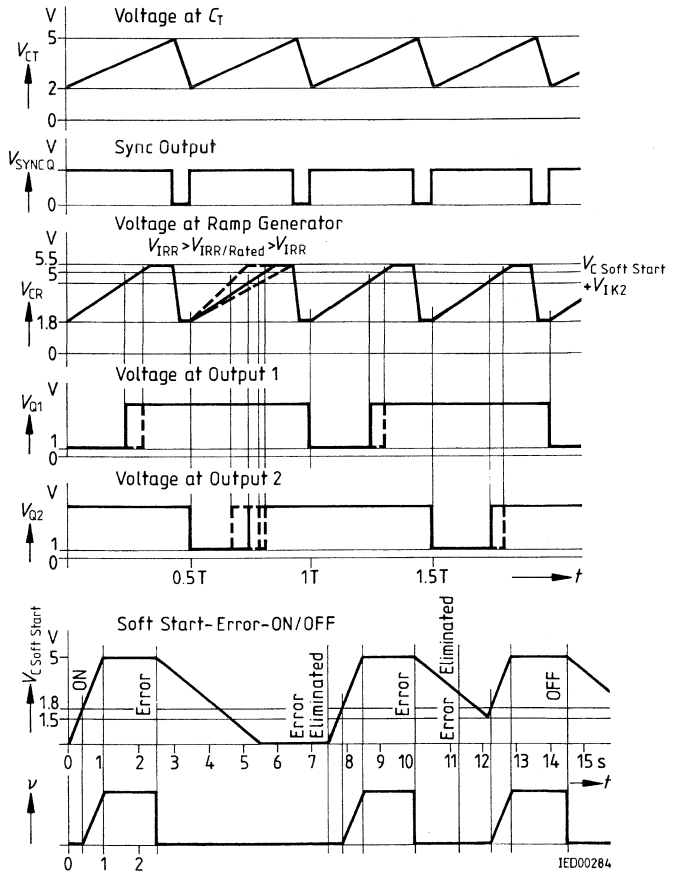
5. In the case of a free-running VCO: connect sync output with sync input.

6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2. (TDA 4700; TDA 4700 A)

7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

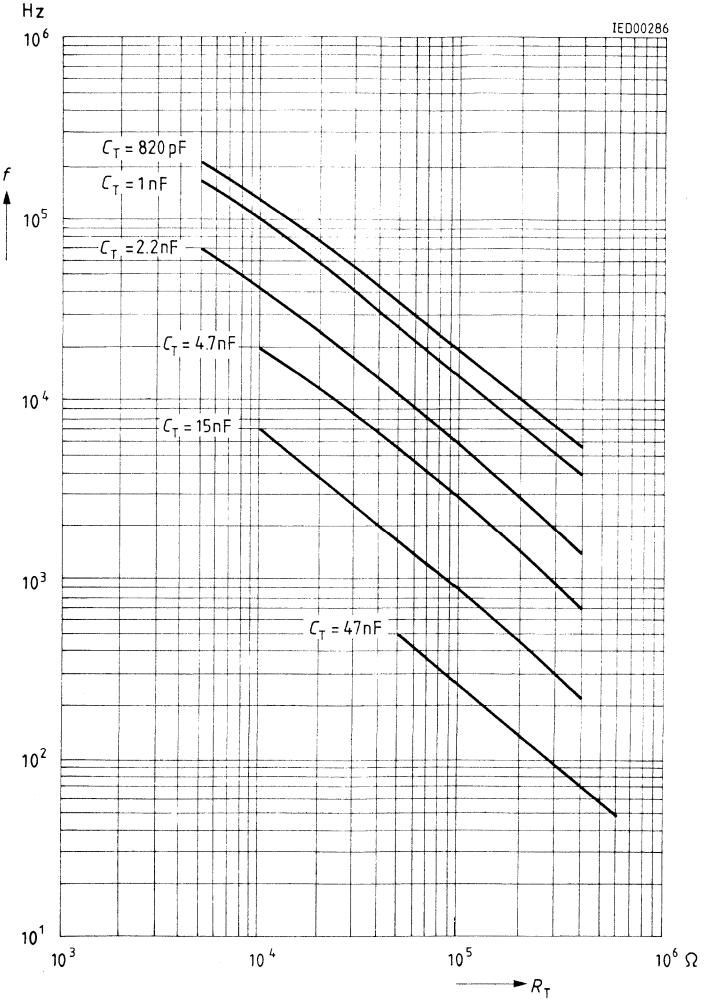
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF



Pulse Diagram

VCO Frequency versus R_T and C_T



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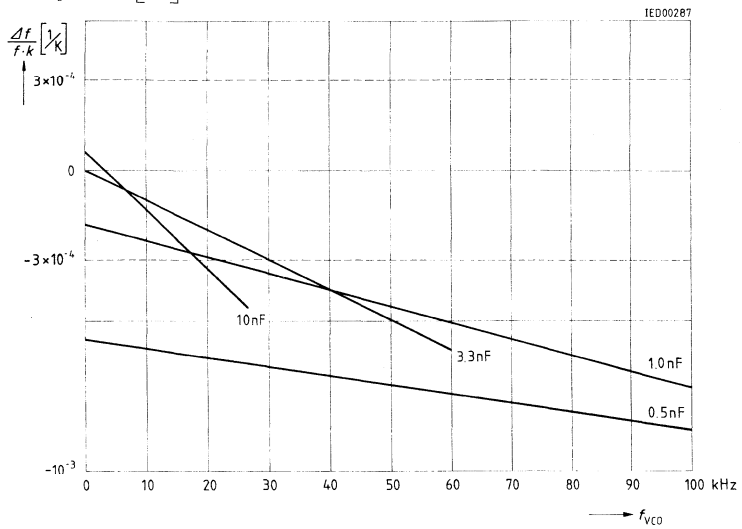
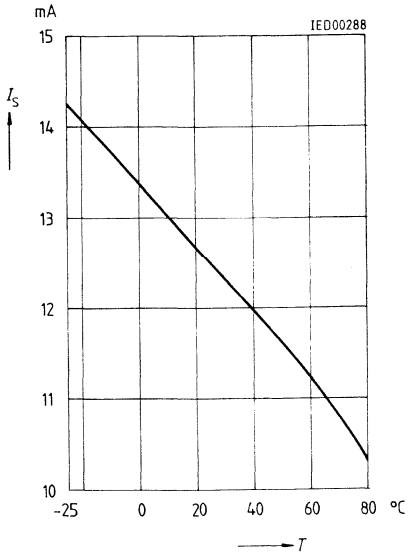
VCO Temperature Response

V_S = 12 V; D = max.

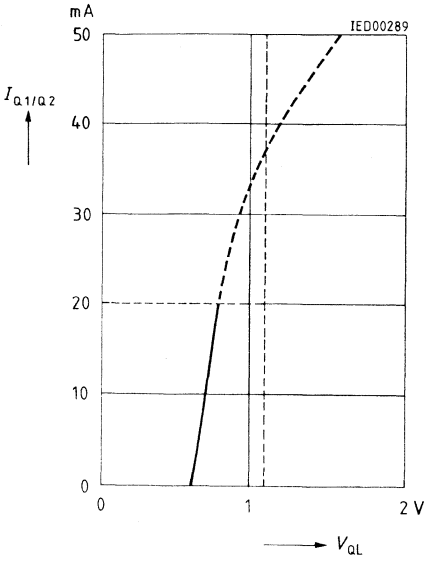
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current Consumption versus Temperature



Output Current versus Output Voltage



SIEMENS

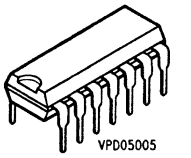
IC for Switched-Mode Power Supplies (SMPS)

TDA 4714 C
TDA 4716 C

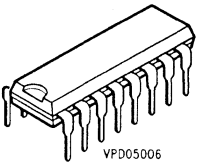
Bipolar IC

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source
- Reference overload protection
- Soft start
- Feed-forward control
- Operational amplifier (TDA 4716 C)



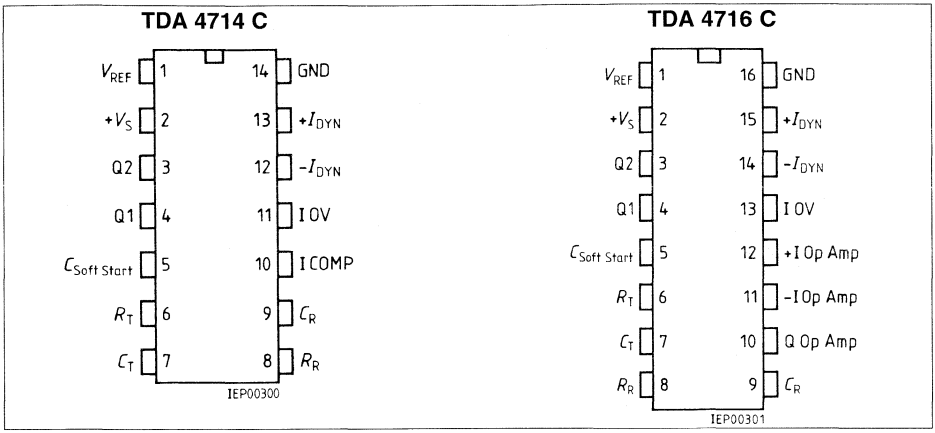
P-DIP-14-1



P-DIP-16

Type	Ordering Code	Package
▼ S TDA 4714 C	Q67000-A8312	P-DIP-14-1
▼ S TDA 4716 C	Q67000-A8313	P-DIP-16

These versatile SMPS ICs comprise digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The components can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps which activate protective functions.



Pin Configuration
(top view)

Pin Definitions and Functions (TDA 4714 C)

Pin	Symbol	Function
1	V_{REF}	Reference voltage
2	+ V_S	Supply voltage
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	I COMP	Input comparator
11	I OV	Input overvoltage
12	– I_{DYN}	Dynamic current limitation (–)
13	+ I_{DYN}	Dynamic current limitation (+)
14	GND	Ground

Pin Definitions and Functions (TDA 4716 C)

Pin	Symbol	Function
1	V_{REF}	Reference voltage V_{REF}
2	V_S	Supply voltage V_S
3	Q2	Output Q2
4	Q1	Output Q1
5	$C_{soft\ start}$	Soft start
6	R_T	VCO R_T
7	C_T	VCO C_T
8	R_R	Ramp generator R_R
9	C_R	Ramp generator C_R
10	Q op amp	Operational amplifier output
11	– I op amp	Operational amplifier input (–)
12	+ I op amp	Operational amplifier input (+)
13	I OV	Input overvoltage
14	– I_{DYN}	Dynamic current limitation (–)
15	+ I_{DYN}	Dynamic current limitation (+)
16	GND	Ground

Circuit Description

The following is a description of the individual functional units and their interaction.

Voltage Controlled Oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp Generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a DC voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-Pull Flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-OFF flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier K1 (TDA 4716 C)

The op amp K1 is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free positive input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and + 5 V.

Pulse Turn-OFF Flipflop

The pulse turn-OFF flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage of capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of + 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft Start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA at the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again by the soft start.

Comparator K5, K8, V_{REF} Overcurrent Load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again by the soft start.

Comparator K7

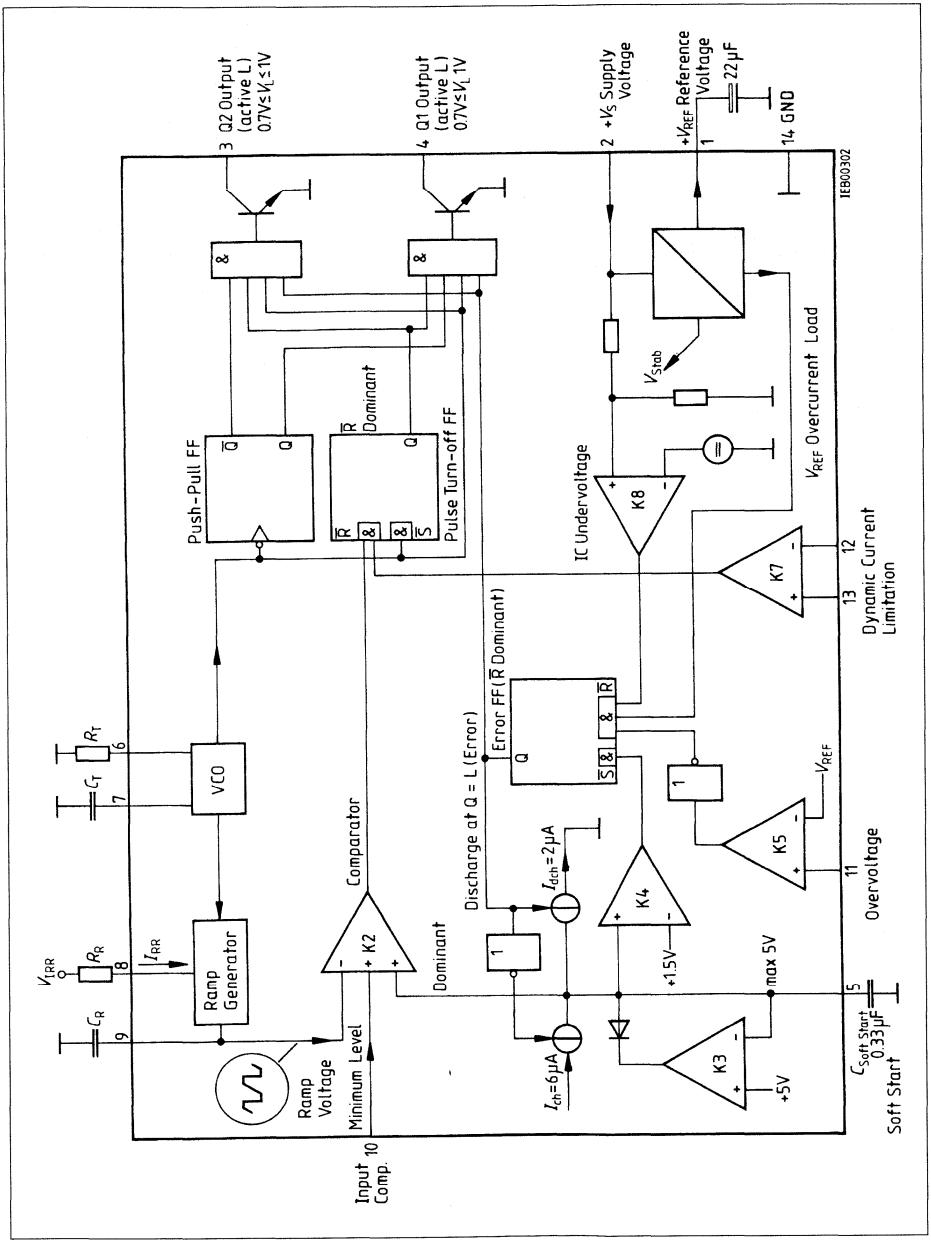
K7 serves to recognize overcurrents. This is the reason why both inputs of the operational amplifier have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and + 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

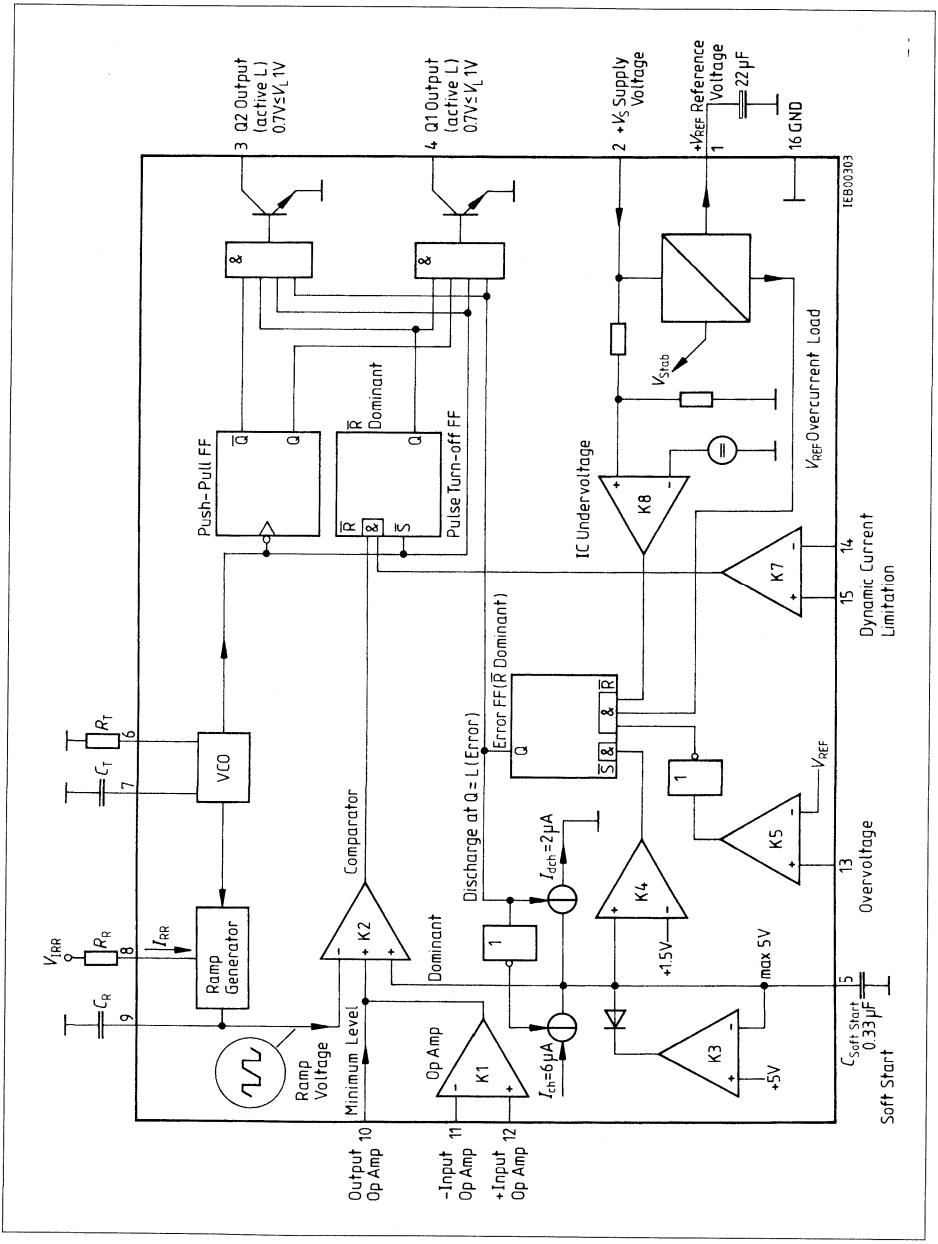
Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference Voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.



Block Diagram (TDA 4714 C)



Block Diagram (TDA 4716 C)

4

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Supply voltage	V_S	– 0.3	33	V	
Voltage at Q1, Q2	V_Q	– 0.3	33	V	Q1, Q2 high
Current at Q1, Q2	I_Q		70	mA	Q1, Q2 low
Input R_T	$V_{I\,RT}$	– 0.3	7	V	
Input C_T	$V_{I\,CT}$	– 0.3	7	V	
Input R_R	$V_{I\,RR}$	– 0.3	7	V	
Input C_R	$I_{I\,CR}$	– 10	10	mA	
Input comparator K2, K5, K7	$V_{I\,K2,\,5,\,7}$	– 0.3	33	V	
Output K5	$V_{Q\,K5}$	– 0.3	33	V	
Input op amp TDA 4716 C	$V_{I\,Op\,Amp}$	– 0.3	33	V	
Output op amp TDA 4716 C	$V_{Q\,Op\,Amp}$	– 0.3	$V_S - 1$ max. 7 V	V	
Reference voltage	$V_{Q\,REF}$	– 0.3	V_{REF}	V	
Input $C_{soft\,start}$	$V_{I\,soft\,start}$	– 0.3	7	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 55	125	°C	
Thermal resistance system - air	$R_{th\,SA}$		70	K/W	

Operating Range

Supply voltage	V_S	10.5	30	V	
Ambient temperature	T_A	– 25	85	°C	
Frequency	f	40	100	kHz	
VCO frequency	f_{VCO}	40	250	kHz	
Ramp generator frequency	f_{RG}	40	250	kHz	

Characteristics

$11\,V < V_S < 30\,V$; $-\ 25\,°C < T_A < 85\,°C$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current $C_T = 1\,nF$ $f_{VCO} = 100\,kHz$	I_S	8		20	mA
Reference					
Reference voltage, $T_A = 25\,°C$ $I_{REF} = 1\,mA$, $V_S = 12\,V$	V_{REF}	2.475	2.500	2.525	V
Voltage change $V_S = 14\,V \pm 20\%$	ΔV_{REF}		8		mV
Voltage change $V_S = 25\,V \pm 20\%$	ΔV_{REF}		15		mV
Voltage change [1] $0\,mA < I_{REF} < 5\,mA$	ΔV_{REF}			15	mV
Temperature coefficient	TC		0.25	0.4	mV/K
Response threshold of I_{REF} overcurrent	I_{REF}		10		mA
Oscillator (VCO)					
Frequency range	f	40		100	kHz
Frequency change $V_S = 14\,V \pm 20\%$	$\Delta f/f$		0.5		%
Frequency change $V_S = 25\,V \pm 20\%$	$\Delta f/f$	− 1		1	%
Tolerance $\Delta R_T = 0$; $\Delta C_T = 0$	$\Delta f/f$	− 7		7	%
Fall time sawtooth					
$C_T = 1\,nF$			1		µs
$C_T = 10\,nF$			10		µs
RC combination	C_T	0.82		47	nF
VCO	R_T	5		700	kΩ
Ramp Generator					
Frequency range	f_{RG}	40		100	kHz
Maximum voltage at C_R	V_H		5.5		V
Minimum voltage at C_R	V_L		1.8		V
Input current through R_R	I_{RR}	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4		

[1] Between 0 °C and 70 °C ambient temp. ΔV_{REF} is reduced to max. 5 mV.

Characteristics (cont'd)
11 V < V_S < 30 V; – 25 °C < T_A < 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Comparator K2					
Input current	$-I_{K2}$			2	µA
Turn-OFF delay time [1]	$t_{D\,OFF}$			500	ns
Input voltage	$V_{I\,K2}$				
Duty cycle $D = 0$			1.8		V
D = max			5		V
Common-mode input voltage range	V_{IC}	0		5.5	V
Soft Start K3, K4					
Charge current for $C_{soft\ start}$	I_{ch}		6		µA
Discharge current for $C_{soft\ start}$	I_{dch}		2		µA
Upper limiting voltage	V_{lim}		5		V
Switching voltage K4	V_{K4}		1.5		V
Operational Amplifier (TDA 4716 C)					
Open-loop voltage gain	G_{V0}	60	80		dB
Input offset voltage	V_{IO}	– 10		10	mV
Temperature coefficient of V_{IO}	TC	– 30		30	µV/K
Input current	$-I_I$			2	µA
Common-mode input voltage range	V_{IC}	0		5	V
Output current	I_Q	– 3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$		1		V/µs
Transition frequency	f_T		3		MHz
Phase at f_T	φ_T		120		degr.
Output voltage – 3 mA < I < 1.5 mA	$V_{Q\,H/L}$	1.5		5.5	V
Output Stages Q1, Q2					
Output voltage I_Q = 20 mA	V_{QH} V_{QL}			30 1.1	V V
Output leakage current V_{QH} = 30 V	I_Q			2	µA

[1] At the input: step function $\Delta V = -$ 100 mV ⌐▸ $\Delta V = +$ 100 mV

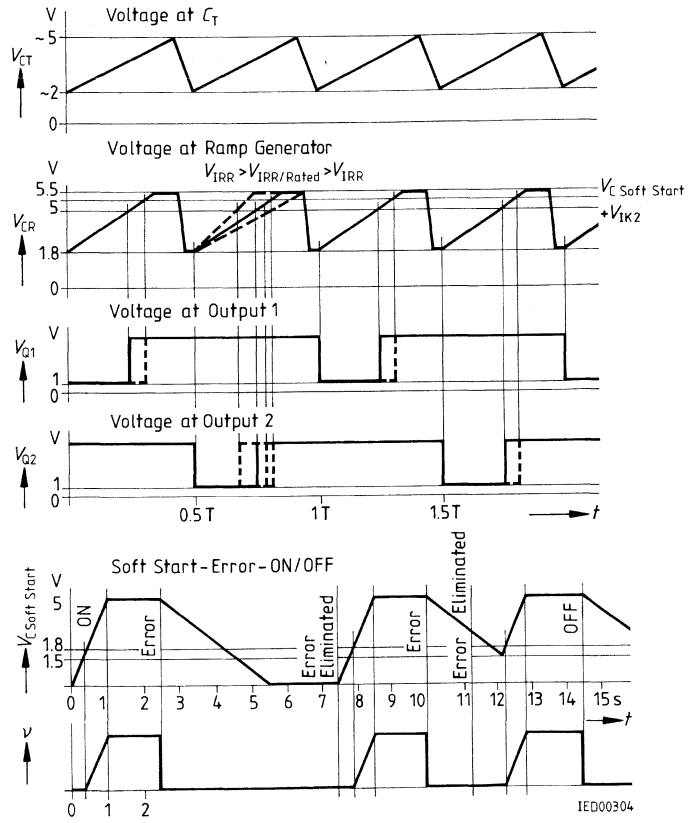
Characteristics (cont'd)
11 V < V_S < 30 V; – 25 °C < T_A < 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Dynamic Current Limitation K7					
Common-mode input voltage range	V_{IC}	0		4	V
Input offset voltage	V_{IO}	– 10		10	mV
Input current	$-I_I$			2	µA
Turn-OFF delay time[2]	$t_{D\,OFF}$		250		ns
Error detection time[2]	t		50		ns
Overvoltage K5					
Switching voltage	V	V_{REF} – 0.03		V_{REF} + 0.03	V
Input current	$-I_I$			2	µA
Turn-OFF delay time[1]	$t_{D\,OFF}$		250		ns
Error detection time[1]	t		50		ns
Supply Undervoltage					
Turn-ON threshold for V_S, rising	V_S	8.8		11	V
Turn-ON threshold for V_S, rising (0 °C < T_A < 70 °C)	V_S			10.5	V
Turn-OFF threshold for V_S, falling	V_S	8.5		10.5	V
Turn-ON threshold for V_S, falling (0 °C < T_A < 70 °C)	V_S			10	V

1) At the input: step function V_{REF} = – 100 mV ⌐→ V_{REF} = + 100 mV
2) At the input: step function ΔV = – 100 mV ⌐→ ΔV = + 100 mV

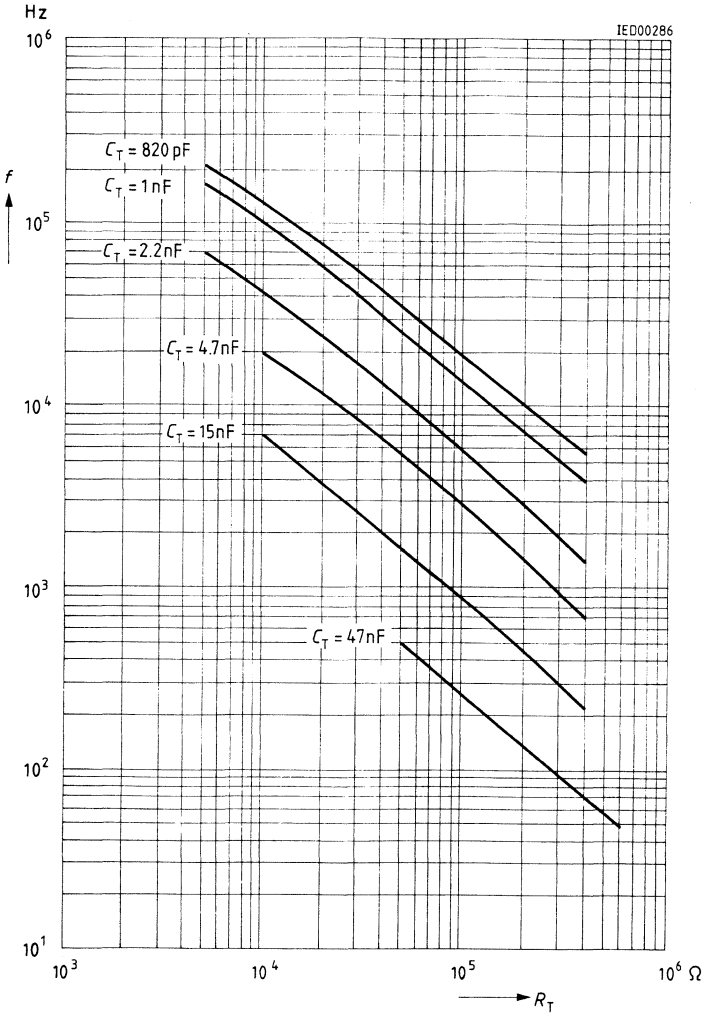
Dimensioning Notes for RC Network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 × output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\ start}$
5. Wiring of the operational amplifier according to the dynamic requirements (TDA 4716 C).



Pulse Diagram

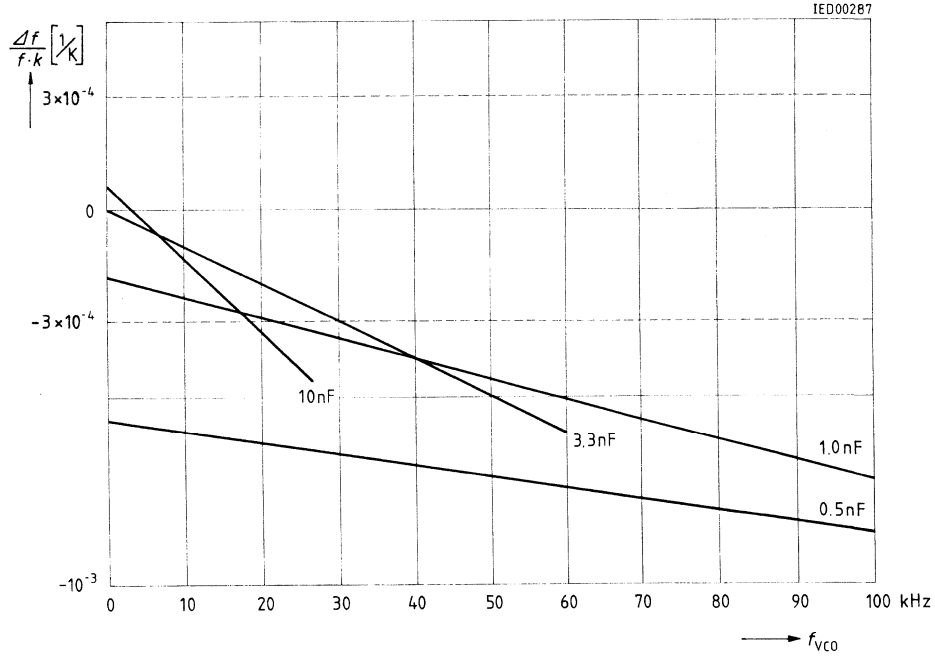
VCO Frequency versus R_T and C_T



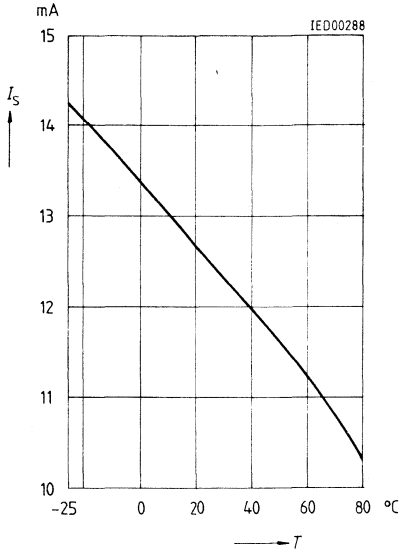
VCO Temperature Response

V_S = 12 V; D = max.

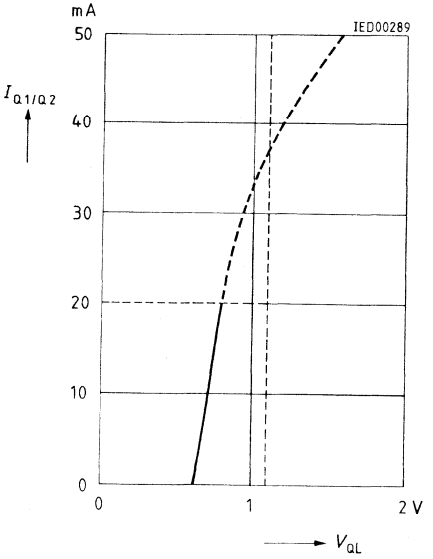
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Supply Current versus Temperature



Output Current versus L-Output Voltage



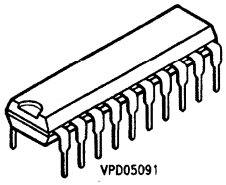
SMPS - IC with SIPMOS Driver Output

TDA 4918
TDA 4919

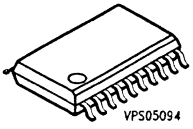
Bipolar IC

Features

- Switching frequency up to 300 kHz (TDA 4919) or 150 kHz (TDA 4918)
- Push-pull output driver with + 700 mA/– 500 mA
- Separate GND for the driver outputs
- Feed-forward control
- Soft start
- Hysteresis adjustable at overvoltage and undervoltage comparator
- Current-saving starting circuit
- Current mode and voltage mode operation are possible



P-DIP-20-1

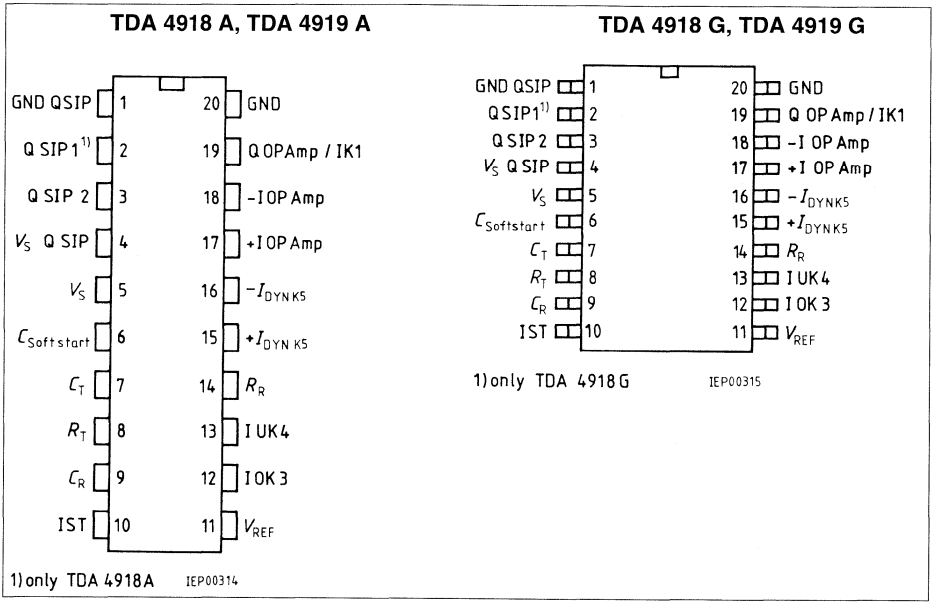


P-DSO-20-1

Type	Ordering Code	Package
S TDA 4918 A	Q67000-A8021	P-DIP-20-1
S TDA 4918 G	Q67000-A8142	P-DSO-20-1 (SMD)
S TDA 4919 A	Q67000-A8143	P-DIP-20-1
S TDA 4919 G	Q67000-A8018	P-DSO-20-1 (SMD)

Functional Description

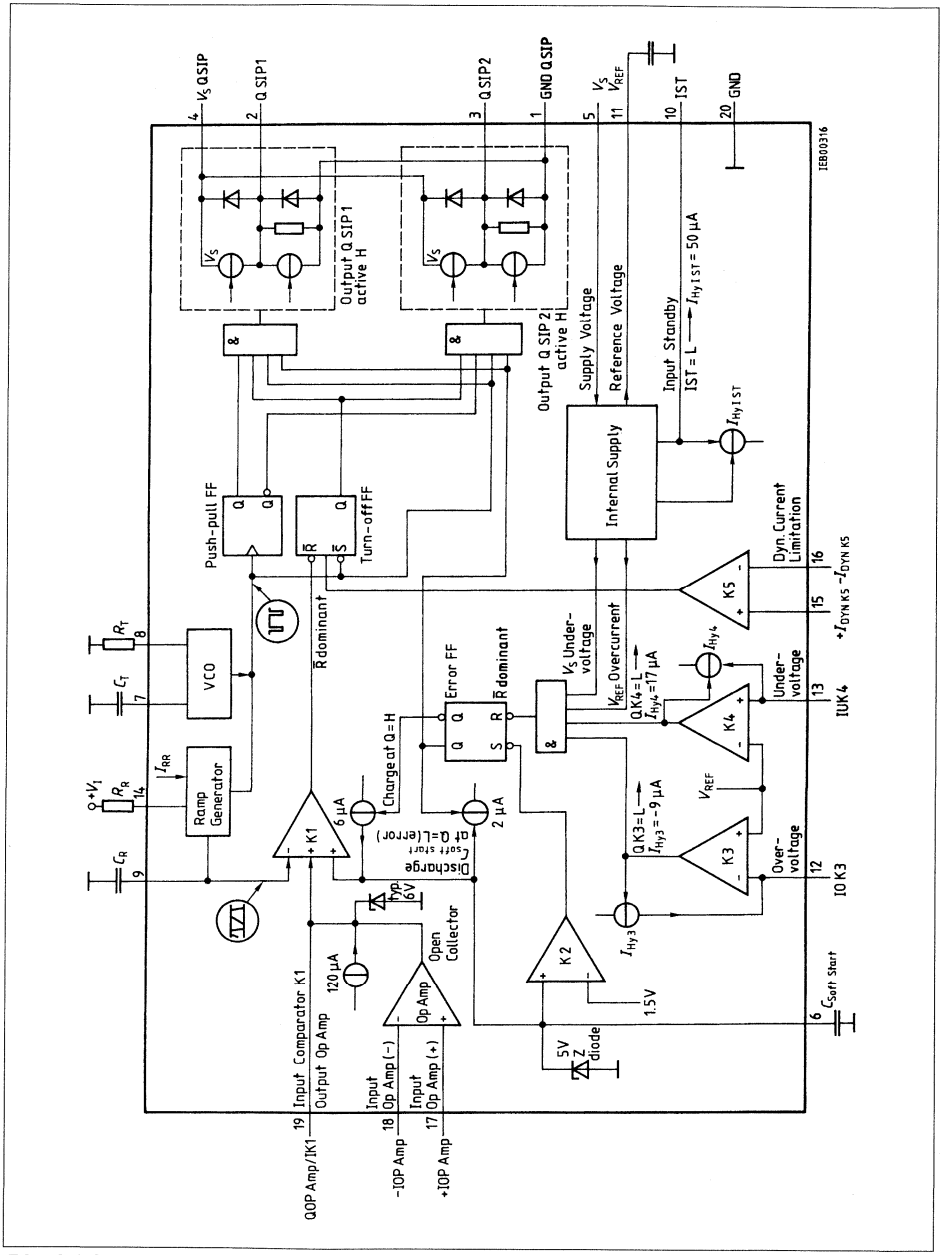
The versatile switch-mode power supply ICs for the direct control of SIPMOS power transistors comprise digital and analog functions. These functions are required for the design of high-quality flyback and forward converters during single-phase and push-pull operation in normal, half-bridge and full-bridge configurations. The ICs can also be used for transformerless voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switch-mode power supply are recognized by on-chip comparators which activate protective functions. The TDA 4918 has two driver outputs for push-pull switch-mode power supplies, as well as single-phase SMPS with a duty cycle limitation of 50 %. The TDA 4919 with a driver output is suitable for single-ended SMPS with duty cycles of up to 100 % approximately.



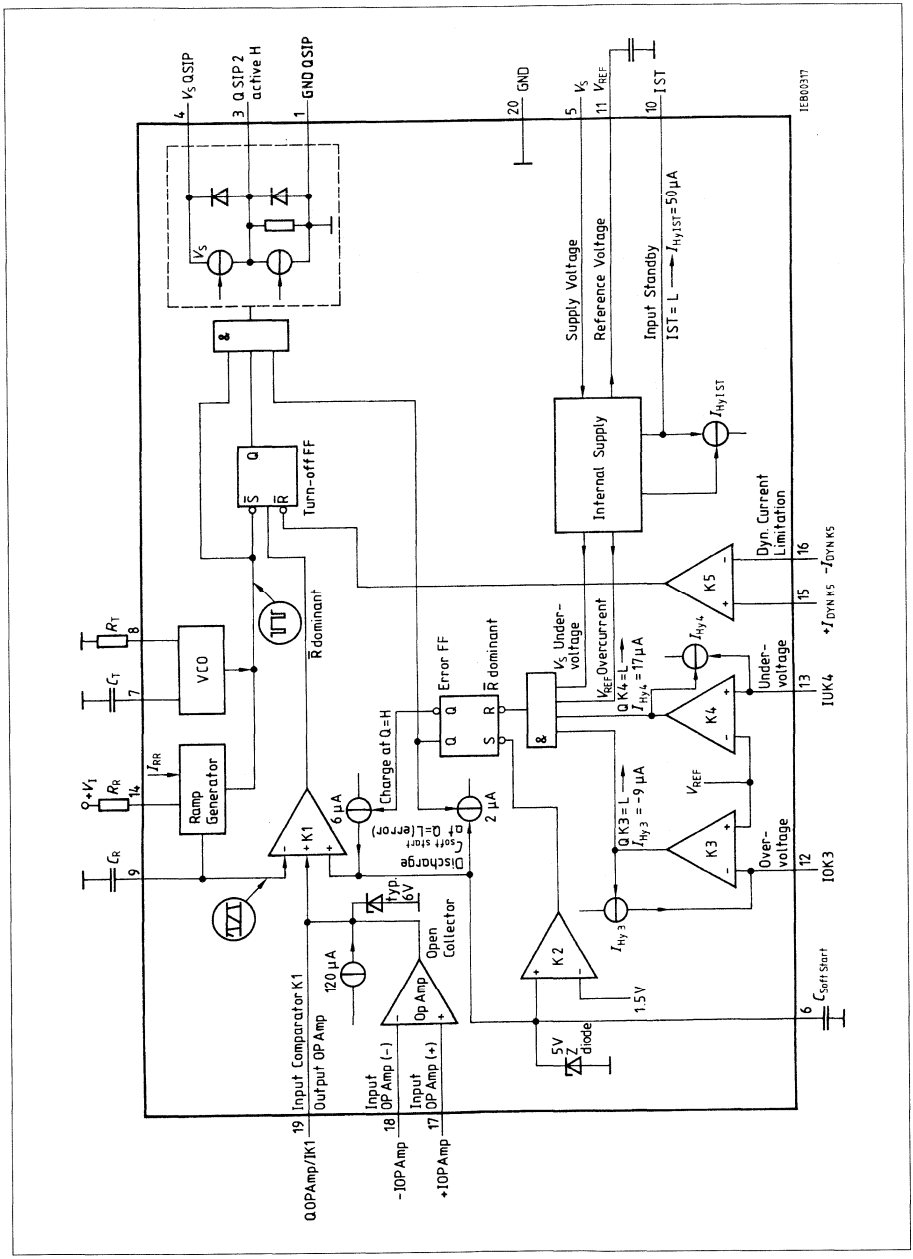
Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND Q SIP	Ground driver
2	Q SIP1	SIPMOS driver 1 (only TDA 4918)
3	Q SIP2	SIPMOS driver 2
4	V_S QSIP	Supply voltage driver
5	V_S	Supply voltage
6	$C_{soft\ start}$	Soft start
7	C_T	Frequency generator
8	R_T	Frequency generator
9	C_R	Ramp generator
10	I ST	Input standby
11	V_{REF}	Reference voltage
12	I OK3	Input overvoltage
13	I UK4	Input undervoltage
14	R_R	Ramp generator
15	$+ I_{DYN\ K5}$	Dyn. current limitation
16	$- I_{DYN\ K5}$	Dyn. current limitation
17	I Op Amp (+)	Input operational amplifier
18	I Op Amp (–)	Input operational amplifier
19	Q Op Amp/IK1	Output operational amplifier Q Op Amp / input comparator
20	GND	Ground



Block Diagram (TDA 4918)



Block Diagram (TDA 4919)

Functional Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

The IC enables the two outputs not before the turn-on threshold ($V_{S\,ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp Generator

The ramp generator is triggered by the VCO and TDA 4919 operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g. input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-Pull Flipflop (only TDA 4918)

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two SIPMOS driver outputs is enabled at a time.

Comparator K1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K1. A voltage change is thus converted to a duty cycle change.

Turn-OFF Flipflop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-OFF flipflop set, the outputs are enabled. Upon an error signal from K5 or upon a turn-off signal from K1 the flipflop disables the outputs.

Z-Diode

The Z-diode limits the voltage at capacitor $C_{\text{soft start}}$ to a maximum of 5 V. The ramp generator voltage can reach 5.5 V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5 V at the plus input, and with its output it sets the error flipflop if the voltage at capacitor $C_{\text{soft start}}$ is below 1.5 V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K1 plus inputs - compared with the ramp generator voltage - is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{\text{soft start}}$ is equal to 0. As long as no error exists, the capacitor will be charged to the maximum value of 5 V with a current of 6 µA.

In the case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 µA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5 V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error Flipflop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the outputs (low), and after elimination of the error, a restart of the outputs by soft start.

Comparators K3 (Overvoltage), K4 (Undervoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K3 and K4, that can be used to enable an adjustable hysteresis or a holding function. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K3 or K4. In the undervoltage case, the set current flows at K4 into the component in the technical direction of current flow, with overvoltage at K3 out of the component.

Comparator K5 (Dynamic Current Limiter)

K5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Standby Input (I ST)

This input switches voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S - standby input - ground.

In standby mode the component has a much lower current consumption compared to active operation. The outputs are then active low.

Should the component be operated by means of feedback supply from the switch-mode power supply, the starting phase can optimally be dimensioned.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp, the error comparators, the ramp generator, or other external components. The voltage source is short-circuit proof to ground.

SIPMOS Driver Outputs (Q SIP)

TDA 4918

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

TDA 4919

The output is active high. The duration during which the output is active can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which the output is low (dead time).

The output drivers are designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at pin I St).

Output Q SIP is connected with the supply voltage $V_{S\,Q\,SIP}$ and with ground via diodes.

The diode connected to V_S routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at V_S during turning on the SMPS supply voltage. The voltage at V_S can reach approximately 2.3 V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to – 0.7 V. This provides an unimpeded flow off of capacitive currents occurring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approx. 2 V, both outputs are active low in the disabled state. The function of the diode connected to V_S is then taken over by the pull-down source.

The maximum output voltage is limited by the respectively lowest value of V_S, $V_{SQ\,SIP}$ or an internal Z-diode. The internal Z-diode limits the voltage at Q SIP to typ. 20 V.

Absolute Maximum Ratings

T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SQSIP}, V_S	– 0.3	33	V
Inputs Op Amp, K3, K5, I ST	V_I	– 0.3	33	V
Input K4	V_I	– 0.3	V_S	V
Frequency Generator (VCO)				
Voltage at R_T; C_T	V_{CT}, V_{RT}	– 0.3	6	V
Current at C_T	I_{CT}		3	mA
$V_{CT} > 6$ V				
Ramp Generator				
C_R input	V_{CR}	– 0.3	6	V
R_R input	I_{RR}	0	3	mA
Reference voltage	V_{REF}	– 0.3	6	V
Output Op Amp	$V_{Q\ op\ amp}$	– 0.3	6	V
$V_{Q\ op\ amp} > 6$ V	$I_{Q\ op\ amp}$		2	mA
Driver output Q SIP [1]	$V_{Q\ SIP}$	– 0.3	$V_{S\ QSIP}$	V
Q SIP clamp diodes	$I_{Q\ SIP}$	– 100	100	mA
$V_{Q\ SIP} > V_S$ or $V_{Q\ SIP} < -0.3$ V				
Soft start	$V_{C\ soft\ start}$	– 0.3	6	V
$V_{C\ soft\ start} > 6$ V	$I_{C\ soft\ start}$	0	100	µA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 65	125	°C
Thermal resistance				
system - air P-DIP-20	$R_{th\ SA}$		60	K/W
P-DSO-20	$R_{th\ SA}$		90	K/W

The characteristics refer to both the pins connected to ground.

[1] With this, the max. power dissipation or junction temperature must be taken into account!

4

Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S $V_{SQ\ SIP}$	$V_{S\ ON}$ [1]	30 30	V V
Frequency generator (VCO) Ramp generator	f_{VCO} f_R		300 300	kHz kHz
Ambient temperature	T_A	– 40	85	°C
Ground QSIP	$V_{GNDQ\ SIP}$	– 0.3	0.5	V

Characteristics

$V_{SON} < V_S < 30\,V$ [2], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption without load at V_{REF} Q op amp, Q SIP 1/2	I_S	6		18	mA	$C_T = 1$ nF frequency generator with 100 kHz outputs active
Standby operation	I_{ST}			3.5	mA	$V_S = 20$ V

Hysteresis at V_S

Turn-on threshold for V_S rising	V_{SH}			9.6	V	$V_{IST} \geq V_{ISTH}$
Turn-off threshold for V_S falling	V_{SL}	7.8			V	

The characteristics refer to both the pins connected to ground.

1) For V_{SON} values refer to characteristic data.

2) $V_{S\ ON}$ means that $V_{S\ HIGH}$ has been exceeded, while $V_{S\ LOW}$ has not yet been undercut.

Characteristics (cont'd)
$V_{SON} < V_S < 30\,V$ [1], $T_A = -40$ to $85\,^{\circ}C$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference						
Voltage	V_{REF}	2.475	2.5	2.525	V	$I_{REF} = 1\,mA$ $T_A = 25\,^{\circ}C$ $V_S = 15\,V$
Load current	$-I_{REF}$	0		3	mA	
Voltage change Voltage change	ΔV_{REF} ΔV_{REF}			10 3	mV mV	$I_{REF} = 1\,mA \pm 20\%$ $V_S = 15\,V \pm 20\%$
Temperature response	$\Delta V_{REF}/\Delta T\Delta$	− 0.3		0.3	mV/K	
Response threshold for V_{REF} overcurrent	$-I_{REF\,O}$	4	7	10	mA	
Frequency Generator (VCO)						
Frequency range	f_{VCO}			300	kHz	
Frequency change Tolerance	$\Delta f/f_{VCO}$ $\Delta f/f_{VCO}$	− 7		1 7	% %	$V_S = 15\,V \pm 20\%$ $C_T = 1\,nF$ $f_{VCO} = 100\,kHz$; $T_A = 25\,^{\circ}C$
Charge current for C_T (perm.) = current at pin R_T Discharge current for C_T	 $-I_{RT}$ I_{dch}	 0	 2	 1	 mA mA	 $I_{RT} = V_{REF/RT}$ internally fixed
C_T range		0.47		68	nF [2]	
Dead time	T_t		350 400	450 500	ns ns [2]	$C_T = 470\,pF$, $f_{VCO} = 100\,kHz$ $C_T = 470\,pF$, $f_{VCO} = 300\,kHz$

1) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
2) The time of the falling edge (fall time) is proportional to C_T, if the discharge current largely exceeds the charge current. The fall time is proportional to the minimum dead time at the outputs.

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Ramp Generator						
Frequency range	f_R			300	kHz	
Maximum voltage at C_R Minimum voltage at C_R	V_{CRH} V_{CRL}	5.4 1.65	6.1 1.8	6.7 1.95	V V	
Charge current for C_R (perm) = current at pin R_R Discharge current for C_R	 I_{ch} I_{dch}	 0 1.3	 2	 1 2.7	 mA mA	 V_{RR} approx. 0.7 V internally fixed
Ratio $I_{RR}/I_{CR\,charge}$		0.95		1.1		$I_{RR} = 0.5$ mA
Capacitance	C_R	100			pF	
Duty cycle (active time/ period at output)	t_V		5/20			
Temperature coefficient of duty cycle	T_C		0.2		%/K	
Comparator K1						
Input current	$-I_{K1}$			2	µA	
Common-mode input voltage range	V_{IC}	0		V_{CRH}	V	
Turn-OFF delay time	t			500	ns [2]	Rated load 3 nF at Q SIP

[1] $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
[2] Step function $V_{REF} = -100$ mV ⌐► $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Operational Amplifier						
Open-loop voltage gain	G_{V0}	60	80		dB	
Input offset voltage	V_{IO}	– 10		10	mV	Pin 19 n.c.
Input current	$-I_{I\,op\,amp}$			2	µA	
Common-mode input voltage range	V_{IC}	0		4	V	
Output current	$I_{Q\,op\,amp}$	0		2	mA	
Output voltage range	V_Q	0.5		V_{CRH}	V	0 mA < I_Q < 2 mA
Transition frequency Transition phase	f_T ϕ_T		3 120		mHz deg.	
Temperature coefficient of V_{IO}	TC	– 30		30	µV/K	Pin 19 n.c.; V_{IC} = 3 V
Source current at Q Op Amp	$I_{op\,amp}$	70	100	130	µA	0.5 V < V_Q < V_{CRH}
Soft Start						
Charge current for $C_{soft\,start}$ Discharge current for $C_{soft\,start}$	I_{ch} I_{dch}	4 1	6 2	8 3.2	µA µA	
Upper limiting voltage Switching voltage of K2	V_{lim} V_{K2}	4.4 1.3	4.8 1.5	5.0 1.7	V V	

[1] $V_{S\,ON}$ means that V_{SHIGH} has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.

Characteristics (cont'd)
$V_{SON} < V_S < 30$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Current Limitation K5						
Input current Input offset voltage	$-I_{IDYN}$ V_{IO}	– 10		2 10	µA mV	
Common-mode input voltage range	V_{IC}	0		$V_S - 3$	V	
Turn-OFF delay time	t		250	400	ns [2]	Rated load 3 nF at QSIP
Undervoltage K4						
Input current at K4	$-I_{IK4}$			0.2	µA	
Switching voltage at K4	V_{sw}	V_{REF} – 0.01		V_{REF} + 0.01	V	
Hysteresis current	I_{Hy4H} I_{Hy4L}	11	17	22 0.1	µA µA	$V_{(+K4)} < V_{sw}$ $V_{(+K4)} > V_{sw}$
Turn-OFF delay time	t			3	µs [2]	
Overvoltage K3						
Input current	$-I_{IK3}$			0.2	µA	
Switching voltage	V_{sw}	V_{REF} – 0.01		V_{REF} + 0.01	V	
Turn-OFF delay time	t			3	µs [2]	
Hysteresis current	$-I_{Hy3H}$ $-I_{Hy3L}$	6	9	12 0.1	µA µA	$V_{(-K6)} > V_{sw}$ $V_{(-K6)} < V_{sw}$

1) $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
2) Step function $V_{REF} = -100$ mV ⌐► $V_{REF} = +100$ mV (for transit time from input comparator to Q SIP)

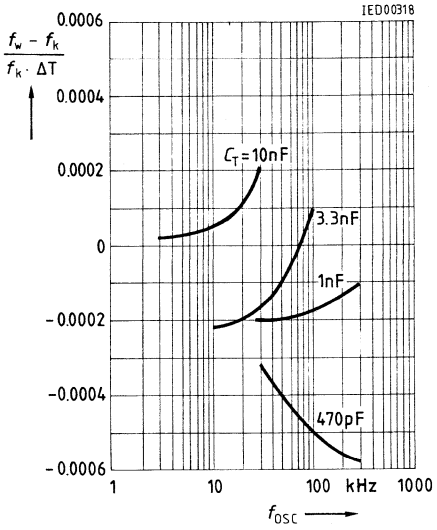
Characteristics (cont'd)
$V_{SON} < V_S < 40$ V [1], $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Driver QSIP 1/2						
H-output voltage	V_{QH}	$V_S - 3$			V	$I_{Q\,SIP} = -250$ mA; $V_S = V_{S\,Q\,SIP}$
L-output voltage	V_{QL}			2.1	V	$I_{Q\,SIP} = +250$ mA; $V_S = V_{S\,Q\,SIP}$
	V_{QL}			1.4	V	$I_{Q\,SIP} = +10$ mA; $V_S = V_{S\,Q\,SIP}$
Output current	$I_{Q\,SIP}$	500	700		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 20$ V
	$-I_{Q\,SIP}$	300	500		mA [2]	
	$I_{Q\,SIP}$		600		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 15$ V
	$-I_{Q\,SIP}$		500		mA [2]	
	$I_{Q\,SIP}$		400		mA [2]	$C_{Q\,SIP} = 10$ nF; $V_S = V_{S\,Q\,SIP} = 10$ V
	$-I_{Q\,SIP}$		400		mA [2]	
Input Standby IST						
Turn-ON threshold for V_{IST} rising	V_{ISTH}	6.1	6.8	7.5	V	$V_S > V_{S\,ON}$; $T_A = 25$ °C
Temperature response	$\Delta V_{ISTH}/\Delta T$		− 0.023		%/K	
Turn-OFF threshold for V_{IST} falling	V_{ISTH}	5.5	6.1	6.7	V	
Temperature response	$\Delta V_{ISTL}/\Delta T$		0.047		%/K	
Hysteresis current	$-I_{HyISTH}$			2	µA	$V_{IST} > V_{IST\,H}$
	I_{HyISTL}	35	50	65	µA	$V_{ISTL} \le V_{IST} \le V_{ISTH}$; $T_A = 25$ °C
Temperature response	$\Delta I_{HyIST}/\Delta T$		0.01		%/K	

[1] $V_{S\,ON}$ means that V_{SHGH} has been exceeded, while $V_{S\,LOW}$ has not yet been undercut.
[2] Dynamic maximum current during rising or falling edge.

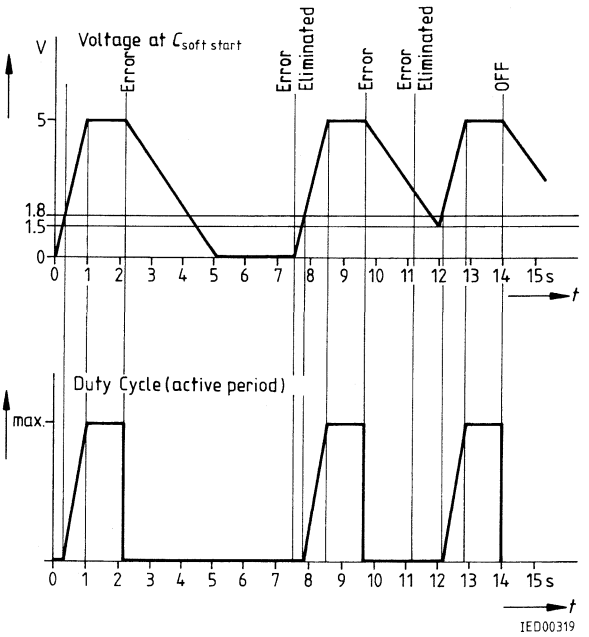
Diagrams

Typical temperature dependance of the frequency generator at different C_T values.

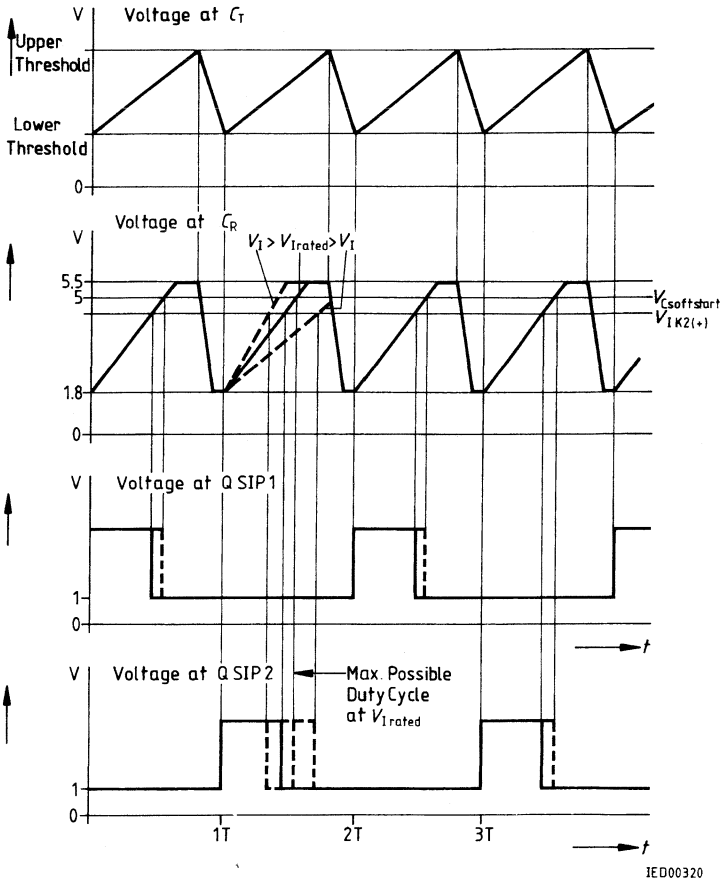


f_k = Frequency at room temperature
f_w = Frequency at thermal increase

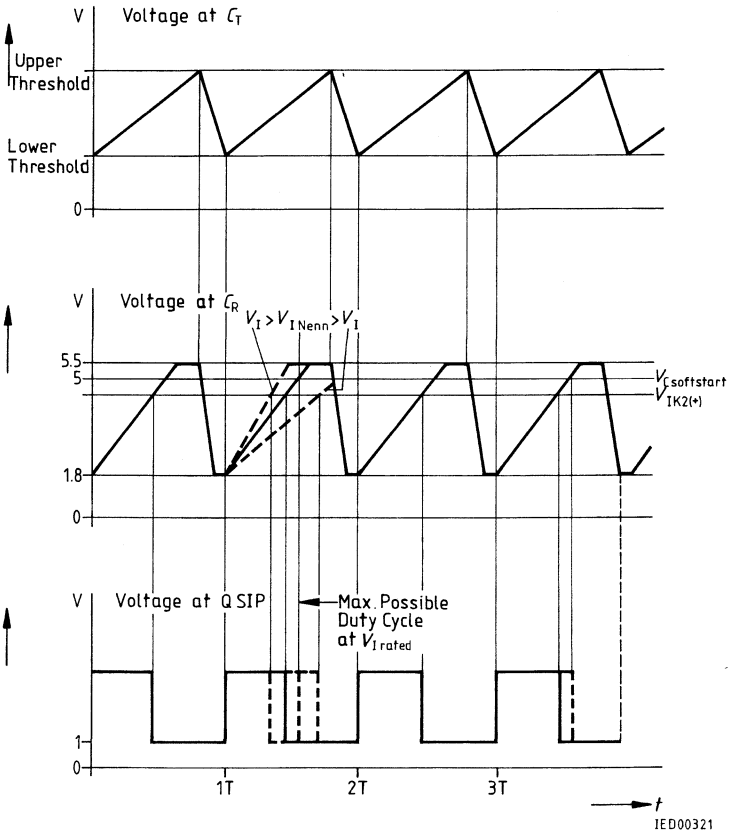
Soft Start/Error/ON-OFF



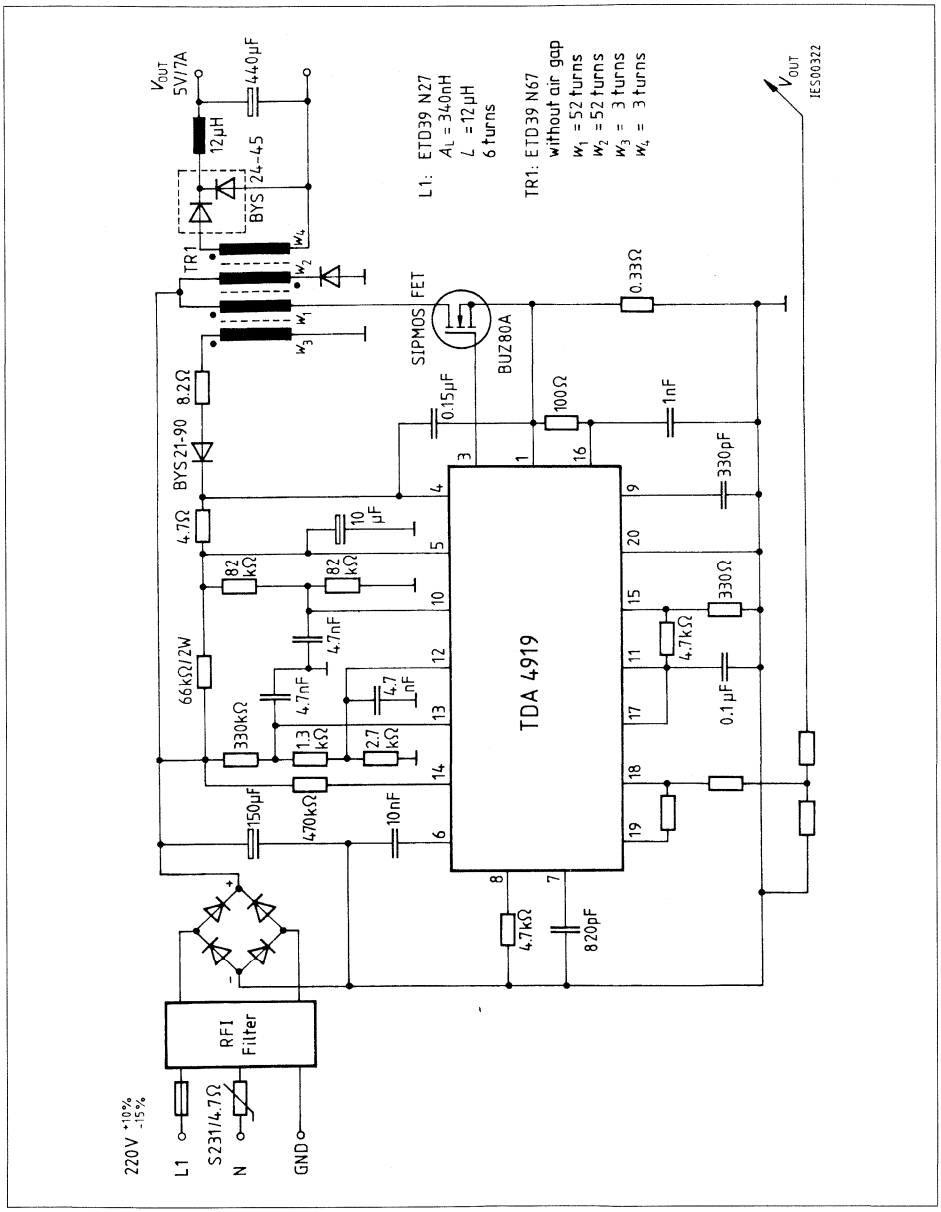
Pulse Diagram



Pulse Diagram (TDA 4918)



Pulse Diagram (TDA 4919)



Application Circuit (TDA 4919)

SIEMENS

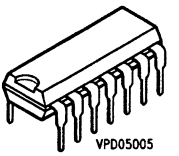
Power Factor Controller IC for High Power Factor and Active Harmonic Filter

TDA 4814
TDA 4816

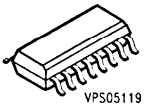
Bipolar IC

Features

- IC for sinusoidal line-current consumption
- Power factor approaching 1
- Controls boost converter as an active harmonics filter
- Direct drive of SIPMOS transistor
- Zero crossing detector for discontinuous operation mode with variable frequency
- 110/220 V AC operation without switchover
- Standby current consumption of 0.5 mA
- Start/stop monitoring circuit for lamp generators

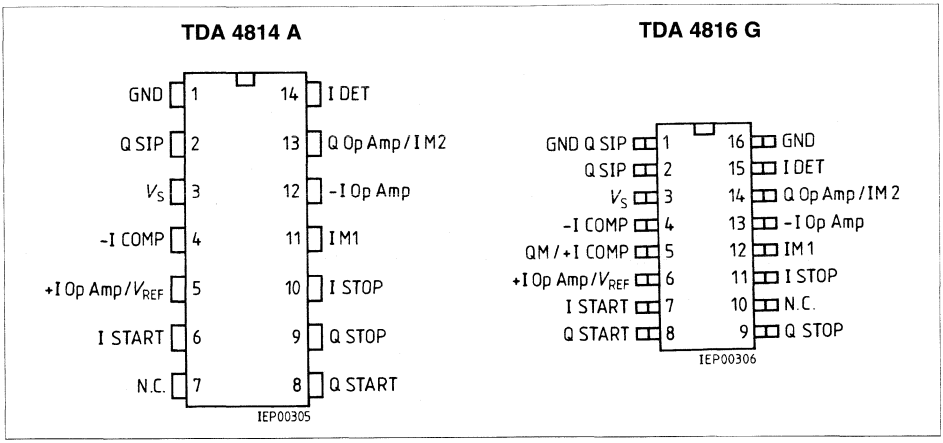


P-DIP-14-1



P-DSO-16-1

	Type	Ordering Code	Package
S	TDA 4814 A	Q67000-A8163	P-DIP-14-1
S	TDA 4816 G	Q67000-A8290	P-DSO-16-1 (SMD)



Pin Configurations
(top view)

Pin Definitions and Functions

Pin		Symbol	Function
P-DIP-14	P-DSO-16		
	1	GND QSIP	Driver Ground
1		GND	Ground
2	2	QSIP	Driver output
3	3	V_S	Supply voltage
4	4	– ICOMP	Negative comparator input
	5	QM/+ICOMP	Multiplier output/positive comparator input
5	6	+I OP Amp/V_{REF}	Positive input/reference voltage
6	7	I START	Start input
7	10	N.C.	Not connected
8	8	Q START	Start output
9	9	Q STOP	Stop output
10	11	I STOP	Stop input
11	12	I M1	Multiplier input M1
12	13	– I OP Amp	Negative input OP amplifier
13	14	QOP Amp/I M2	Op amplifier output and multiplier input M2
14	15	I DET	Detector input
	16	GND	Ground 0 V

The TDA 4814 A and TDA 4816 G contain all functions for designing electronic ballasts and switched-mode power supplies with sinusoidal line current consumption and a power factor approaching 1.

They control a boost converter as an active harmonic filter in a discontinuous (triangular shaped current) mode with variable frequency.

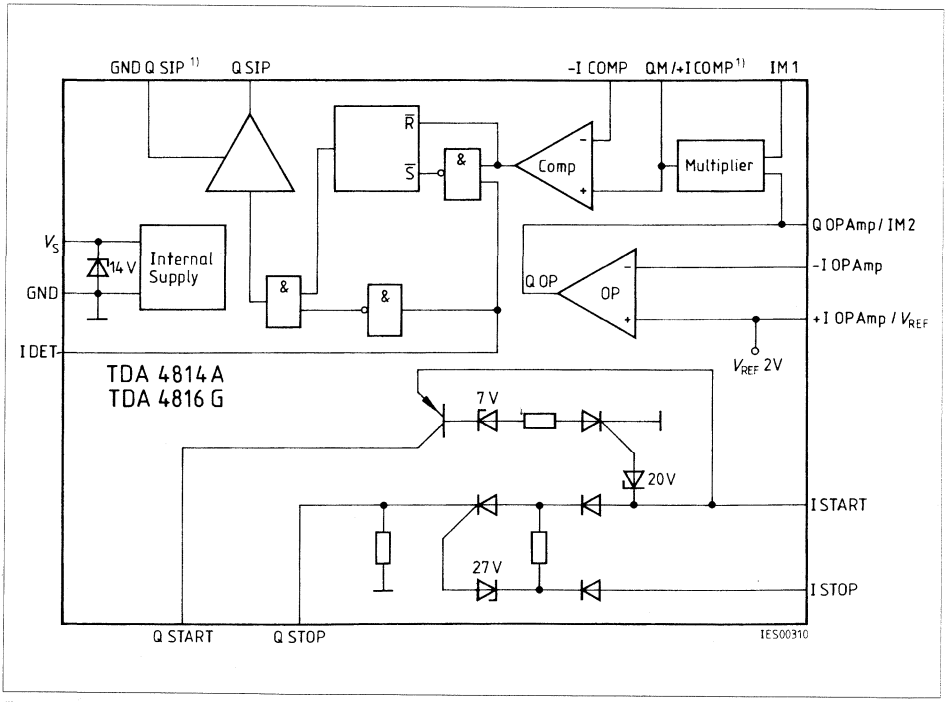
The output voltage of this filter is regulated with high efficiency. Therefore the device can easily be operated on different line voltages (110/220 V_{AC}) without any switchover.

The on-chip start/stop circuit monitors the lamp generator of electronic ballasts. It starts a self-oscillating lamp generator and shuts it down in the event of malfunction, e.g. if the lamp is defective.

A typical application is in electronic ballasts, especially when a large number of such lamps are concentrated on one line supply point.

With the TDA 4816 G the features of the TDA 4814 A have been extended.
The multiplier output was bonded out to faciliate fixed-frequency operation with an additional PWM-IC.
Besides that a separate driver ground (GND QSIP) is implemented.

The TDA 4816 G comes in a P-DSO-16 package, the TDA 4814 A in a P-DIP-14 package.



Block Diagram

Circuit Description

This device has a conditioning circuit for the internal power supply. It allows standby operation with very low current consumption (less than 0.5 mA), a hysteresis between enable and switch-off levels and an internal voltage stabilization. An integrated Z-diode limits the voltage on V_S, when impressed current is fed.

The **output driver (Q SIP)** is controlled by detector input and current comparator.

The **detector input (I DET)** which is highly resistive in the operating state reacts on hysteresis-determined voltage levels. To keep down the amount of circuitry required, clamping diodes are provided which allow control by a current source.

The operating state of the boost converter choke is sensed via the detector input. H-level means that the choke discharges and the output driver is inhibited. H-level sets a flip-flop, which stores the switch-off instruction of the current comparator to reduce susceptibility to interference. As soon as demagnetization is finished the choke voltage reverses and the detector input is set to L-level, thus enabling the output driver. This ensures that the choke is always currentless when the SIPMOS transistor switches on and that no current gaps appear.

The nominal voltage of the multiplier output is compared to the voltage derived from the actual line current **(– I COMP)**, thus setting the switch-off threshold of the comparator. The current comparator blocks the output driver when the nominal peak value of the choke current given by the multiplier output is reached.

This state is maintained in the flip-flop until H-level appears at detector input which takes over the hold function and resets the flip-flop.

Operating states might occur without any useful detector signal. This is the case with magnetic saturation of the choke and when the input voltage approaches or exceeds the output voltage as, for example, during switch-on. The driver remains inhibited for the flip-flop due to the absent set signal.

The trigger signal can be derived from the subsequent lamp generator, a SMPS control device or, if neither one of them is available, from the start circuit designed as a pulse generator in the TDA 4814. The trigger signal level should be so low that with standard operation the signal from the detector winding dominates.

The multiplier delivers the preset nominal value for the current comparator by multiplying the input voltage, which determines the nominal waveform **(IM1)** and the output voltage of the control amplifier.

The control amplifier stabilizes the output dc voltage of the active harmonic filter in the event of load and input voltage changes. The **control amplifier** compares the actual output voltage to a reference voltage which is provided in the IC and stable with temperature.

Output Driver

The output driver is intended to drive a SIPMOS transistor directly. It is designed as a push-pull stage.

Both the capacitive input impedance and keeping the gate level at zero potential in standby operation by an internal 10-kΩ-resistor are taken into account. Possible effects on the output driver by line inductances or capacitive couplings via SIPMOS transistor Miller capacitance are limited by diodes connected to ground and supply voltage.

Ground Pins

Between the ground pins GND and GND QSIP, a very close and low-impedance connection is to be established.

Monitoring Circuit (I START, I STOP, Q START, Q STOP)

The monitoring circuit guarantees the secure operation of subsequent circuitries.

Any circuitry that is shut down because of a fault, for instance, cannot be started up again until the **monitoring start (I START / Q START)** has turned on and a positive voltage pulse has been impressed on Q START. This function starts for example the lamp generator of an electronic ballast or generates auxiliary trigger signals for the detector input.

If there is a defect present (e.g. defective fluorescent lamp) the **monitoring stop (I STOP / Q STOP)** will shut down either the entire unit or simply the circuitry that has to be protected. No restart is possible then until the hold current impressed on I START or Q STOP has been interrupted (e.g. by a power down).

4

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_S	– 0.3	V_Z	V	V_Z = Z Voltage
Inputs					
Comparator	V_{ICOMP}	– 0.3	33	V	–
	$V_{-I\ COMP}$	– 0.3	33	V	–
Op Amp	$V_{I\ Op\ Amp}$	– 0.3	6	V	–
	$V_{-I\ Op\ Amp}$	– 0.3	6	V	–
Multiplier	V_{M1}	– 0.3	33	V	–
Outputs					
Multiplier	V_{QM}	– 0.3	3	V	V_S > 3 V
Op Amp	$V_{Q\ Op\ Amp}$ / I_{M2}	– 0.3	6	V	–
Z current V_S GND	I_Z	0	300	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	– 0.3	V_S	V	Observe P_{max}
QSIP clamping diodes	$I_{QSIP\ D}$	– 10	10	mA	$V_Q > V_S$ or $V_Q < -0.3$ V
Input START	$V_{I\ START}$	– 0.3	25	V	see characteristics
STOP	$V_{I\ STOP}$	– 0.3	33	V	see characteristics
Output START	$V_{Q\ START}$	– 10	3	V	–
STOP	$V_{Q\ STOP}$	– 0.3	6	V	–
Detector input	$V_{I\ DET}$	0.9	6	V	–
Detector clamping diodes	$I_{I\ DET}$	– 10	10	mA	$V_{I\ DET}$ > 6 V or $V_{I\ DET}$ < 0.9 V
Capacitance at I START to ground	$C_{I\ START}$	–	150	nF	–
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 55	125	°C	–
Thermal resistance system - air P-DIP-14	$R_{th\ SA}$	–	65	K/W	–
P-DSO-16-1	$R_{th\ SA}$	–	100	K/W	–

Absolute Maximum Ratings (cont'd)

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Operating Range					
Supply voltage	V_S	$V_{S\,ON}$	V_Z	V	Values for $V_{S\,ON}$, V_Z: see characteristics
Z-current	I_Z	0	200	mA	Observe P_{max}
Driver current	$I_{Q\,QSIP}$	– 500	500	mA	–
Operating temperature	T_A	– 25	85	°C	–

Characteristics

$V_{S\,ON}$ [1] < V_S < V_Z; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Current Consumption					
Without load on driver QSIP and V_{REF}; QSIP LOW					
0 V < V_S < $V_{S\,ON}$	I_S	–	–	0.5	mA
$V_{S\,ON}$ < V_S > V_Z	I_S	2.5	5	6.5	mA
Load on QD with SIPMOS gate; dynamic operation 50 kHz; V_S = 12 V; load on Q = 10 nF	I_S	–	–	15	mA
Hysteresis on V_S					
Turn-ON threshold for V_S rising	V_{SH}	9.6	10.4	11.2	V
Switching hysteresis	$V_{S\,hy}$	1.0	–	1.7	V
Comparator (COMP)					
Input offset voltage	V_{IO}	– 10	–	10	mV
Input current	$-I_I$	–	–	2	µA
Common-mode input voltage range	V_{IC}	0	–	3.5	V

Characteristics (cont'd)

$V_{S\,ON}$ [1] < V_S < V_Z; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Operational Amplifier (Op Amp)					
Open-loop voltage gain	G_{V0}	60	80	–	dB
Input offset voltage	V_{IO}	– 30	–	– 10	mV
Input current	$-I_I$	–	–	2	µA
Common-mode input voltage range	V_{IC}	0	–	3.5	V
Output current	$I_{Q\,Op\,Amp}$	– 3	–	1.5	mA
Output voltage	$V_{Q\,Op\,Amp}$	1.2	–	4	V
Transition frequency	f_T	–	2	–	MHz
Transition phase	φ_T	–	120	–	deg.
Output Driver (QSIP)					
Output voltage high	V_{QH}	5	–	–	V
I_Q = – 10 mA	–	–	–	–	–
Output voltage low	V_{QL}	–	–	1	V
I_Q = + 10 mA	–	–	–	–	–
Output current	–	–	–	–	–
rising edge C_L = 10 nF	$-I_Q$	200	300	400	mA
falling edge C_L = 10 nF	I_Q	250	350	450	mA
Reference-Voltage Source					
Voltage 0 < I_{REF} < 3 mA	V_{REF}	1.9	2	2.1	V
Load current	$-I_L$	0	–	3	mA
Voltage change 10 V < V_S < V_Z	ΔV_{REF}		–	5	mV
Voltage change 0 mA < I_{REF} < 3 mA	ΔV_{REF}	–	–	20	mV
Temperature response	ΔV_{REF} / ΔT	– 0.3	–	0.3	mV/K
Z-Diode (V_S – GND)					
Z-voltage I_Z = 200 mA Observe P_{max}	V_Z	13	15.5	17	V

Characteristics (cont'd)

$V_{S\,ON}$ [1] < V_S < V_Z; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Multiplier (M1) [2]					
Quadrant for input voltages	–	–	1	–	qu.
Input voltage M1	V_{M1}	0	–	1	V
Reference level for M1	$V_{REF\,M1}$	–	0	–	V
Input voltage M2	V_{M2}	V_{REF}	–	V_{REF} + 1	V
Reference level for M2	$V_{REF\,M2}$	–	V_{REF}	–	V
Input current M1, M2	$-I_I$	0	–	2	µA
Coefficient for output-voltage source	C_Q	0.4	0.6	0.8	I / V
Max. output voltage	$V_{QM\,max}$	–	1.6	–	V
Output resistance	R_Q	–	5	–	kΩ
Temperature response of output-voltage coefficient	$\Delta TC / C_Q$	– 0.3	– 0.1	0.1	% / K
Monitoring Circuit					
Input I START					
Turn-ON voltage	$V_{I\,ON\,START}$	17	22	26	V
Turn-ON current	$I_{I\,ON\,START}$	50	90	130	µA
Turn-OFF voltage	$V_{I\,OFF\,START}$	2	3.5	5	V
Turn-OFF current	$I_{I\,OFF\,START}$	70	110	150	µA
Input I STOP *)					
Turn-ON voltage	$V_{I\,ON\,STOP}$	27	30	33	V
Turn-ON current	$I_{I\,ON\,STOP}$	100	150	200	µA
Turn-OFF voltage	$V_{I\,OFF\,STOP}$	4.5	6.5	8.5	V
Turn-OFF current	$I_{I\,OFF\,STOP}$	175	250	320	µA
Transfer I START - Q START					
Output current on Q START					
V_{START} = 15 V;					
$V_{Q\,START}$ = 2 V	$-I_{Q\,START}$	400	600	800	mA
Transfer I STOP - Q STOP					
Output current on Q STOP					
I_{STOP} = 1.5 mA;	$-I_{Q\,STOP}$	0.9	1.2	–	mA
V_{STOP} = 18 V;					
$V_{Q\,STOP}$ = 1.2 V;					
I_{STOP} = 0.4 mA;	$-I_{Q\,STOP}$	60	150	–	µA
V_{STOP} = 7 V;					
V_{STOP} = 1.2 V;					

*) The turn-ON voltage of I_{STOP} exceeds the turn-on voltage of I_{START} by at least 3 V.

Characteristics (cont'd)

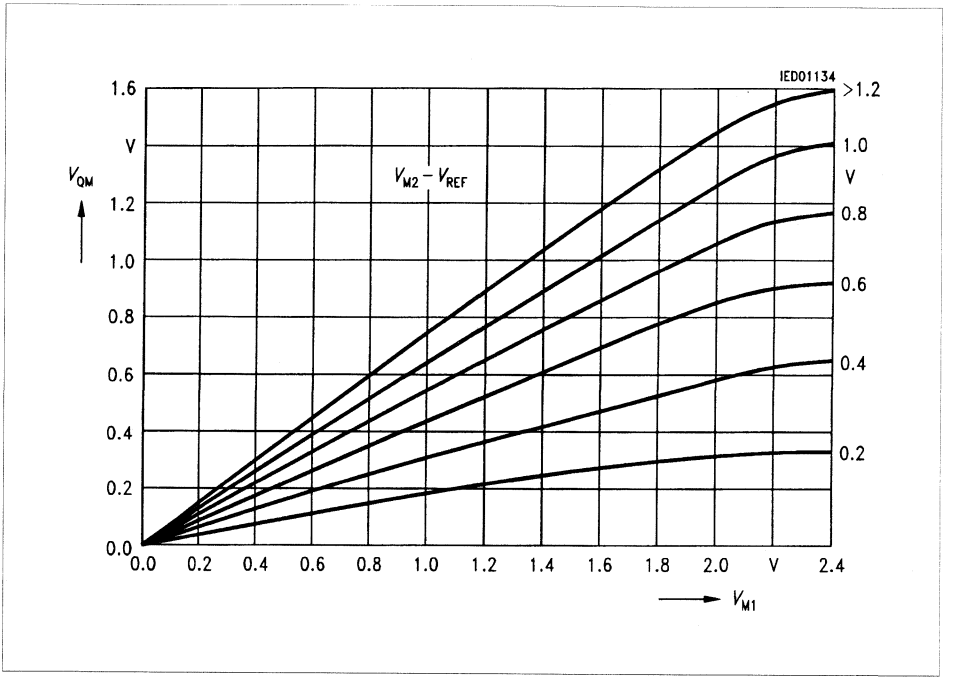
$V_{S\,ON}$ [1] < V_S < V_Z; T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Detector (I DET)					
Upper switching voltage for voltage rising (H)	$V_{DET\,H}$	1	1.3	1.6	V
Lower switching voltage for voltage falling (L)	$V_{DET\,L}$	0.95	–	–	V
Switching hysteresis	$V_{S\,hy}$	50	–	300	mV
Input current 0.9 V < V_{DET} < 6 V	$-I_{DET}$	–	5	10	µA
Clamping-diode current V_{DET} > 6 V or V_{DET} < 0.9 V	I_{DET}	– 3	–	3	mA
Delay Times					
Input comparator QSIP [3]	t	–	200	500	ns

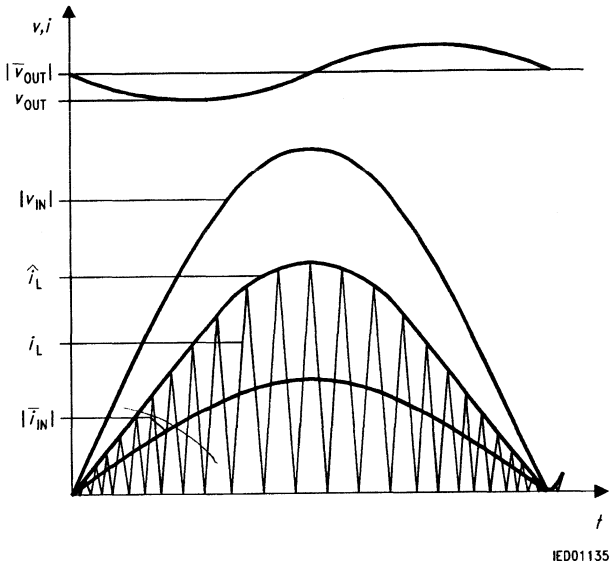
1) $V_{S\,ON}$ means that V_{SH} has been exceeded but that the voltage is still greater than ($V_{SH} - V_{S\,hy}$).

2) Calculation of the output voltage V_{QM}: V_{QM} = C x V_{M1}* x V_{M2}* in V.

3) Step functions at comparator input ΔV_{COMP} = – 100 mV ⌐→ ΔV_{COMP} = + 100 mV.



Multiplier Characteristics



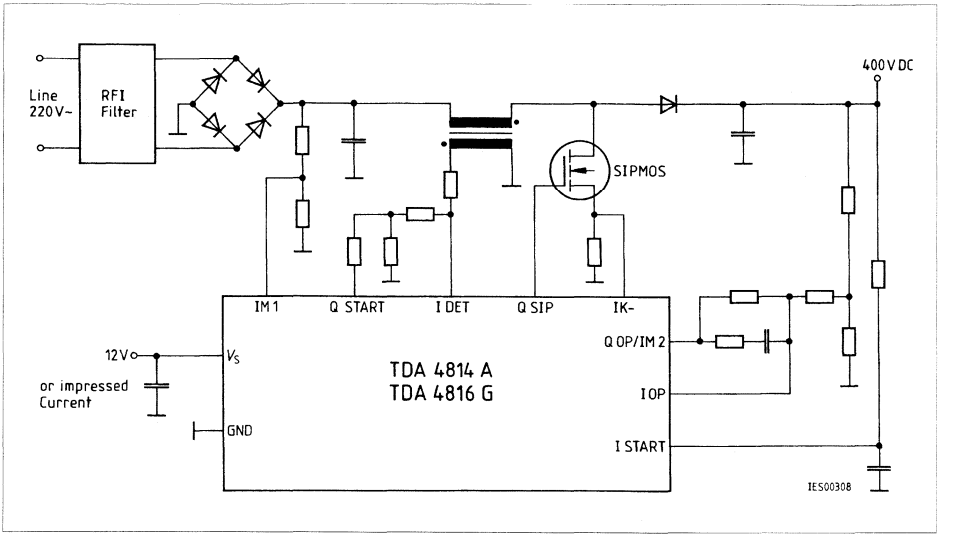
Discontinuous Operation Mode with Variable Frequency

The TDA 4814 A and TDA 4816 G work in a discontinuous operation mode with variable frequency.

The principle of a freely oscillating controller exploits the physical relationship between current and voltage at the boost converter choke. The current in the semiconductors flows in a triangular shape. It is only when the current in the boost converter diode has gone to zero that the transistor goes conductive. This arrangement does away with the diode's power-squandering reverse currents.

If triangular currents flow continuously through the boost converter choke the input current averaged over a high-frequency period is exactly half the peak of the high-frequency choke current.

If the peak values of the choke current are located along an envelope curve that is proportional to a sinusoidal, low-frequency input voltage, the input current available after smoothing in an RFI filter is sinusoidal.



Typical Application Circuit
Boost Converter with TDA 4814 A / 4816 G

The TDA 4814A and TDA 4816G control a boost converter as an active harmonic filter, drawing a sinusoidal line current and providing a regulated DC voltage at the converter output.

The active harmonic filter improves the power factor in electronic ballasts for fluorescent lamps and in switched-mode power supplies, reducing the harmonic content of the incoming, non rectified mains current and if suitably dimensioned permitting operation at input voltages between 90 V and 270 V.

Benefits of TDA 4814 A and TDA 4816 G in Electronic Ballasts and SMPS

- Sinusoidal line current consumption
- Power Factor approaching 1 increases the power available from the AC line by more than 35 % compared to conventional rectifier circuits. Circuit breakers and connectors become more reliable because of the lower peak currents.
- Active harmonic filtering reduces harmonic content in line current to meet VDE / IEC / EN-standards.
- Wide-range power supplies are easier to implement for AC input voltages of 90 to 250 V without switchover.
- Preregulated DC output voltage provides optimal operating conditions for a subsequent converter.
- Reduced smoothing capacitance:
  For a given amplitude of the 100 / 120 Hz ripple voltage the smoothing capacitance can be reduced by 50 % in comparison to a conventional recitifier circuit.
- Reduced choke size:
  Rectifier circuits capable ot more than 200 W usually employ chokes to decrease the charging current of the capacitor. These chokes are larger than those used in a preregulator with power-factor control.
- Higher effciency:
  A preregulator does cause some additional losses, but these are more than cornpensated for by the cut in losses created by the rectifier configuration and the optimum operting conditions that are produced for a subsequent converter, even in the event of supply-voltage fluctuations.

Summary of Effects of DC-Voltage Preregulation with Power-Factor Control

Parameter	Conventional Power Rectification	Power Rectification with Preregulator and Power-Factor Control
Mean DC supply voltage	280 V	340 V
Maximum DC supply voltage with line overvoltage	350 V	350 V
Minimum DC supply voltage with line undervoltage	230 V	330 V
Relative reverse voltage of diodes with line overvoltage	1	0.7
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and line undervoltage	1	2.06
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and rated supply voltage	1	1.74
Relative input capacitance with sustained ripple voltage	1	0.3 to 0.5
Power factor	0.5 to 0.7	0.99

SIEMENS

Power Factor Controller (PFC)

IC for High Power Factor and Active Harmonic Filtering

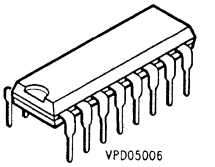
TDA 4815; TDA 4818; TDA 4819

Advance Information

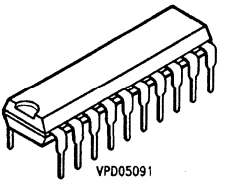
Bipolar IC

Features

- Power factor approaching 1
- For wide-range power supplies
- Continuous mode with fixed frequency (TDA 4815, TDA 4819)
- Discontinuous mode with variable frequency (TDA 4818)
- 0.5 A driver for SIPMOS
- 300 kHz switching frequency
- Feed-forward control
- Complete protective functions



P-DIP-16



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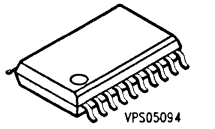


P-DSO-20-1

	Type	Ordering Code	Package
▼	TDA 4815	Q67000-A8323	P-DIP-20-1
▼	TDA 4815 G	Q67000-A8324	P-DSO-20-1 (SMD)
▼	TDA 4818	Q67000-A8325	P-DIP-20-1
▼	TDA 4819	Q67000-A8326	P-DIP-16

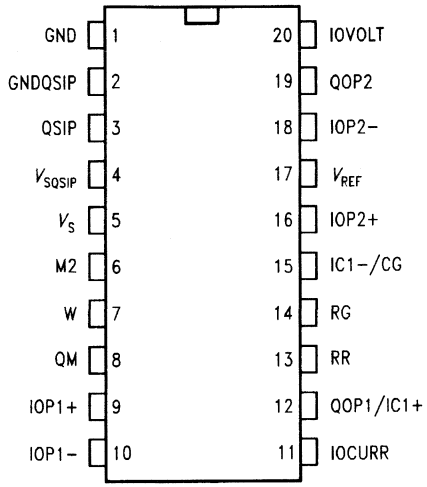
▼ = New type

The TDA 4815, 4818, 4819 family of integrated circuits permits power-factor correction and voltage regulation over a wide range. These devices are designed for preregulators in switched-mode power supplies (SMPS). TDA 4815 and TDA 4819 produce sinusoidal line current generated by trapezoidal shaped current (continuous mode) through the primary inductor. This type of control is particularly suitable for preregulators with a fixed switching frequency and changing load conditions.

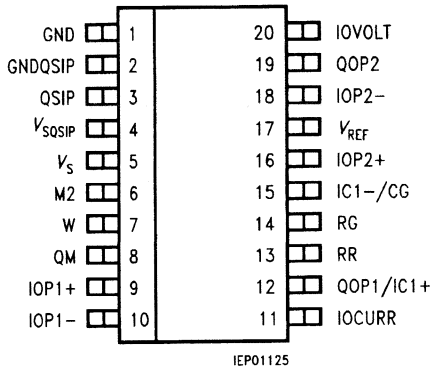
For constant loads and free-running frequency TDA 4818 provides control for triangular shaped current (discontinuous mode). All devices drive SIPMOS transistors directly and feature a multiplier, a pulse-width modulator, two control amplifiers, a reference voltage of 2.5 V plus overvoltage and overcurrent comparators. TDA 4815 additionally features feed-forward control to compensate for known interference such as input-voltage ripple.

TDA 4819 is an economy version of TDA 4815 in a P-DIP-16 package.

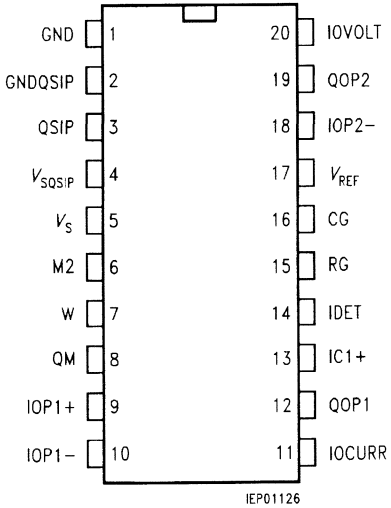
TDA 4815



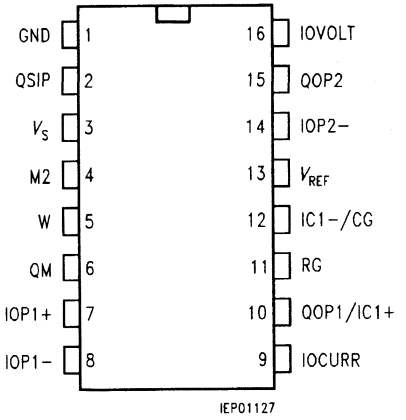
TDA 4815 G



TDA 4818



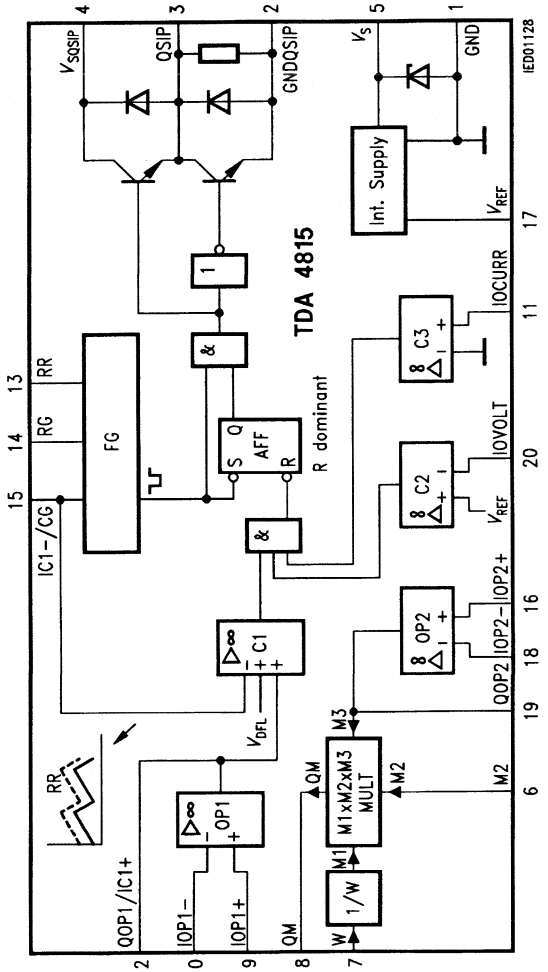
TDA 4819



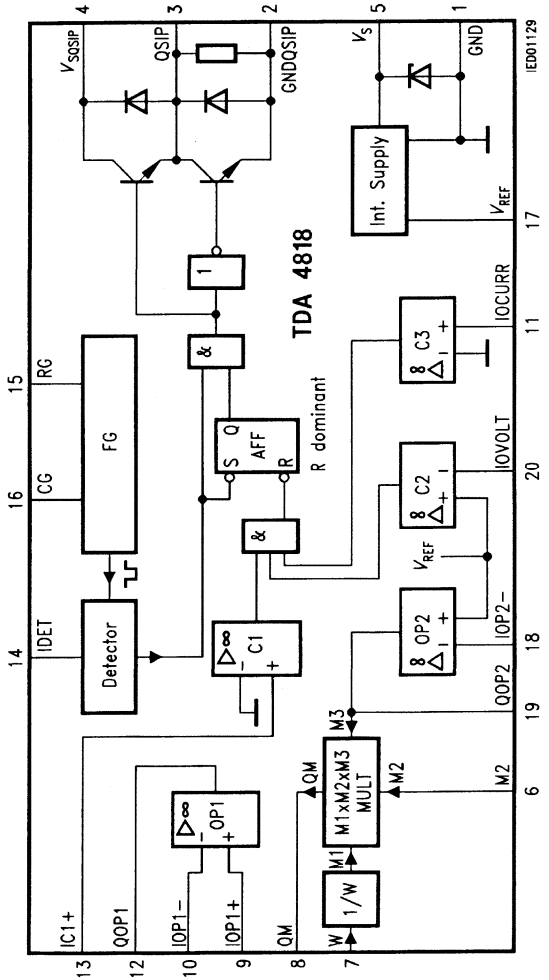
Pin Configuration
(top view)

Pin Definitions and Functions

Symbol	Function
GND	Ground
GNDQSIP	Ground, SIPMOS driver
QSIP	SIPMOS driver output
V_{SQSIP}	Supply voltage, SIPMOS driver
V_S	Supply voltage
M2	Multiplier input
W	Wide voltage range input
QM	Multiplier output
IOP +	Non-inverting input op-amp1
IOP –	Inverting input op-amp 1
IOCURR	Overcurrent sense input
QOP1	Output op-amp 1
IC1 +	Non-inverting input current comparator 1
RR	Ramp generator resistor
RG	Frequency generator resistor
IC1 –	Inverting input current comparator 1
CG	Frequency generator capacitor
V_{REF}	Reference voltage
IOP2 +	Non-inverting input op-amp 2
IOP2 –	Inverting input op-amp 2
QOP2	Output op-amp 2
IOVOLT	Overvoltage sense input
IDET	Detector input



Block Diagram (TDA 4815)



Block Diagram (TDA 4818)

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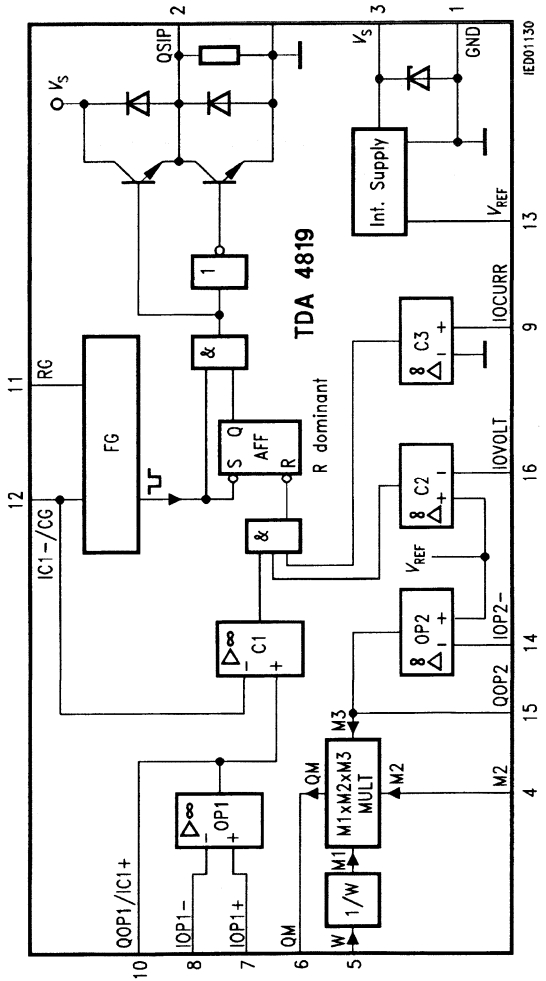


Block Diagram (TDA 4819)

Functional Description

Voltage Supply

The IC does not switch from standby to full current consumption until the turn-ON threshold on V_S is exceeded. Turn-OFF is controlled by hysteresis. The integrated Z-diode limits the voltage on V_S when impressed current is fed.

Operational Amplifier

Operational amplifier 1 (OP1) is a control amplifier and compares the current on the current-sensing resistor to the setpoint on the output of the multiplier. The duty factor that is momentarily necessary is then set via comparator C1 and the ramp generator.

Operational amplifier 2 (OP2) is also configured as a control amplifier. This compares the divided output voltage to the adjusted reference voltage V_{REF}, which is stable with temperature. The output voltage of OP2 produced in this way is multiplied in the triple multiplier by a sine-magnitude voltage. On the output of the multiplier a sine-magnitude current then appears that is variable in amplitude.

Multiplier and 1/W

The multiplier (MULT) processes two, relatively slowly altering voltages (M1, M3) and a sine-magnitude voltage (M2). With the voltage on input M1 preregulation for wide-range AC voltage is produced via 1/W on the input of the SMPS. This takes the load from OP2. The output voltage of the SMPS is regulated to a constant value, independent of the load, with the voltage on input M3.

At its output the multiplier produces an impressed sine-magnitude current. The pulse width of the output signal on QSIP has to be altered so that the potential on the output of the multiplier is always kept on OV. This is managed by OP1, C1 and the ramp generator.

Frequency Generator

The frequency generator (FG) produces a constant frequency for operation with trapezoidal current. The time of the falling edge on FG determines the minimum time for which output QSIP is reliably turned off.

The frequency generator produces on the capacitor CG also the ramp voltage for the pulse width modulation (PWM).

Using the TDA 4818 (with triangular current) the circuit has to be started and possibly restarted at regular intervals. This can be done externally by a lamp generator for instance. But a convenient solution is to use the internal frequency generator to retrigger it.

Feed Forward Control (TDA 4815)

The TDA 4815 has the additional advantage of a feed forward control, i. e. via the input RR (pin 13) the PWM-ramp will be controlled dependent on the line input voltage. The current fed into pin 13 causes (via an internal current mirror) a parallel shift of the PWM-ramp voltage with the transfer ratio V_{Shift}/I_{RR} and without changing the slope. This function controls the duty cycle to increase the dynamic of the current regulator.

The benefit is a better shape of the drawn line current especially at low operation frequencies.

The parallel shift of the PWM-ramp voltage has to be dimensioned this way: If the peak value of the input voltage reaches the output voltage, then V_{Shift} has to correspond to the amplitude of the ramp voltage (typ. 1.5 V).

Detector (TDA 4818)

For operation with triangular current IDET is connected to the current-sensing choke. When input IDET is high, the SIPMOS driver is turned off. At the same time the flipflop (AFF) can be set. When IDET is low and there is no more current flowing in the choke, output QSIP is enabled. After the setpoint current has been reached in the choke, comparator C1 turns the output off again by resetting AFF. In this way the choke is always currentless when the SIPMOS transistor turns on and no gaps appear in the choke current.

Comparators C2 and C3

Comparator C2 turns off output QSIP when the output voltage of the SMPS is overvoltage. Comparator C3 turns off output QSIP when the SIPMOS transistor has source overcurrent. This guards the SMPS against overload during the turn-on operation or if there are abrupt changes in load.

Output QSIP

The output driver is designed as a push-pull stage. There is a resistor of 10 kΩ across QSIP and GND. This keeps the SIPMOS transistor turned off during standby mode.

Output QSIP is also connected via diodes to the supply V_S and to GND.

When the supply of the SMPS is turned on, the diode to V_S conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smoothing capacitor on V_S. The voltage on V_S should not then exceed 0.7 V if the SIPMOS transistor is to remain turned off.

The diode to GND clamps negative voltages on QSIP to – 0.7 V. Capacitive currents produced by voltage breakdown on the drain of the SIPMOS transistor can then flow away unhindered.

Absolute Maximum Ratings
T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	V_Z	V	V_Z = Z-voltage
Supply voltage for SIPMOS driver	V_{SQSIP}	– 0.3	17	V	(**see Characteristics**)
Inputs IC1, IC2, IC3, W, IOP, M2, M3	V_n	– 0.3	17	V	
IDET	V_{IDET}	1	4	V	
	I_{IDET}	– 5	5	mA	V_{IDET} > 4 V or < 1 V
Reference voltage	V_{REF}	– 0.3	6	V	
Outputs QOP	V_{QOP}	– 0.3	6	V	
QM	V_{QM}	– 2	6	V	
Z-current V_S-GND	I_Z	0	70	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	– 0.3	V_{VSQSIP}	V	
QSIP clamping diodes	I_{QSIP}	– 150	50	mA	V_{QSIP} > V_{VSQSIP} or V_{QSIP} < – 0.3 V
Inputs CG, RG, RR	$V_{CG,RG}$	– 0.3	6	V	
	I_{RR}	0	1	mA	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	– 65	125	°C	
Thermal resistance system-air					
TDA 4819	$R_{th\,SA}$		70	K/W	P-DIP-16
TDA 4815, 4818	$R_{th\,SA}$		60	K/W	P-DIP-20
TDA 4815 G	$R_{th\,SA}$		95	K/W	P-DSO-20-1

Operating Range

Supply voltage	V_S	V_{SON}	V_Z	V	1)
Supply voltage QSIP	V_{SQSIP}		17	V	
Z-current	I_Z	0	50	mA	Observe P_{max}
Driver current	I_{QSIP}	– 500	500	mA	Observe P_{max}
Switching frequency	f_{FG}	50	300000	Hz	
Ambient temperature	T_A	– 40	85	°C	
QSIP clamping diodes	I_{QSIP}	– 100	30	mA	Observe P_{max}
GNDQSIP	$V_{GNDQSIP}$	– 0.3	0.5	V	TDA 4815/4818

1) V_{SON} means V_{SH} has been exceeded but the supply voltage is still above V_{SL}. The device has switched from standby to active. For V_{SH} and V_{SL} values, **see Characteristics**. If 0 V < V_S < V_{SON}, the device is on standby and output QSIP is low.

4

Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Without load on driver (QSIP) and V_{REF}:						
QSIP low	I_S			0.7	mA	$0\ V < V_S < V_{S\,ON}$
				10	mA	$V_{S\,ON}$ [1] $< V_S < V_Z$
Load on QSIP with SIPMOS gate; dynamic operation	I_S		20		mA	$V_S = 12$ V; $f_{FG/DET} = 100$ kHz; load QSIP = 3 nF
Hysteresis on V_S						
Turn-ON threshold for V_S rising	V_{SH}		10.5		V	
Turn-OFF threshold for V_S falling	V_{SL}		8.5		V	
Comparators (C1, C2, C3)						
Input offset voltage C2, C3	V_{IO} [2]	− 10		10	mV	
Input offset voltage C1 (TDA 4815, 4819)	V_{IO} [2]		50		mV	
Input offset voltage C1 (TDA 4818)	V_{IO} [2]		100	2	mV	
Input current	$-I_I$				µA	
Common-mode range C1, C2, C3	V_{CM}	− 0.3		V_{DFL}	V	See frequency generator
Operational Amplifiers (OP1, OP2)						
Open-loop voltage again	G_{VOL}	60	80		dB	
Input offset voltage OP1	V_{IO}	0		12	mV	$I_Q = 100$ µA
OP2	V_{IO}	− 6		6	mV	$I_Q = 100$ µA
Input current	$-I_I$			2	µA	
Common-mode range	V_{CM}	− 0.3		4	V	
Output current	I_Q	− 2		1	mA	$1.5\ V < V_Q < 4.5$ V
Output voltage	V_{QOP}	0.8		4	V	
Gain-bandwith product	f_T		2		MHz	
Transition phase	p_T		90		deg	

1) V_{Son} means V_{SH} has been exceeded but voltage is still > V_{SL}. The device has switched from standby to active.

2) $V_{IO} = V_+ - V_-$

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference Voltage (V_{REF})						
Voltage	V_{REF}	0	2.5		V	$0 < I_{REF} < 1$ mA
Load current	$-I_L$			3	mA	
Voltage change	ΔV_{REF}		5		mV	$10\ V < V_S < V_Z$
Voltage change	ΔV_{REF}		10		mV	$0\ mA < I_{REF} < 1$ mA
Temperature response	$\Delta V_{REF}/\Delta T$	– 0.3		0.3	mV/K	
Accuracy		– 1		1	%	$V_S = 12$ V; $I_{REF} = 1$ mA; $T_A = 25$ °C
Output Driver (QSIP)						
H-output voltage	V_{QSIPH}	6			V	$I_{QSIP} = -10$ mA
L-output voltage	V_{QSIPL}			1	V	$I_{QSIP} = 10$ mA
Output current [1]						
rising edge	$-I_{QSIP}$		400		mA	$C_L = 3$ nF
falling edge	I_{QSIP}		500		mA	$C_L = 3$ nF
Z-Diode (V_S-GND)						
Z-voltage (observe P_{max})	V_Z	15		17	V	$I_Z = 50$ mA

1) Maximum current during rising or falling edge.

Characteristics (cont'd)

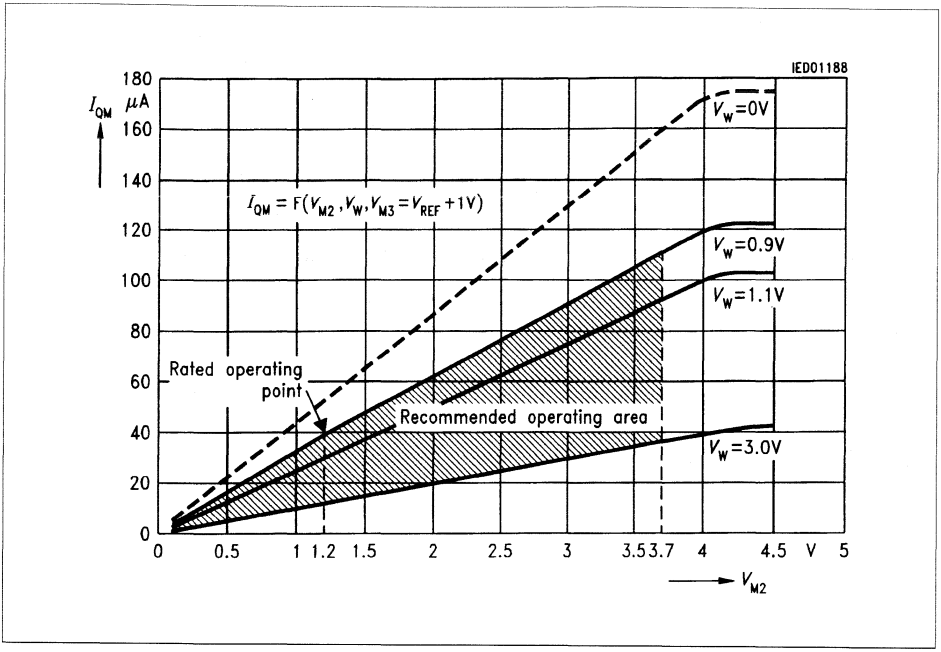
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Multiplier (MULT) and 1/W						
Quadrant for input voltages			I		qu	
Input voltage W	V_W	0.9		3	V	
Reference level for W	$V_{REF\,W}$		0		V	
Input voltage M2	V_{M2}	0		3.7	V	
Reference level for M2	$V_{REF\,M2}$		0		V	
Input voltage M3	V_{M3}	V_{REF}		$V_{QOP(max)}$	V	
Reference level for M3	$V_{REF\,M3}$		V_{REF}		V	
Input current W, M2, M3	$-I_I$	0		2	µA	
Coefficient of output current	k		30		µA/V	
Temperature response of coefficient	$\Delta k/\Delta(k_0 K)$		± 0.1		%/K	
Multiplier output current at rated operating point (ROP)	$I_{QM(ROP)}$		40		µA	Rated operating point: V_{M2} = 1.2 V V_W = 0.9 V $V_{M3} - V_{REF}$ = 1 V

Calculation of output current: $I_{QM} = k \times \frac{V_M \times (V_{M3} - V_{REF})}{V_W}$

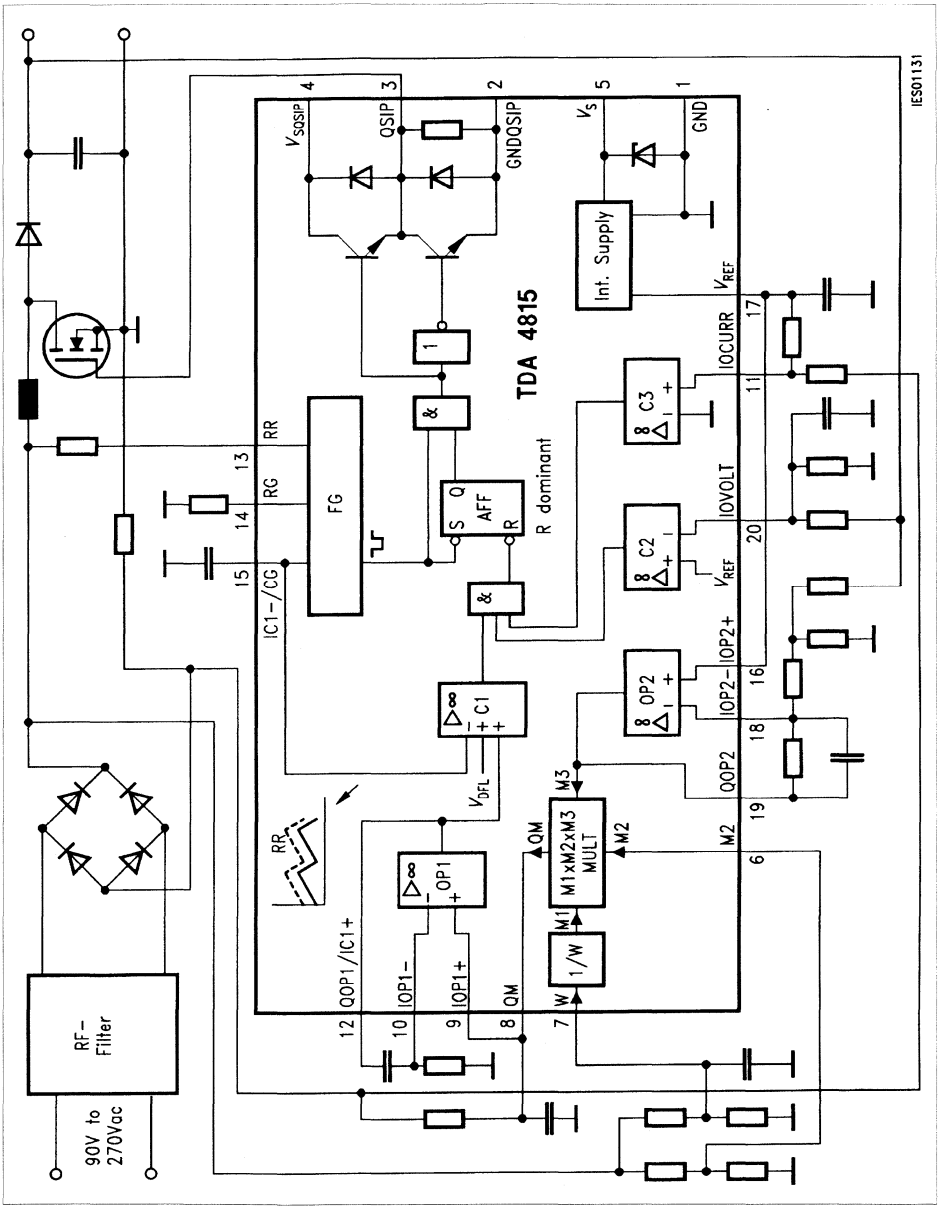
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay Times (C1, C2, C3)						
Between input comp. and QSIP	t [1]		200		ns	
Frequency Generator						
Frequency range	f	0.05		300	kHz	
Frequency deviation	$\Delta f/f_O$		1		%	V_S = 12 V ± 20 %
Tolerance	$\Delta f/f_O$	– 7		7	%	C_G = 1 nF; f_O = 100 kHz; T_A = 25 °C
Permissible charge current for C_G = current on pin R_G	$-I_{RG}$	0		1	mA	$I_{RG} = V_{REF/RG}$
Discharge current on C_G	I_{dis}		3		mA	Set internally
Range of C_G	C_G	0.05		1000	nF	
Minimum dead time	t_D		300		ns	
Upper ramp voltage	V_{Ru}		2.6		V	I_{RR} = 0
Lower ramp voltage	V_{Rl}		0.9		V	I_{RR} = 0
Max. voltage on C_G	V_{CGH}		5.2		V	
Min. voltage on C_G	V_{CGL}		0.9		V	
Current on pin RR	I_{RR}	0		300	µA	V_{RR} = appr. 1.7 V I_{RR} = 100 µA
Transfer ratio V_{Shift}/I_{RR}			25		mV/µA	
Duty factor limiting voltage on C1	V_{DFL}		3.5		V	
Detector						
Upper switching voltage for voltage rising (H)	V_{DETH}		2.6		V	
Lower switching voltage for voltage falling (L)	V_{DETL}		2		V	
Input current	$-I_{DET}$			35	µA	$V_{DETL} < V_{DET} < V_{DETH}$
Clamping-diode current	I_{DET}	– 3		3	mA	$V_{DET} > V_{DETH}$ or $V_{DET} < V_{DETL}$
Switching hysteresis	V_{DEThy}		0.6		V	

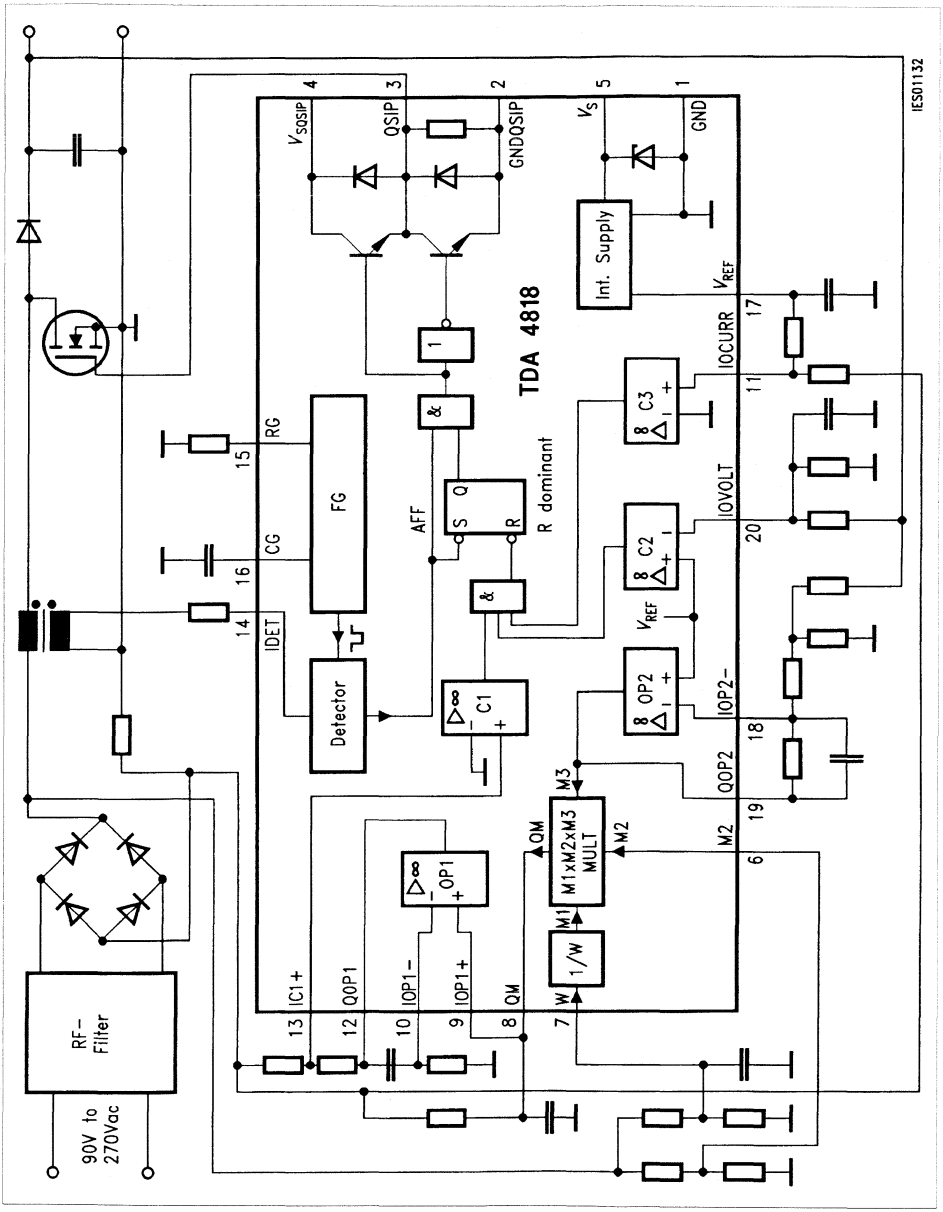
1) Step function on comparator input ΔV_{Comp} from – 100 mV to + 100 mV.



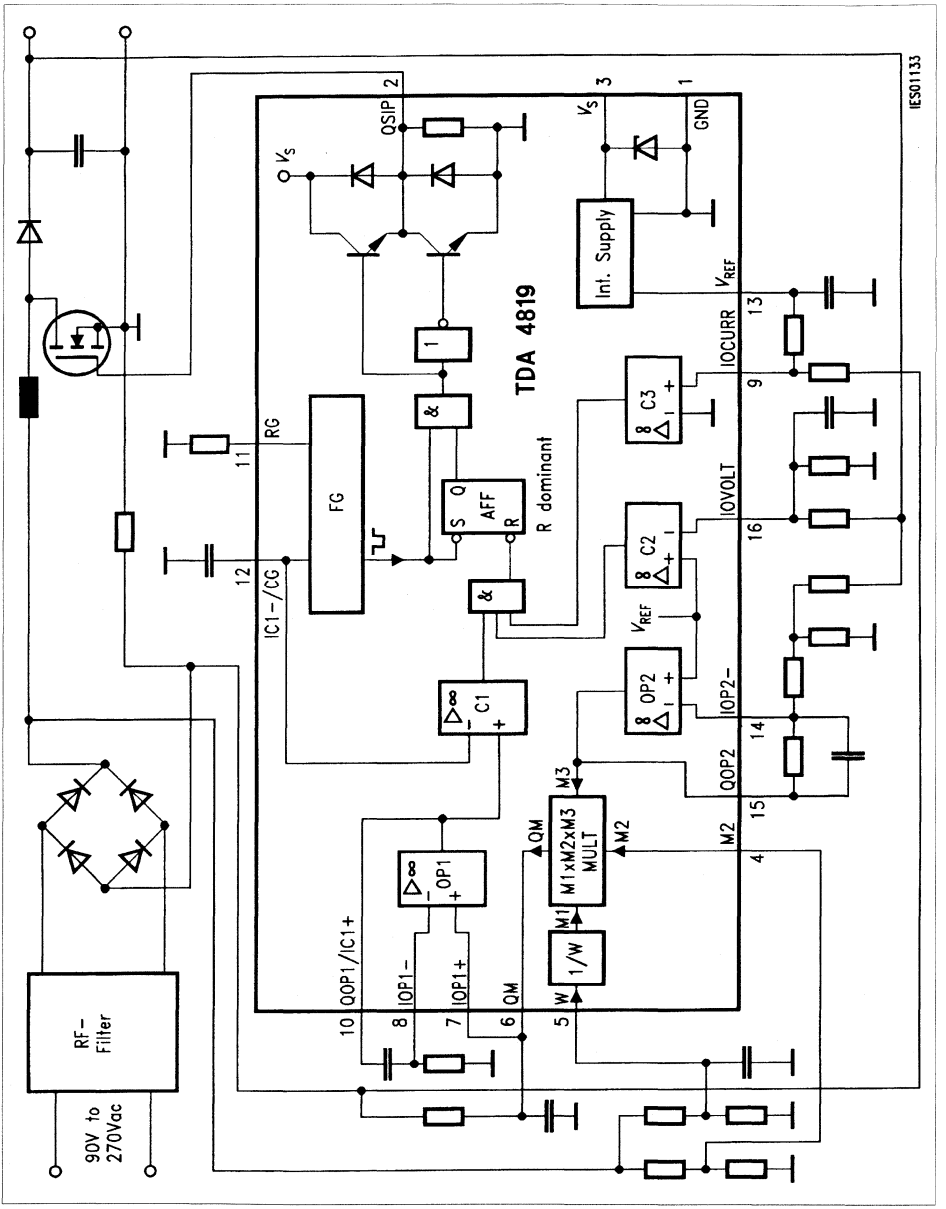
Multiplier Transfer Characteristics
$I_{QM} = f(V_{M2}, V_W, V_{M3} = V_{REF} + 1\ V)$



Application Circuit 1 for Continuous Mode with TDA 4815



Application Circuit 2 for Discontinuous Mode with TDA 4818



Application Circuit 3 for Low-Cost Continuous Mode with TDA 4819

Benefits of Preregulators with Power-Factor Controller in SMPS

- Power-factor correction increases the power available from the AC line by more than 35 % compared to conventional rectifier circuits. Circuit breakers and connectors become more reliable because of the lower peak currents.
- Wide-range power supplies are easier to implement for AC input voltages of 90 to 270 V without switch-over.
- Sinusoidal line current consumption and active harmonic filtering:
  Line harmonics are reduced to a minimum that the power factor is approaching 1 and all standards (IEC 555-2, EN 60555) are fulfilled.
- Stabilized DC output voltage:
  Preregulated DC output voltage provides optimal operating conditions for a subsequent converter.
- Reduced smoothing capacitance:
  For a given amplitude of the 100/120 Hz ripple voltage the smoothing capacitance can be reduced in comparison to a conventional rectifier circuit.
  Reduced choke size:
  Rectifier circuits capable of more than 200 W usually employ chokes to decrease the charging current ot the capacitor. These chokes are larger than those used in a preregulator with power-factor control.
- Higher efficiency:
  A preregulator does cause, some additional losses but these are more than compensated for by the cut in losses created by the rectifier configuration and the optimum operating conditions that are produced for a subsequent converter, even in the event of supply-voltage fluctuations.

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Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and line undervoltage	1	2.06
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and rated supply voltage	1	1.74
Relative input capacitance with sustained ripple voltage	1	0.3 to 0.5
Power factor	0.5 to 0.7	0.99

Differences between Power-Factor Control Using Continuous Mode and Discontinuous Mode

- Continuous Mode (TDA 4815, TDA 4819):
  This is best suited for medium and large power supplies with changing load conditions. The switching frequency is fixed, so the preregulator can synchronize the subsequent converter. A fast diode should be used to reduce switching losses.
- Discontinuous Mode (TDA 4818):
  This is best suited for small ($\leq$ 200 W) power supplies with constant load conditions. The frequency is free-running and the ripple current of the supply slightly higher.

SIEMENS

Power Factor Controller

TDA 4817

IC for High Power Factor and
Active Harmonic Filtering

Advance Information

Bipolar IC

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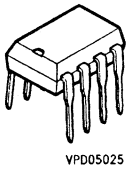
Features

- IC for sinusoidal line-current consumption
- Power factor approaching 1
- Controls boost converter as an active harmonics filter
- Direct drive of SIPMOS transistor
- Zero crossing detector for discontinuous operation mode with variable frequency
- 110/220 V AC operation without switchover
- Standby current consumption of 0.5 mA



P-DIP-8

P-DSO-8-1

	Type	Ordering Code	Package
S ▼	TDA 4817	Q67000-A8298	P-DIP-8
S ▼	TDA 4817 G	Q67000-A8299	P-DSO-8-1 (SMD)

▼ = New type

The TDA 4817 contains all functions for designing electronic ballasts and switched-mode power supplies with sinusoidal line current consumption and a power factor approaching 1.

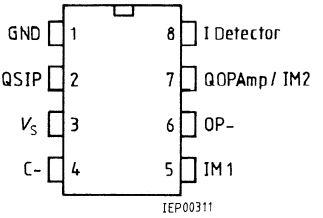
The TDA 4817 controls a boost converter as an active harmonic filter in a discontinuous (triangular shaped current) mode with variable frequency.

A typical application is in electronic ballasts, especially when a large number of such lamps are concentrated on one line supply point.

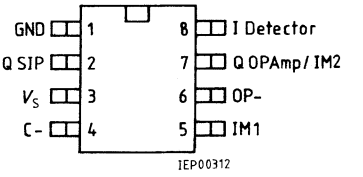
The output voltage of this filter is regulated with high efficiency. Therefore the device can be easily operated on different line voltages (110/220 V_{AC}) without any switchover.

The TDA 4817 is an 8-pin-economy-version of the TDA 4814 A without reference voltage output and start/stop monitoring circuit.

TDA 4817



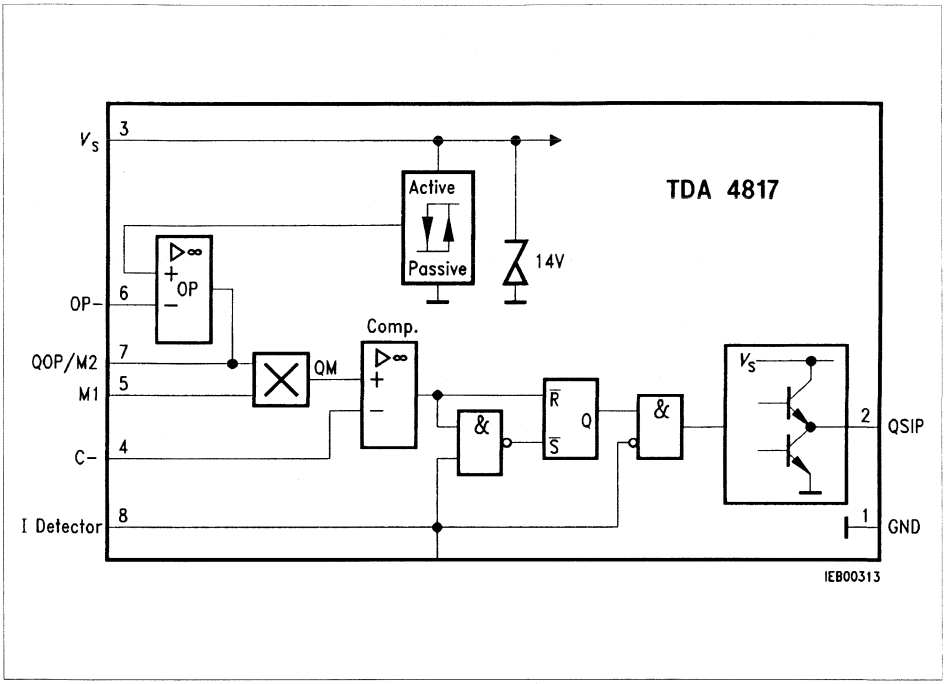
TDA 4817 G



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	QSIP	Driver output
3	V_S	Supply voltage
4	C –	Comparator input
5	IM1	Multiplier input
6	OP –	Input
7	QOP/IM2	Operational-amplifier output QOP and multiplier input M2
8	I Detector	Detector input



Block Diagram

Circuit Description

This device has a conditioning circuit for the internal power supply. It allows standby operation with very low current consumption (less than 0.5 mA), a hysteresis between enable and switch-off levels and an internal voltage stabilization. An integrated Z-diode limits the voltage on V_S, when impressed current is fed.

The **output driver (Q SIP)** is controlled by detector input and current comparator.

The **detector input (I DET)** which is highly resistive in the operating state reacts on hysteresis-determined voltage levels. To keep down the amount of circuitry required, clamping diodes are provided which allow control by a current source.

The operating state of the boost converter choke is sensed via the detector input. H-level means that the choke discharges and the output driver is inhibited. H-level sets a flip-flop, which stores the switch-off instruction of the current comparator to reduce susceptibility to interference. As soon as demagnetization is finished the choke voltage reverses and the detector input is set to L-level, thus enabling the output driver. This ensures that the choke is always currentless when the SIPMOS transistor switches on and that no current gaps appear.

The nominal voltage of the multiplier output is compared to the voltage derived from the actual line current **(– I COMP)**, thus setting the switch-off threshold of the comparator. The current comparator blocks the output driver when the nominal peak value of the choke current given by the multiplier output is reached.

This state is maintained in the flip-flop until H-level appears at detector input which takes over the hold function and resets the flip-flop.

Operating states might occur without any useful detector signal. This is the case with magnetic saturation of the choke and when the input voltage approaches or exceeds the output voltage as, for example, during switch-on. The driver remains inhibited for the flip-flop due to the absent set signal.

The trigger signal can be derived from the subsequent lamp generator or a SMPS control device. The trigger signal level should be so low that with standard operation the signal from the detector winding dominates. The multiplier delivers the preset nominal value for the current comparator by multiplying the input voltage **(IM1)**, which determines the nominal waveform and the output voltage of the control amplifier.

The control amplifier stabilizes the output dc voltage of the active harmonic filter in the event of load and input voltage changes. The **control amplifier** compares the actual output voltage to a reference voltage which is provided in the IC and stable with temperature.

Output Driver

The output driver is intended to drive a SIPMOS transistor directly.

It is designed as a push-pull stage.

Both the capacitive input impedance and keeping the gate level at zero potential in standby operation by an internal 10-kΩ-resistor are taken into account. Possible effects on the output driver by line inductances or capacitive couplings via SIPMOS transistor Miller capacitance are limited by diodes connected to ground and supply voltage.

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Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply voltage	V_S	– 0.3		V_Z	V	V_Z = Z-voltage
Inputs Comparator Operational amplifier Multiplier	V_C – V_{OP} – V_{M1}	– 0.3 – 0.3 – 0.3		20 20 20	V V V	
Output OP	V_{QOP}	– 0.3		6	V	
Z-current V_S-GND	I_Z	0		100	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	– 0.3		V_S	V	
QSIP clamping diodes	I_{QSIP}	– 10		10	mA	$V_{QSIP} > V_S$ or $V_{QSIP} < -0.3$ V
Detector input	V_{Det}	0.9		6	V	
Detector clamping diodes	I_{Det}	– 10		10	mA	$V_{Det} > 6$ V or $V_{Det} < 0.9$ V
Junction temperature	T_j			150	°C	
Storage temperature	T_{stg}	– 55		125	°C	
Thermal resistance system-air TDA 4817 TDA 4817 G	 $R_{th\ SA}$ $R_{th\ SA}$			 100 170	 K/W K/W	 P-DIP-8 package P-DSO-8 package

Operating Range

Supply voltage	V_S	V_{Son}		V_Z	V	1)
Z-current	I_Z	0		100	mA	Observe P_{max}
Driver current	I_{QSIP}	– 500		500	mA	Observe P_{max}
Ambient temperature	T_A	– 25		85	°C	

Characteristics

$V_{SON} < V_S < V_Z$; $T_A = -25$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Without load on driver (QSIP) and V_{REF} ; QSIP low						
Load on QSIP with	I_S			0.5	mA	0 V < V_S < V_{SON}
SIPMOS gate;	I_S		5	10	mA	$V_{SON} < V_S < V_Z$
dynamic operation	I_S			15	mA	V_S = 12 V; f_{switch} = 50 kHz; load QSIP = 10 nF
Hysteresis on V_S						
Turn-ON threshold for V_S rising	V_{SH}	9.6	10.4	11.2	V	
Switching hysteresis	V_{Shy}	1.0		1.7	V	
Comparator						
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Common-mode input voltage	V_{ICM}	0		3.5	V	
Operational Amplifier						
Open-loop voltage gain	G_{VO}	60	80		dB	
Input offset voltage	V_{IO}	– 10		10	mV	
Input current	$-I_I$			2	µA	
Common-mode input voltage	V_{IC}	0		3.5	V	
Output current	I_Q	– 3		1.5	mA	
Output voltage	V_Q	1.2		4	V	
Gain-bandwidth product	f_r		2		MHz	
Transition phase	Φ_T		120		deg	
Reference Voltage Source						
Voltage	V_{REF}	1.9	2			
0 < I_{REF} < 3 mA				2.1	V	
Load current	$-I_L$	0				
Voltage change	ΔV_{REF}			3	mA	
10 V < V_S < V_Z				5	mV	
Voltage change	ΔV_{REF}					
0 mA < I_{REF} < 3 mA				20	mV	
Temperature response	$\Delta V_{REF}/\Delta T$	– 0.3		0.3	mV/K	

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Characteristics (cont'd)

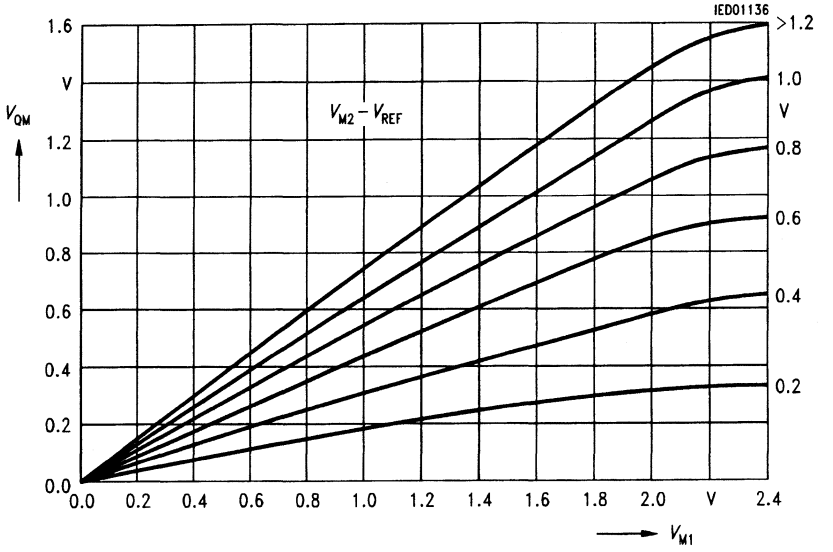
$V_{SON} < V_S < V_Z$; $T_A = -25$ to 85 °C

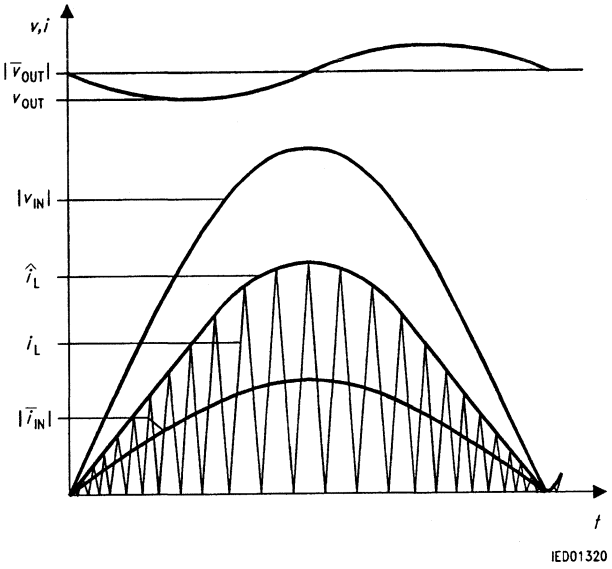
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Driver						
H-output voltage	V_{QSIPH}	5			V	$I_{QSIP} = -10$ mA
L-output voltage	V_{QSIPL}			1	V	$I_{QSIP} = 10$ mA
Output current rising edge	$-I_{QSIP}$	200	300	400	mA	$C_L = 10$ nF
falling edge	I_{QSIP}	250	350	450	mA	$C_L = 10$ nF
Z-Diode (V_S)						
Z-voltage (observe P_{max})	V_Z	13	15.5	17	V	$I_Z = 200$ mA
Multiplier						
Quadrant for input voltages			I.		qu	
Input voltage M1	V_{M1}	0		1	V	
Reference level for M1	$V_{REF\ M1}$		0		V	
Input voltage M2	V_{M2}	V_{REF}		$V_{REF} + 1$	V	
Reference level for M2	$V_{REF\ M2}$		V_{REF}		V	
Input current M1, M2	$-I_I$	0		2	µA	
Max. output voltage	$V_{QM\ max}$		1.6		V	
Coefficient output voltage	C_Q	0.4	0.6	0.8	V^{-1}	
Temperature response of coefficient	$\Delta TC/C_Q$	− 0.3	− 0.1	0.1	%/K	
Delay Times						
Input comparator-QSIP	t_I		200	500	ns	1)
Detector						
Upper switching voltage for voltage rising (H)	V_{DetH}	1.0	1.3	1.6	V	
Lower switching voltage for voltage falling (L)	V_{DetL}	0.95			V	
Input current	$-I_{Det}$			10	µA	0.9 V < V_{Det} < 6 V
Clamping-diode level positive	$V_{Det}+$		6.9		V	$I_{Det} = 3$ mA
negative	$V_{Det}-$		0.6			$I_{Det} = 3$ mA
Switching hysteresis	V_{Dethy}	50		300	mV	

Calculation of output voltage V_{QM}: $V_{QM} = C \times V_{M1} \times V_{M2}$ in V.

1) Step function on comparator input ΔV_{Comp} from − 100 mV to + 100 mV.

Multiplier Characteristics





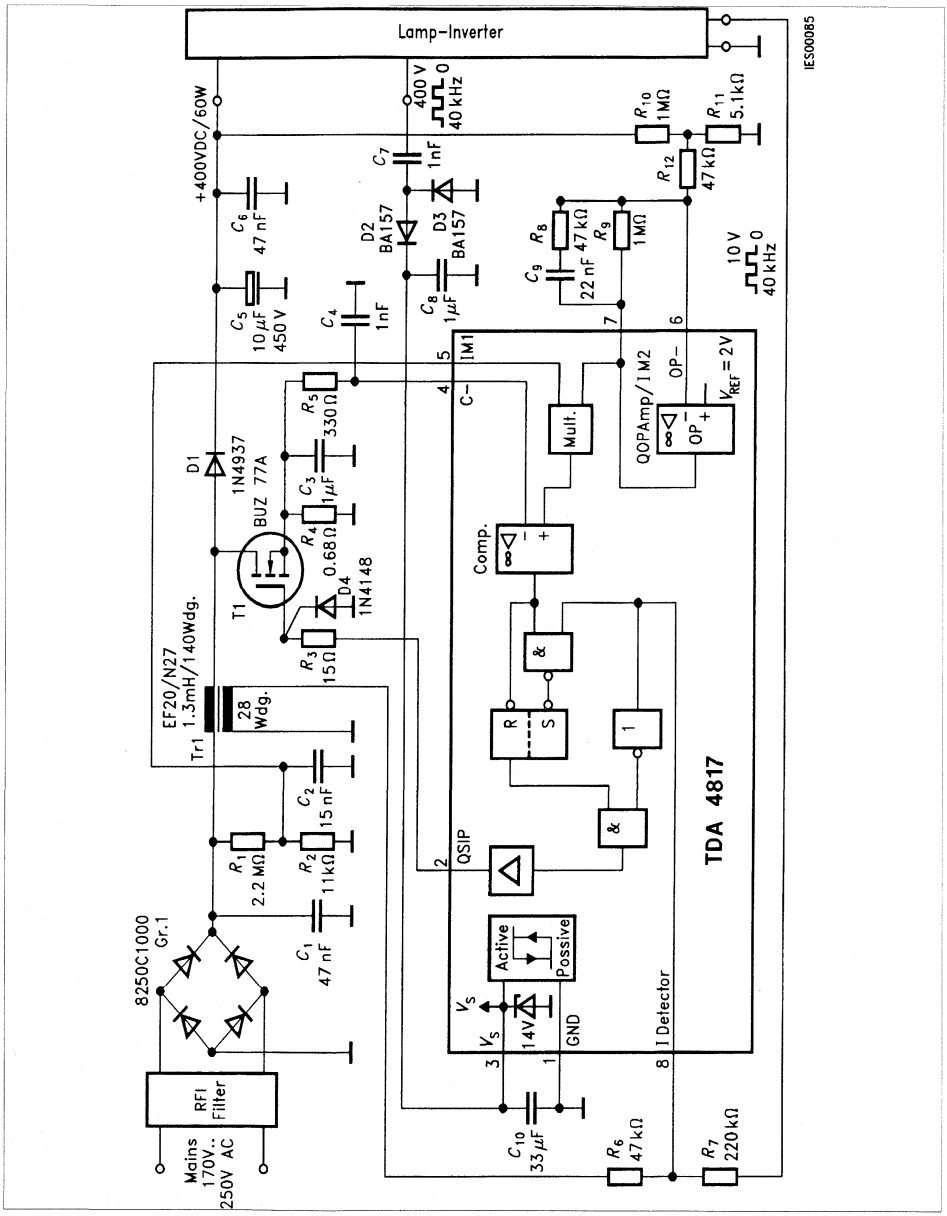
Discontinuous Operation Mode with Variable Frequency

The TDA 4817 works in a discontinuous operation mode with variable frequency.

The principle of a freely oscillating controller exploits the physical relationship between current and voltage at the boost converter choke. The current in the semiconductors flows in a triangular shape. This is only when the current in the boost converter diode has gone to zero that the transistor goes conductive. This arrangement does away with the diode's power-squandering reverse currents.

If triangular currents flow continuously through the boost converter choke the input current averaged over a high-frequency period is exactly half the peak of the high-frequency choke current.

If the peak values of the choke current are located along an envelope curve that is proportional to a sinusoidal low- frequency input voltage, the input current available after smoothing in an RFI filter is sinusoidal.



Application Circuit: Electronic Ballast

The TDA 4817 controls a boost converter as an active harmonic filter, drawing a sinusoidal line current and providing a regulated DC voltage at the converter output.

The active harmonic filter improves the power factor in electronic ballasts for fluorescent lamps and in switched-mode power supplies, reducing the harmonic content of the incoming, non rectified mains current and if suitably dimensioned permitting operation at input voltages between 90 V and 270 V.

Benefits of TDA 4817 in Electronic Ballasts and SMPS

- Sinusoidal line current consumption
- Power factor approaching 1 increases the power available from the AC line by more than 35 % compared to conventional rectifier circuits. Circuit breakers and connectors become more reliable because of the lower peak currents.
- Active harmonic filtering reduces harmonic content in line current to meet VDE/IEC/EN-standards.
- Wide-range power supplies are easier to implement for AC input voltages of 90 to 250 V without switch-over.
- Preregulated DC output voltage provides optimal operating conditions for a subsequent converter.
- Reduced smoothing capacitance:
  For a given amplitude of the 100/120 Hz ripple voltage the smoothing capacitance can be reduced by 50 % in comparison to a conventional rectifier circuit.
  Reduced choke size:
  Rectifier circuits capable of more than 200 W usually employ chokes to decrease the charging current ot the capacitor. These chokes are larger than those used in a preregulator with power-factor control.
- Higher efficiency:
  A preregulator does cause some additional losses, but these are more than compensated for by the cut in losses created by the rectifier configuration and the optimum operating conditions that are produced for a subsequent converter, even in the event of supply-voltage fluctuations.

Summary of Effects of DC-Voltage Preregulation with Power-Factor Control

Parameter	Conventional Power Rectification	Power Rectification with Preregulator and Power-Factor Control
Mean DC supply voltage	280 V	340 V
Maximum DC supply voltage with line overvoltage	350 V	350 V
Minimurn DC supply voltage with line undervoltage	230 V	330 V
Relative reverse voltage of diodes with line overvoltage	1	0.7
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and line under-voltage	1	2.06
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and rated supply voltage	1	1.74
Relative input capacitance with sustained ripple voltage	1	0.3 to 0.5
Power factor	0.5 to 0.7	0.99

5-V Low-Drop Voltage Regulator

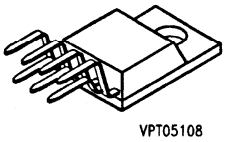
TLE 4258

Preliminary Data

Bipolar IC

Features

- Low-drop voltage
- Low quiescent current
- Reset output
- Protection against reverse polarity
- Overvoltage protection 70 V
- Short-circuit proof
- Suited for automotive electronics
- Inhibit input
- Wide temperature range



P-TO220-7-1

Type	Ordering Code	Package
S TLE 4258	Q67000-A8238	P-TO220-7-1

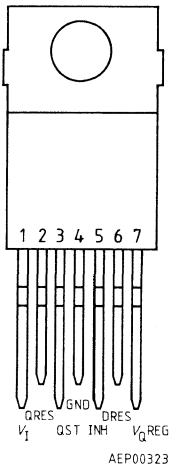
The TLE 4258 is a very low drop voltage regulator which provides two regulated 5-V output voltages. The main regulator can be loaded with 750 mA and is turned on and off by pin 5 (pin 5 unconnected = main regulator off). In addition, the main regulator incorporates a short-circuit current limitation and is turned off in case of overvoltage ($V_I > V_{I\,OFF}$). The standby regulator can be loaded with 35 mA, it does not incorporate a short-circuit current limitation and remains permanently active at positive input voltage independent of the turn-off functions of the main regulator.

If the main regulator output voltage is less than 4.5 V, the reset output is switched to low without delay. As soon as the reset threshold has been exceeded, a delay time to be set by an external capacitor expires and afterwards the reset output switches to high again.

If the lines to the controller are long, the oscillating circuit of line inductance and input capacitance C_I can be attenuated by a resistor $\leq 1\,\Omega$ connected in series to C_I.

Circuit Description

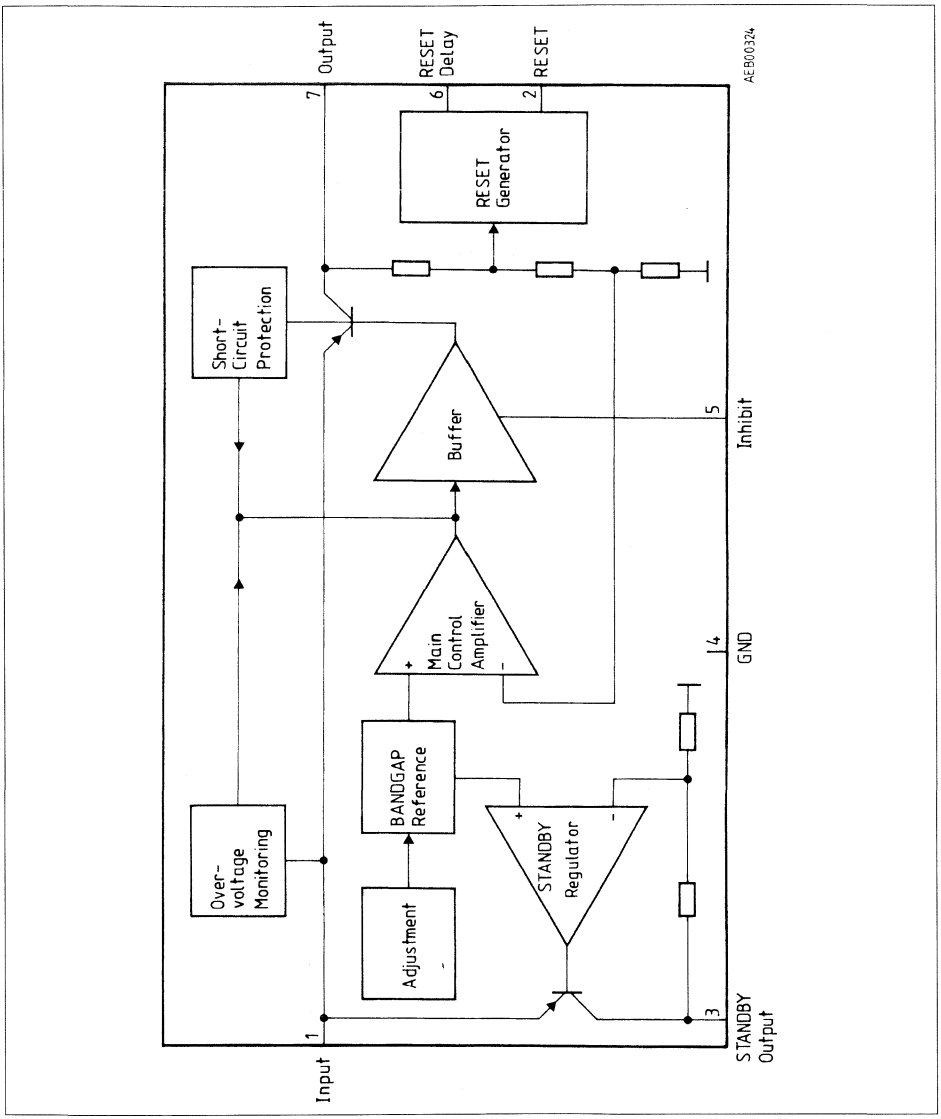
The TLE 4258 incorporates a main and standby-control regulator: The amplifiers regulate the output voltage by comparing the output voltage (from the voltage divider) with a highly precise reference voltage. The standby regulator directly controls the base of a PNP series transistor and the main regulator via a buffer that can be turned off with inhibit pulse at pin 5. If the output voltage V_Q at pin 7 drops below 4.5 V, a reset signal is released which can only be disabled after a delay time to be set at pin 6. The main output is current-limited and remains active up to the input voltage $V_{I\,OFF}$.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	V_I	**Input** of voltage regulator
2	Q RES	**Reset output;** open-collector output NPN to pin 4. If the output voltage V_Q drops below the reset threshold, the output stage becomes conductive.
3	Q ST	**Standby output,** connect with a capacitor ≥ 10 µF
4	GND	**Ground;** reference potential
5	INH	**Inhibit (main regulator ON/OFF),** input for turning on/off main regulator, connected to a 22-kΩ series resistor. With open input, the main regulator remains turned off.
6	D RES	**Reset delay;** pin for reset capacitor; the size of this capacitor determines the delay time of the reset signal typ. 175 ms/µF.
7	V_Q REG	**Main regulator output,** connected to a capacitor ≥ 22 µF.



Block Diagram

Absolute Maximum Ratings

T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input (Pin 1)				
Supply voltage	V_I	– 15	36	V
Polarity reversal with test pulse $t_2 \leq 100$ ms see test circuit	V_I	– 70	–	V
Load-dump with pulse shape $t_2 \leq 400$ ms see test circuit	V_I	–	– 70	V –
Slew rate 0 V ≤ V_I ≤ 24 V	SR	–	100	V/µs
Slew rate 24 V ≤ V_I ≤ 70 V	SR	–	10	V/µs
Current	I_I	–	2.5	A
Reset Output (Pin 2)				
Voltage	V_R	–	8	V
Current	I_R	–	10	mA
Standby Output (Pin 3)				
Voltage	V_{ST}	–	6	V
Current	I_{ST}	–	50	mA
Ground (Pin 4)				
Current	I_{GND}	–	1.8	A
Inhibit (main regulator on/off), (Pin 5) Current	I_{INH}	–	± 7.5	mA
Reset delay (Pin 6) Voltage	V_C	–	V_Q	V
Main regulator output (Pin 7) Voltage $V_I \geq V_Q$ Current	V_Q I_Q	– –	18 1.8	V A
Temperature				
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Input voltage	V_I	6	24	V
Junction temperature	T_j	– 40	150	°C
Thermal resistance system – air system – case	$R_{th\ SA}$ $R_{th\ SC}$	– –	65 4	K/W K/W

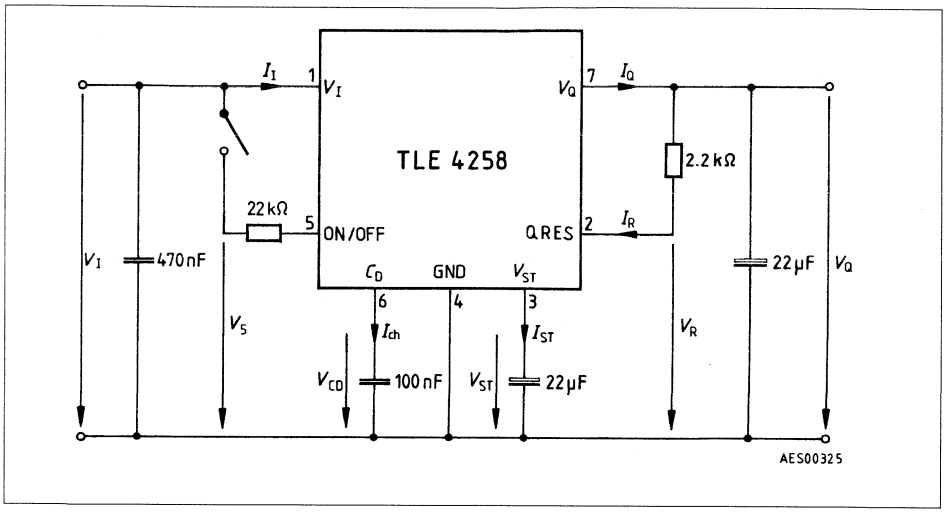
Characteristics

V_I = 13.5 V; T_j = 25 °C; V_5 > 3.5 V (unless otherwise specified)

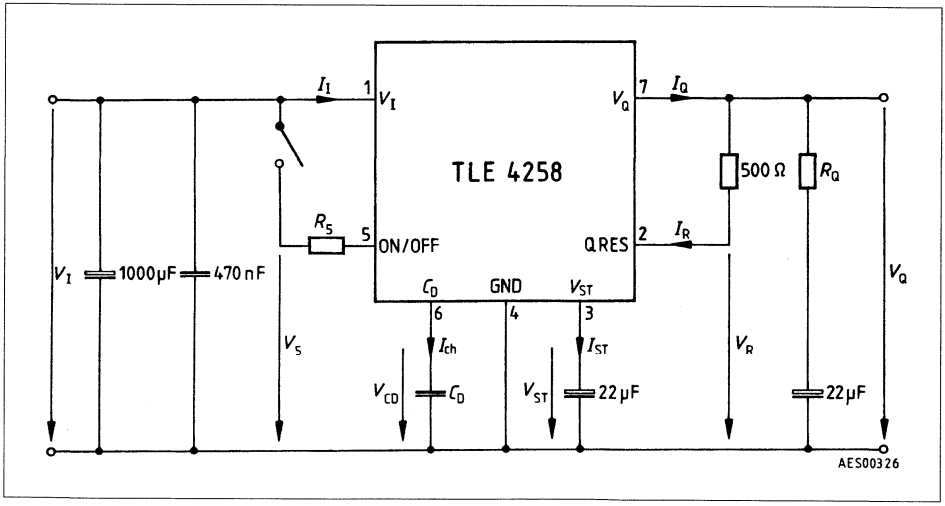
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Main Regulator						
Output voltage	V_Q	4.85	–	5.15	V	0 mA ≤ I_Q ≤ 750 mA 6 V < V_I < $V_{I\,off}$ – 40 °C ≤ T_j ≤ 125 °C
Input current Current consumption without load	I_Q I_Q I_Q I_Q	– – – –	– – – –	30 150 300 300	mA mA mA mA	I_Q = 0 mA; I_{ST} = 0 mA I_Q = 450 mA; I_{ST} = 0 mA I_Q = 750 mA; I_{ST} = 0 mA V_I = 5.8 V; I_Q = 750 mA; I_{ST} = 0 mA
Turn-OFF voltage	$V_{I\,OFF}$	25	–	–	V	V_I > $V_{I\,off}$
Output current Short-circuit current	I_Q I_{SC}	– 0.75	– 1	20 1.8	mA A	V_I > $V_{I\,off}$ V_Q = 0 V; 6 V ≤ V_I < 13.5 V
Drop voltage	V_{Dr} V_{Dr}	– –	0.3 0.5	0.5 0.75	V V	V_I = 4.5 V; I_Q = 450 mA V_I = 4.5 V; I_Q = 750 mA
Static load regulation	$\Delta V_Q/\Delta I_Q$	–	–	0.2	Ω	6 V ≤ V_I ≤ 16 V 0 mA ≤ – I_Q ≤ 750 mA
Dynamic load regulation	ΔV_Q	–	–	150	mV	I_Q = 75 mA of I_Q = 750 mA C_Q ≥ 50 µF
Supply voltage-rejection	α_{SVR}	60	–	–	dB	I_Q = 750 mA; V_I = 12 V+1 V · cos (2 π × 120 Hz × t);
Reverse output current	$-I_{QR}$	–	5	30	mA	V_I = 0; 0 V ≤ V_Q ≤ 4.85 V
Temperature drift of output voltage	α_{VQ}	– 0.5	–	0.5	mV/K	6 V ≤ V_I ≤ $V_{I\,off}$ ΔT_j > 50 K
Reset Generator						
Switching threshold Switching voltage	V_{RT} V_R V_R	4.4 4.4	4.5 –	4.6 0.8 V_Q	V V V	– V_Q < V_{RT}; I_R = 10 mA V_Q > V_{RT}
Reverse current Change current	I_R I_{ch}	– 10	– –	5 30	µA µA	V_R > 4.6 V; 0.5 V < V_{Cd} < (0.75 × V_Q)
Reset delay time	t_D/C_D	–	175	–	ms/µF	–

Characteristics (cont'd)
V_I = 13.5 V; T_j = 25 °C; V_5 > 3.5 V (unless otherwise specified)

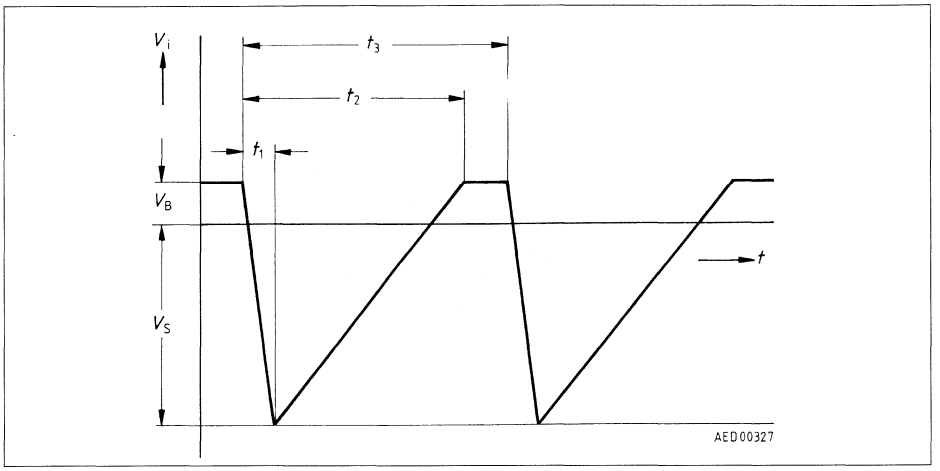
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Standby regulator	–	–	–	–	–	$V_5 \leq 0.5$ V
Output voltage	V_{ST}	4.7	–	5.3	V	0 mA ≤ I_{ST} ≤ 35 mA 6 V ≤ V_I ≤ $V_{I\,off}$
	V_{ST}	4.5	–	6.0	V	0 mA ≤ I_{ST} ≤ 35 mA $V_{I\,off}$ ≤ V_I ≤ 70 V; t_2 ≤ 400 ms
Current consumption without load	I_{QST}	–	–	2	mA	I_Q = 0 mA; I_{ST} = 0 mA
	I_{QST}	–	–	15	mA	I_Q = 0 mA; I_{ST} = 35 mA
Drop voltage	V_{DrST}	–	–	0.75	V	V_I = 4.5 V; I_{ST} = 35 mA
Static load regulation	$\Delta V_{ST}/\Delta I_{ST}$	–	1	–	Ω	6 V ≤ V_I < $V_{I\,off}$ 0 mA ≤ I_{ST} ≤ 35 mA
Supply voltage rejection	$\alpha_{SVR\,ST}$	60	–	–	dB	I_{ST} = 35 mA; V_I = 12 V + 1 V × cos (2 π × 120 Hz × t)
Reverse current	$-I_{ST}$	–	–	2	mA	V_I = 0 V; 0 V ≤ V_{ST} ≤ 4.7 V
General Ratings						
Reverse polarity	$-V_Q$	–	0	0.7	V	V_I = –15 V
	$-I_Q$	–	0	0.5	mA	V_I = –15 V
	$-V_{ST}$	–	0	0.7	V	V_I = –15 V
	$-I_{ST}$	–	0	0.5	mA	V_I = –15 V
Synchronous operation V_{ST}; V_Q	$V_{ST} - V_Q$	– 200	–	200	mV	0 mA ≤ I_{ST} ≤ 35 mA 0 mA ≤ I_Q ≤ 750 mA 6 V ≤ V_I < $V_{I\,off}$
Necessary series resistance	R_5	12	22	24	kΩ	–
Switching threshold for main regulator	V_5	3.5	–	–	V	V_Q > 3 V; I_Q = 0.5 A
	V_5	–	–	0.5	V	V_Q < 3 V; I_Q = 1 mA
Load impedance	R_Q	–	0	2	Ω	$Z_Q = R + (j\,\omega\,C)^{-1}$



Application Circuit

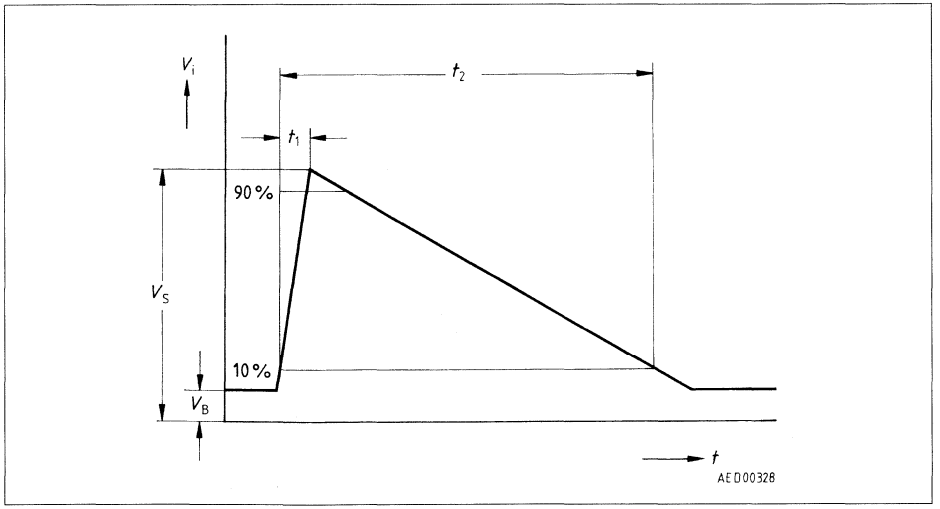


Test Circuit



1. Test Pulse for Negative Interference Voltages V_I

V_B = 14 V t_1 = 10 µs
V_S = 70 V t_2 = 2 ms
R_i = 10 Ω t_3 = 0.5 s to 5 s

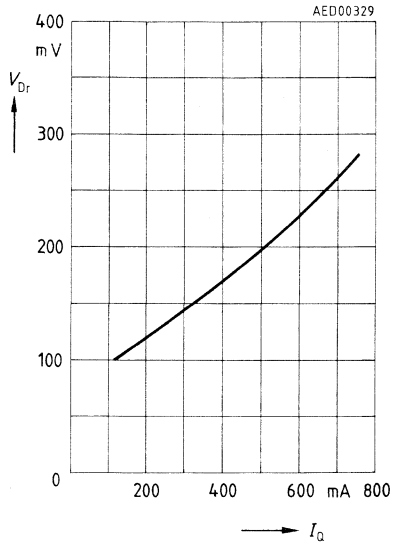


2. Pulse for Load Dump at V_{14}

V_B = 14 V t_1 = 5 ms
V_S = 70 V t_2 = 400 ms
R_i = 0.5 Ω

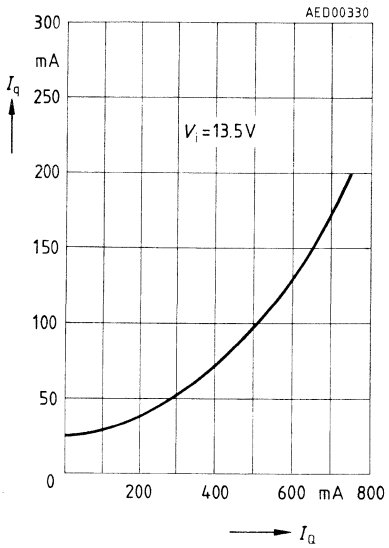
Minimum Drop Voltage versus Output Current

$T_C = 25°C$; $V_i = 4.5$ V



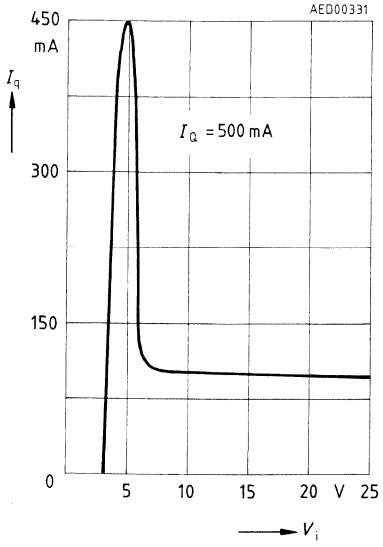
Current Consumption without Load versus Output Current

$T_C = 25°C$



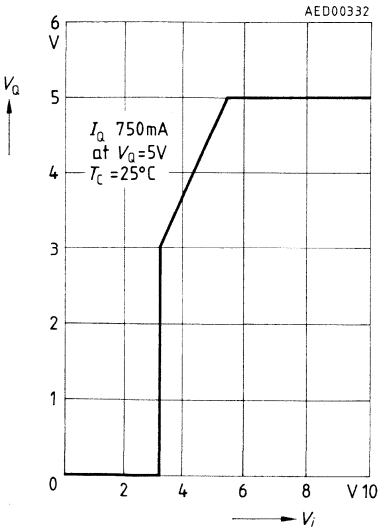
Current Consumption without Load versus Input Voltage

$T_C = 25°C$

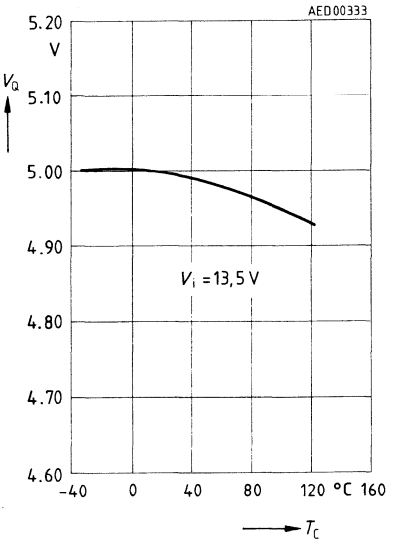


Output Voltage versus Input Voltage

$T_C = 25°C$

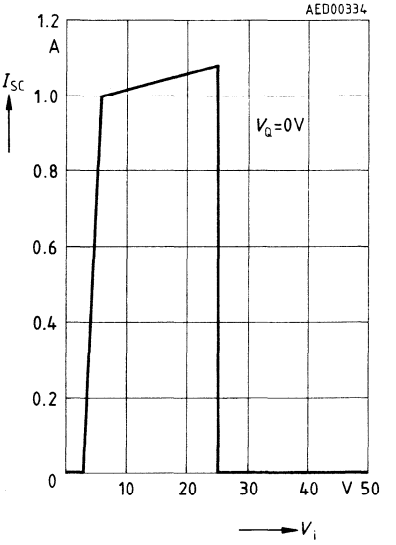


Output Voltage versus Temperature



Short-Circuit Current versus Input Voltage

$T_C = 25°C$



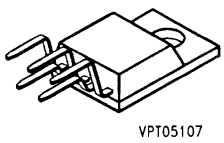
SIEMENS

5-V Low-Drop Voltage Regulator — TLE 4260

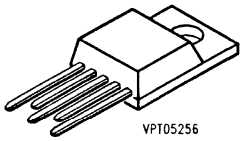
Preliminary Data — **Bipolar IC**

Features

- Low-drop voltage
- Very low quiescent current
- Low starting current consumption
- Integrated temperature protection
- Protection against reverse polarity
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Short-circuit proof
- Suited for automotive electronics
- Wide temperature range
- EMC proofed (100 V/m)



P-TO220-5-1



P-TO220-5-2

	Type	Ordering Code	Package
S	TLE 4260	Q67000-A8187	P-TO220-5-1
▼	TLE 4260 S	Q67000-A9044	P-TO220-5-2

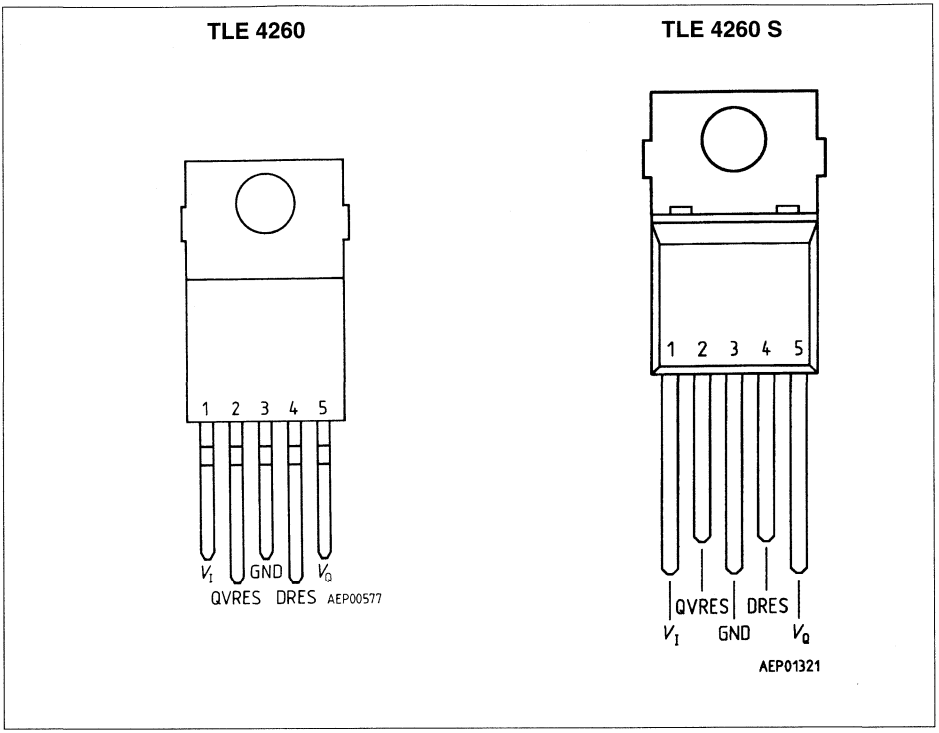
▼ New type

Functional Description

TLE 4260; S is a 5V low-drop fixed-voltage regulator in a P-TO220-5-H/S package. The maximum input voltage is 42 V (65V/≤ 400 ms). The device can produce an output current of more than 500 mA. It is shortcircuit-proof and incorporates temperature protection that disables the circuit at unpermissibly high temperatures.

Due to the wide temperature range of – 40 to 150 °C, the TLE 4260; S is also suitable for use in automotive applications.

The IC regulates an input voltage V_I in the range $6 < V_I < 35$ V to $V_{Qnominal} = 5.0$ V. A reset signal is generated for an output voltage of $V_Q < 4.75$ V. The reset delay can be set externally with a capacitor. If the output current is reduced below 10 mA, the regulator switches internally to standby and the reset generator is turned off. The standby current drops to max. 700 µA.



Pin Configuration
(top view)

Pin Definitions and Functions (TLE 4260 and TLE 4260 S)

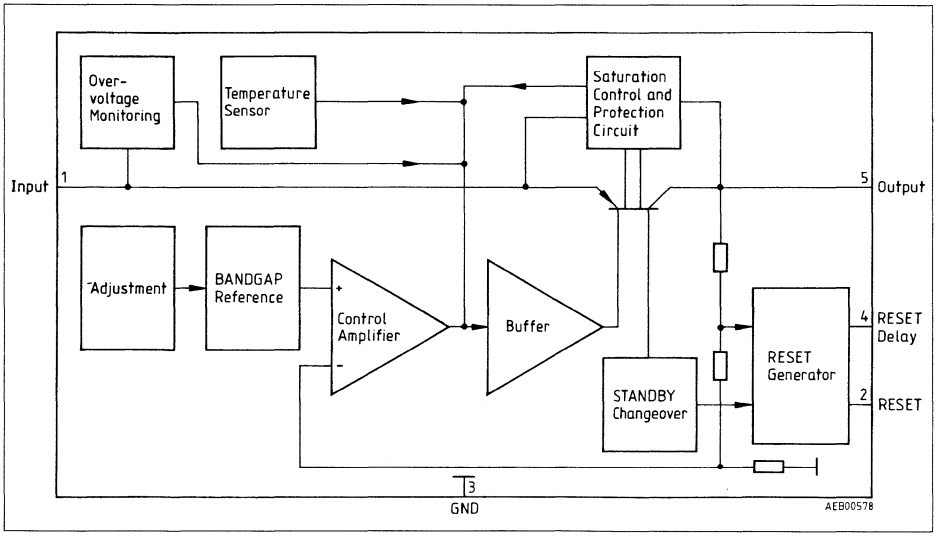
Pin	Symbol	Function
1	V_I	**Input voltage;** block directly to ground on the IC with a 470-nF capacitor
2	QVRES	**Reset output;** open-collector output controlled by the reset delay
3	GND	**Ground**
4	DRES	**Reset delay;** wired to ground with a capacitor
5	V_Q	**5-V output voltage;** block to ground with a 22-µF capacitor

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage goes below 96 % of its typical value, an external capacitor is discharged on pin 4 by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is issued on pin 2 and not cancelled again until the upper threshold V_{DT} is exceeded. For an output current of less than $I_{QN\,Off}$ = 10 mA the standby changeover turns off the reset generator. The latter is turned on again when the output current increases, the output voltage drops below 4.2 V or the delay capacitor is discharged by external measures.

The IC also incorporates a number of internal circuits for protection against:

- overload,
- overvoltage,
- overtemperature,
- reverse polarity.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input (Pin 1)					
Input voltage	V_I	– 42	42	V	–
	V_I	–	65	V	$t \leq 400$ ms
Input current	I_I	–	1.6	A	–
Reset Output (Pin 2)					
Voltage	V_R	– 0.3	42	V	–
Current	I_R	–	–	–	internally limited
Ground (Pin 3)					
Current	I_{GND}	– 0.5	–	A	–
Reset Delay (Pin 4)					
Voltage	V_D	– 0.3	42	V	–
Current	I_D	–	–	–	internally limited
Output (Pin 5)					
Differential voltage	$V_I - V_Q$	– 5.25	V_I	V	–
Current	I_Q	–	1.4	A	–
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Input voltage	V_I	–	32	V	*)
Junction temperature	T_j	– 40	150	°C	–
Thermal resistance					
junction-ambient	$R_{th\,JA}$	–	65	K/W	–
junction - case	$R_{th\,JC}$	–	3	K/W	–

*) **See diagram** "Output Current versus Input Voltage"

Characteristics

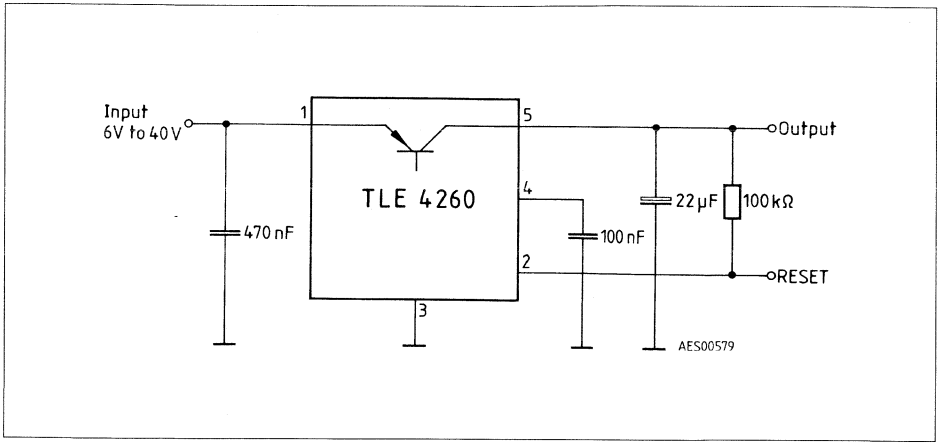
V_I = 13.5 V; T_j = 25 °C (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.75	5.00	5.25	V	25 mA ≤ I_Q ≤ 500 mA 6 V ≤ V_I ≤ 28 V – 40 °C ≤ T_j ≤ 125 °C
Short-circuit current	I_{SC}	500	1000	–	mA	V_I = 17 V to 28 V; V_Q = 0 V
Current consumption; $I_q = I_I - I_Q$	I_q	–	8.5	10	mA*)	6 V ≤ V_I ≤ 28 V; I_Q = 150 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	50	65	mA*)	6 V ≤ V_I ≤ 28 V; I_Q = 500 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	80	mA*)	V_I ≤ 6 V; I_Q = 500 mA
Drop voltage	V_{Dr}	–	0.35	0.5	V	V_I = 4.5 V; I_Q = 0.5 A
Drop voltage	V_{Dr}	–	0.2	0.3	V	V_I = 4.5 V; I_Q = 0.15 A
Load regulation	ΔV_Q	–	15	35	mV	I_Q = 25 mA to 500 mA
Supply-voltage regulation	ΔV_Q	–	15	50	mV	V_I = 6 V to 28 V; I_Q = 100 mA
Supply-voltage regulation	ΔV_Q	–	5	25	mV	V_I = 6 V to 16 V; I_Q = 100 mA
Ripplerejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{pp}
Temperature drift of output voltage*)	α_{VQ}	–	2×10^{-4}	–	1/°C	–
Standby Operation						
Quiescent current; $I_q = I_I - I_Q$	I_q	–	500	700	µA	10 V < V_I < 16 V; I_Q = 0 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	750	850	µA	10 V < V_I < 16 V; I_Q = 5 mA

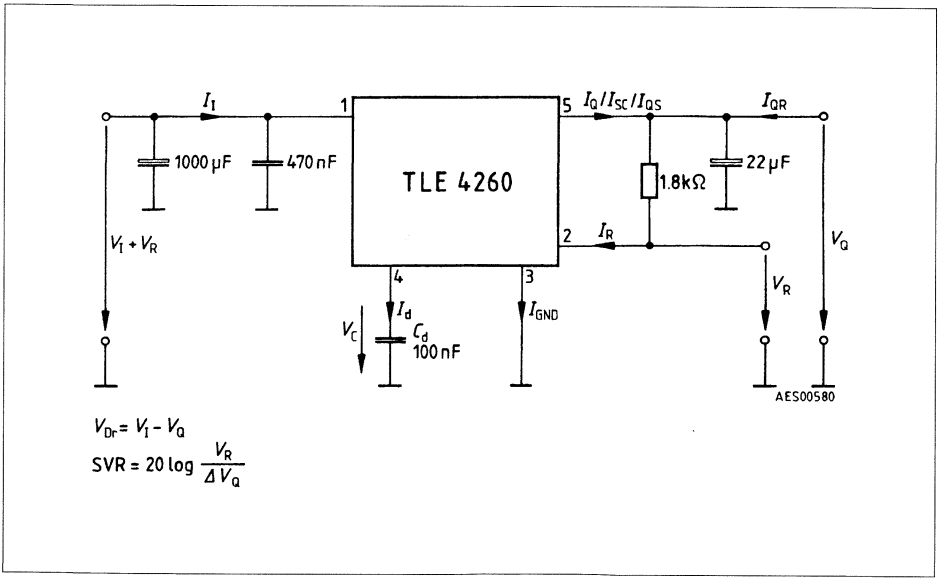
*) **See diagram**

Characteristics (cont'd)
V_I = 13.5 V; T_j = 25 °C (unless specified otherwise)

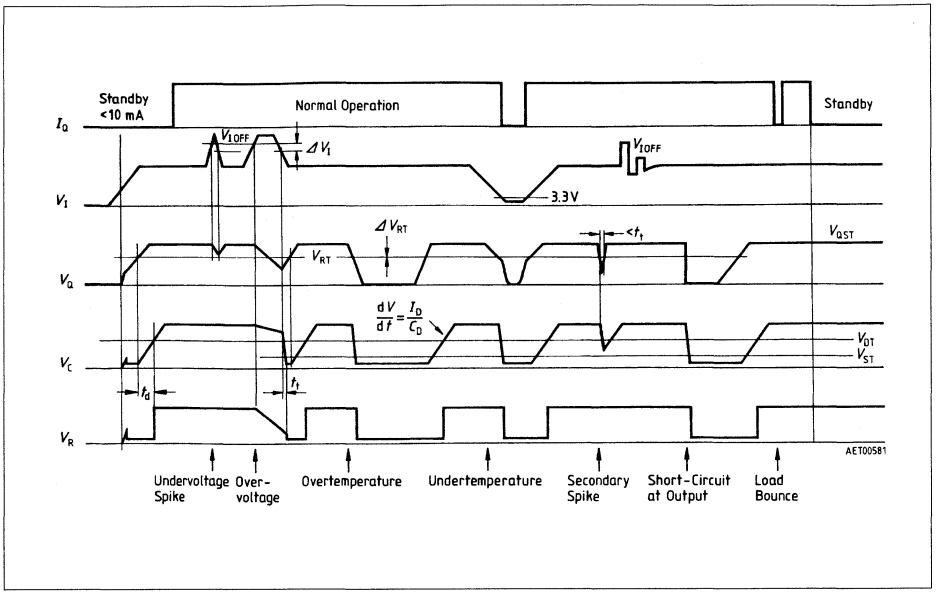
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Standby OFF/Normal ON						
Current consumption	I_{qSOFF}	–	1.0	1.2	mA	**see test diagram**
Current consumption	I_{qNON}	–	1.7	2.2	mA	**see test diagram**
Normal OFF/Standby ON						
Current consumption	I_{qNOFF}	–	1.55	2.00	mA	**see test diagram**
Current consumption	I_{qSON}	–	850	1050	µA	**see test diagram**
Switching threshold	I_{QNOFF}	7.5	10	12.5	mA	**see test diagram**
Switching hysteresis	ΔI_Q	2.25	3	4	mA	**see test diagram**
Reset Generator						
Switching threshold	V_{RT}	94	96	97	%	in % of V_Q I_Q > 500 mA; V_I = 6 V
Switching voltage	V_R	–	0.25	0.40	V	I_R = 3 mA; V_I = 4.5 V
Reverse current	I_R	–	–	1	µA	V_R = 5 V
Charge current	I_D	7	10	13	µA	–
Switching threshold	V_{ST}	0.9	1.1	1.3	V	–
Delay switching threshold	V_{DT}	2.15	2.50	2.75	V	–
Delay time	t_D	–	25	–	ms	C_D = 100 nF
Delay time	t_t	–	5	–	µs	C_D = 100 nF
General Data						
Turn-OFF voltage	V_{IOff}	40	43	45	V	I_Q < 1 mA
Turn-OFF hysteresis	ΔV_I	–	3.0	–	V	–
Leakage current	I_{QS}	–	–	500	µA	V_Q = 0 V; V_I = 45 V
Reverse output current	I_{QR}	–	–	1.5	mA	V_Q = 5 V; V_I = open



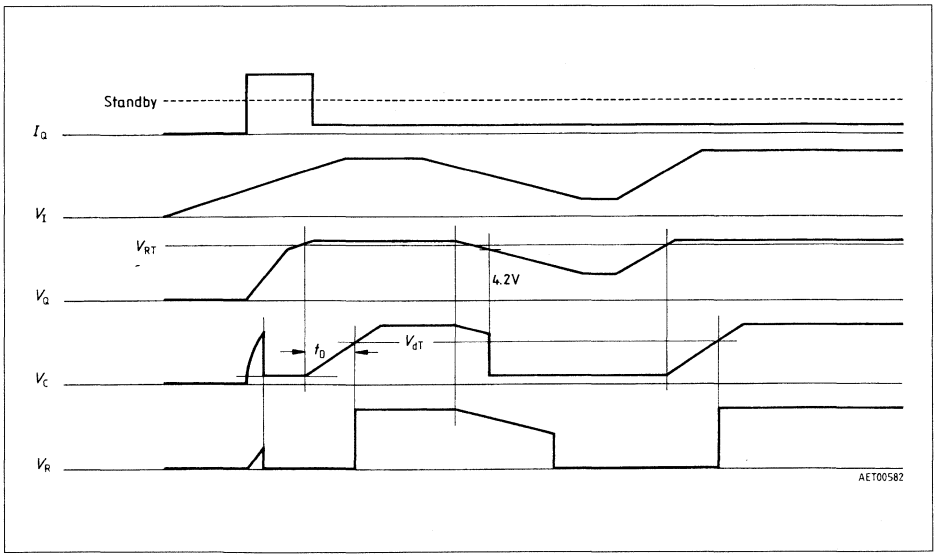
Application Circuit



Test Circuit



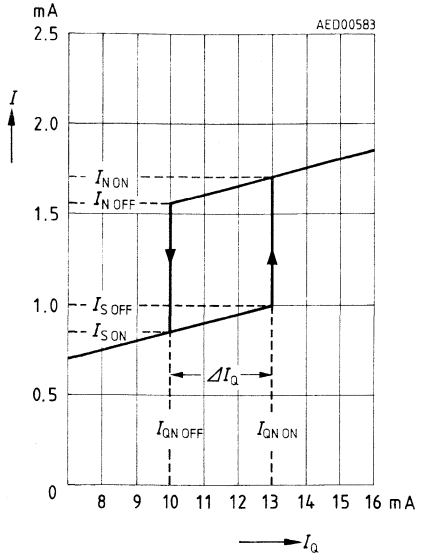
Time Response



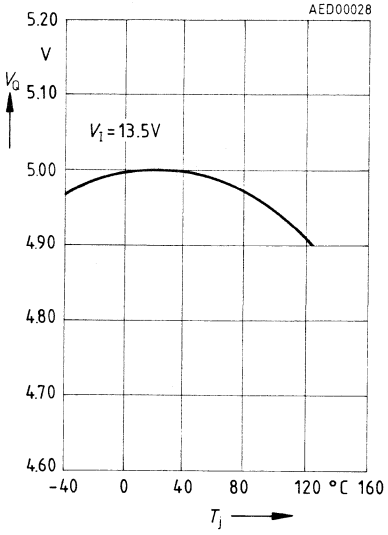
Time Response in Standby Condition

4

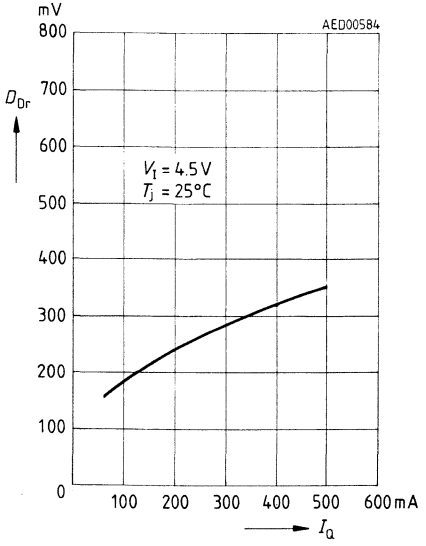
Standby/Normal Changeover



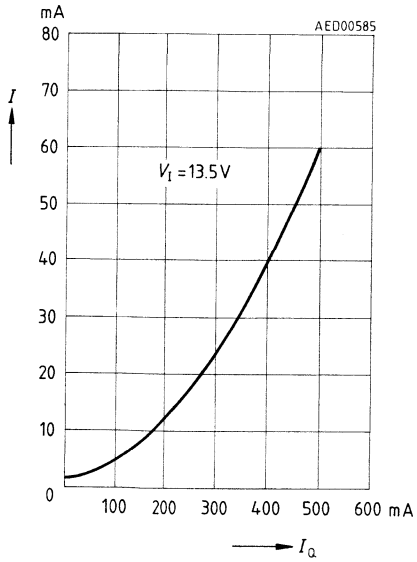
Output Voltage versus Temperature



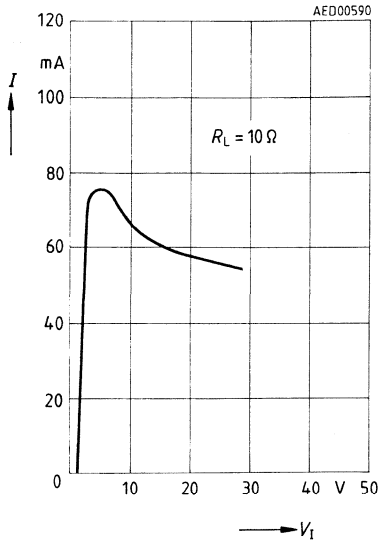
Drop Voltage versus Output Current



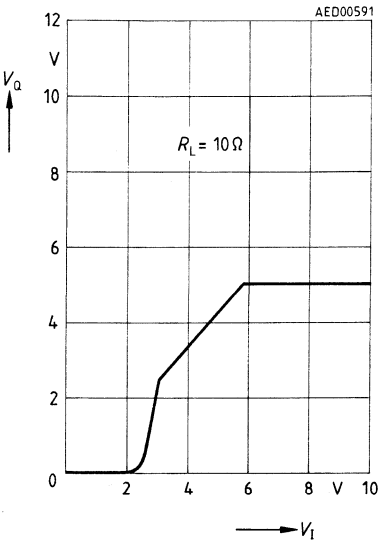
Current Consumption versus Output Current



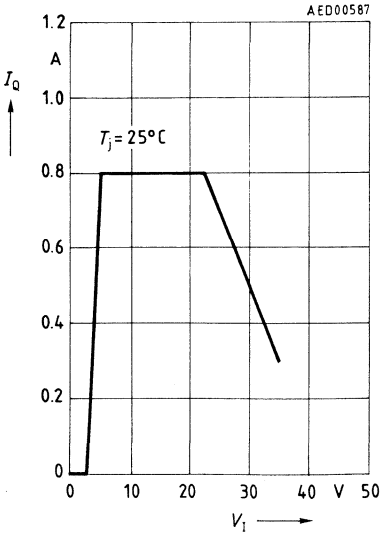
Current Consumption versus Input Voltage



Output Voltage versus Input Voltage



Output Current versus Input Voltage



5-V Low-Drop Voltage Regulator

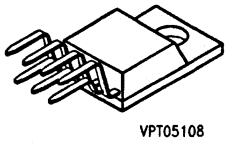
TLE 4261

Preliminary Data

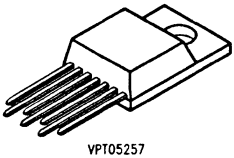
Bipolar IC

Features

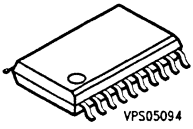
- Very low-drop voltage
- Very low quiescent current
- Low starting-current consumption
- Proof against reverse polarity
- Input voltage up to 42 V
- Overvoltage protection up to 65 V (≤ 400 ms)
- Shortcircuit-proof
- External setting of reset delay
- Integrated watchdog circuit
- Wide temperature range
- Overtemperature protection
- Suitable for automotive use
- EMC proofed (100V/m)



P-TO220-7-1



P-TO220-7-2



P-DSO-20-1

Type	Ordering Code	Package
S TLE 4261	Q67000-A9003	P-TO220-7-1
▼ TLE 4261 S	Q67000-A9109	P-TO220-7-2
▼ TLE 4261 G	Q67000-A9059	P-DSO-20-1 (SMD)

▼ New type

Functional Description

TLE 4261 is a 5V low-drop voltage regulator in a P-T0220-7 or in a P-DSO package. The maximum input voltage is 42 V (65V/≤ 400 ms). The device can produce an output current of more than 500 mA. It is shortcircuit-proof and incorporates temperature protection that disables the circuit at impermissibly high temperatures.

Application Description

The IC regulates an input voltage V_I in the range V_I = 6 to 40 V to V_{Qrated} = 5.0 V. A reset signal is generated for a maximum output voltage of V_Q less than 4.75 V. The reset delay can be set externally with a capacitor. A connected microprocessor is monitored by the integrated watchdog circuit. Connecting this input to the input voltage makes the watchdog function inactive. The presence of a voltage less than 2 V on the inhibit input disables the regulator. The current consumption drops to max. 50 µA.

Design Notes for External Components

The input capacitor C_I causes a low-resistant powerline and limits the rise times of the input voltage. The IC is protected against rise times up to 100 V/µs. It is possible to damp the tuned circuit consisting of supply inductance and input capacitance with a resistor of approx. 1 Ω in series to C_I.

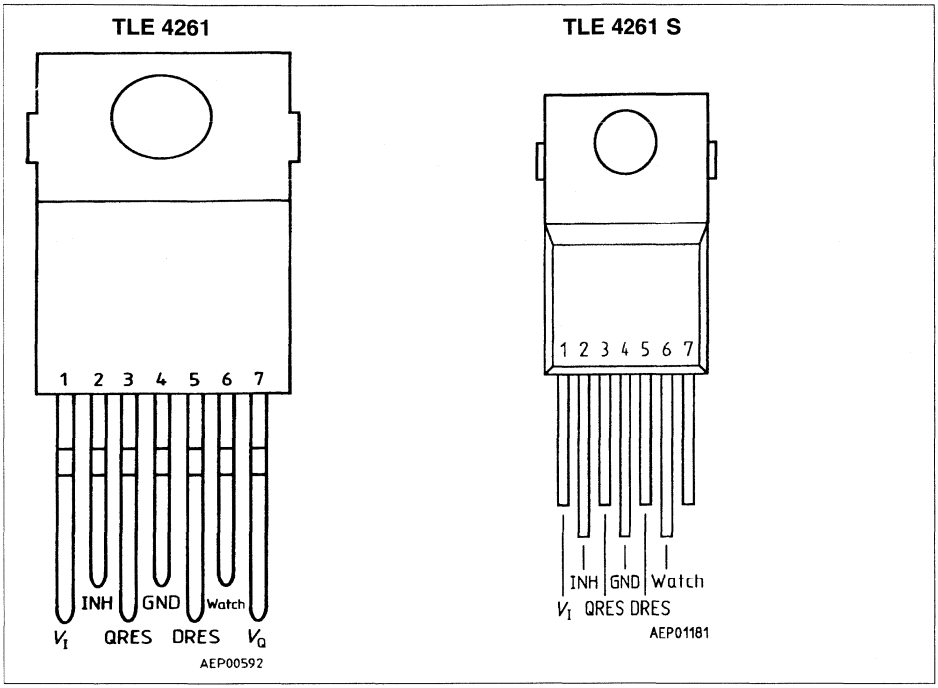
The output capacitor maintains the stability of the regulating loop. Stability is guaranteed with a rating of 22 µF min. at an ESR of 3 Ω max. in the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and controls the base of the series PNP transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the output voltage drops below 95.5 % of its typical value for more than 2 µs, a reset signal is triggered on pin 3 and an external capacitor discharged on pin 5. The reset signal is not cancelled until the voltage on the capacitor has exceeded the upper switching threshold V_{DT}. A positive-edge-triggered watchdog circuit monitors the connected microprocessor and will likewise trigger a reset if pulses are missing. The IC can be disabled by a low level on the inhibit input and the current consumption drops to < 50 µA.

The IC also incorporates a number of circuits for protection against:

- overload,
- overvoltage,
- overtemperature,
- reverse polarity.

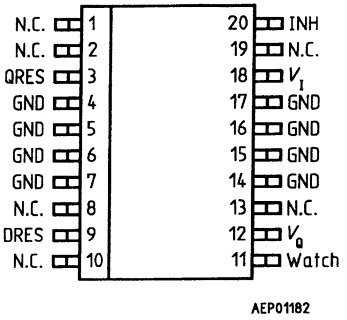


Pin Configuration
(top view)

Pin Definitions and Functions (TLE 4261; S)

Pin	Symbol	Function
1	V_I	**Input voltage**; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vehicle electrical system. Oscillation of the input voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
2	INH	**Inhibit**; switches off the IC when low.
3	QRES	**Reset output**; open-collector output controlled by the reset delay.
4	GND	**Ground**
5	DRES	**Reset delay**; wired to ground using a capacitor.
6	Watch	**Watchdog**; monitors the microprocessor when active.
7	V_Q	**5-V output**; block to ground using a capacitor of ≥ 22 µF. ESR is ≤ 3 Ω in the operating temperature range.

TLE 4261 G

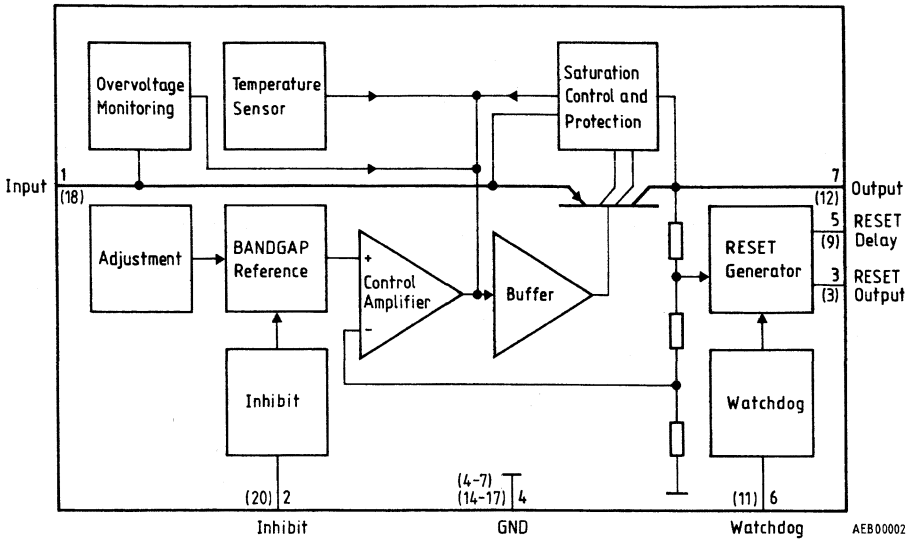


Pin Configuration
(top view)

Pin Definitions and Functions (TLE 4261G)

Pin	Symbol	Function
18	V_I	**Input voltage**; block a capacitor directly to ground on the IC. The capacitor rating will depend on the vehicle electrical system. Oscillation of the input voltage can be damped by a resistor of approx. 1 Ω in series with the input capacitor.
20	INH	**Inhibit**; switches off the IC when low.
3	QRES	**Reset output**; open-collector output controlled by the reset delay.
4 - 7	GND	**Ground**; internally connected with pins 14 to 17.
9	DRES	**Reset delay**; wired to ground using a capacitor.
11	Watch	**Watchdog**; monitors the microprocessor when active.
12	V_Q	**5 V output**; block to ground using a capacitor of ≥ 22 µF. ESR is ≤ 3 Ω in the operating temperature range.

All other pins are not connected.



Numbers in parentheses for TLE 4261 G

Block Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input (pin 1)					
Input voltage	V_I	– 42	42	V	–
Input voltage	V_I	–	65	V	$t \leq 400$ ms
Input current	I_I	–	1.6	A	–
Inhibit (pin 2)					
Voltage	V_2	– 0.3	42	V	–
Current	I_2	–	5	mA	–
Reset Output (pin 3)					
Voltage	V_R	– 0.3	42	V	–
Current	I_R	–	–	–	limited internally
Ground (pin 4)					
Current	I_{GND}	–	0.5	A	–
Reset Delay (pin 5)					
Voltage	V_D	– 0.3	42	V	–
Current	I_D	–	–	–	limited internally
Watchdog (pin 6)					
Voltage	V_W	– 0.3	V_I	V	–
Output (pin 7)					
Differential voltage	$V_I - V_Q$	– 5.25	V_I	V	–
Current	I_Q	–	1.4	A	–
Junction temperature	T_j	–	150	°C	–
Operating Range					
Input voltage	V_I*	–	32	V	–
	V_I	–	–	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal Resistances					
System-air	$R_{th\ SA}$	–	65 (70) 1)	K/W	–
System-case	$R_{th\ SC}$	–	3 (15) 1)	K/W	–

*** See diagram** **1) Figures in parenthesis refer to TLE 4261 G.**

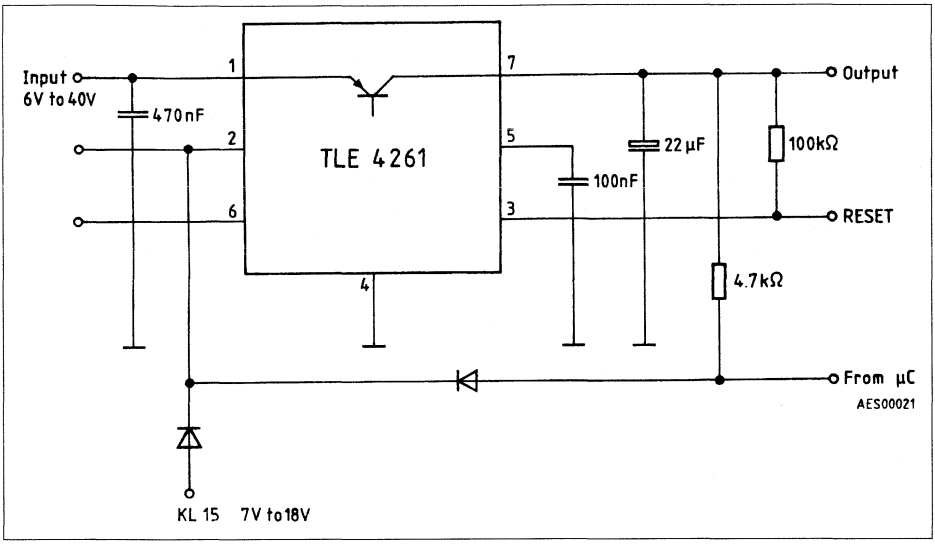
Characteristics

V_I = 13.5 V; T_j = 25 °C; $V_5 \geq 6$ V (unless specified otherwise)

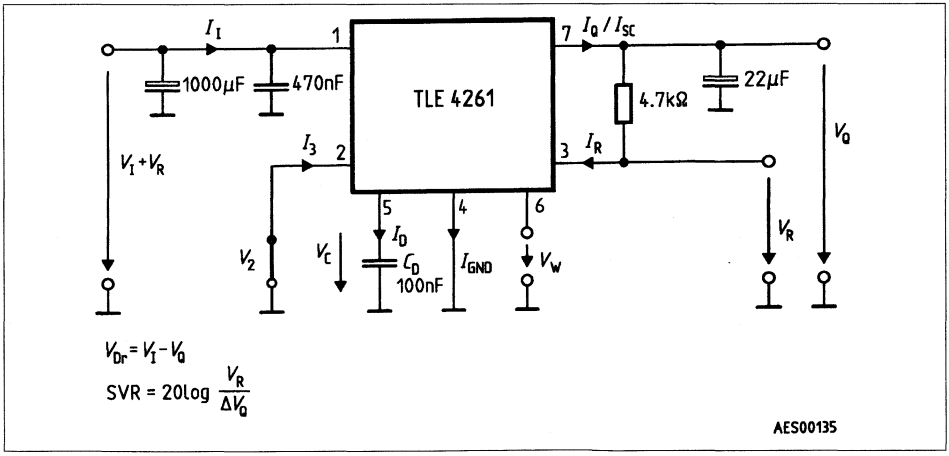
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.75	5.00	5.25	V	25 mA ≤ I_Q ≤ 500 mA; 6 V ≤ V_I ≤ 28 V; – 40 °C ≤ T_j ≤ 125 °C
Output voltage	V_Q	4.85	5.00	5.15	V	25 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 40 V
Output current	I_Q	–	–	50	µA	0 V ≤ V_I ≤ 2 V; $V_2 = V_I$; – 40 °C ≤ T_j ≤ 125 °C
Output current	I_Q	500	1000	–	mA	V_I = 17 V to 28 V
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	3.5	mA	I_Q = 0; V_W > 6V
Current consumption; $I_q = I_I - I_Q$	I_q	–	5.0	10	mA	6 V ≤ V_I ≤ 28 V; I_Q = 150 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	40	65	mA	6 V ≤ V_I ≤ 28 V; I_Q = 500 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	45	80	mA	V_I < 6 V; I_Q ≤ 500 mA
Drop voltage	V_{Dr}	–	0.35	0.5	V	V_I = 4.5 V; I_Q = 0.5 A
Drop voltage	V_{Dr}	–	0.2	0.3	V	V_I = 4.5 V; I_Q = 0.15 A
Load regulation	ΔV_Q	–	15	35	mV	25 mA ≤ I_Q ≤ 500 mA
Supply voltage regulation	ΔV_Q	–	15	50	mV	6 V ≤ V_I ≤ 28 V I_Q = 100 mA
Supply voltage regulation	ΔV_Q	–	5	25	mV	6 V ≤ V_I ≤ 16 V I_Q = 100 mA
Ripple rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{pp}
Temperature drift of output voltage	α_{VQ}	–	2×10^{-4}	–	1/°C	– 40 °C < T_j < 150 °C
Inhibit Operation						
Current consumption	I_I	–	–	50	µA	V_2 < 2 V; I_Q = 0
Current consumption	I_2	–	–	100	µA	V_2 = 6 V
Switching threshold for inhibit	V_2	5.0	5.5	6.0	V	IC turned ON
Switching threshold for inhibit	V_2	2.0	2.7	3.7	V	IC turned OFF

Characteristics (cont'd)
V_I = 13.5 V; T_j = 25 °C; $V_2 \geq 6$ V (unless specified otherwise)

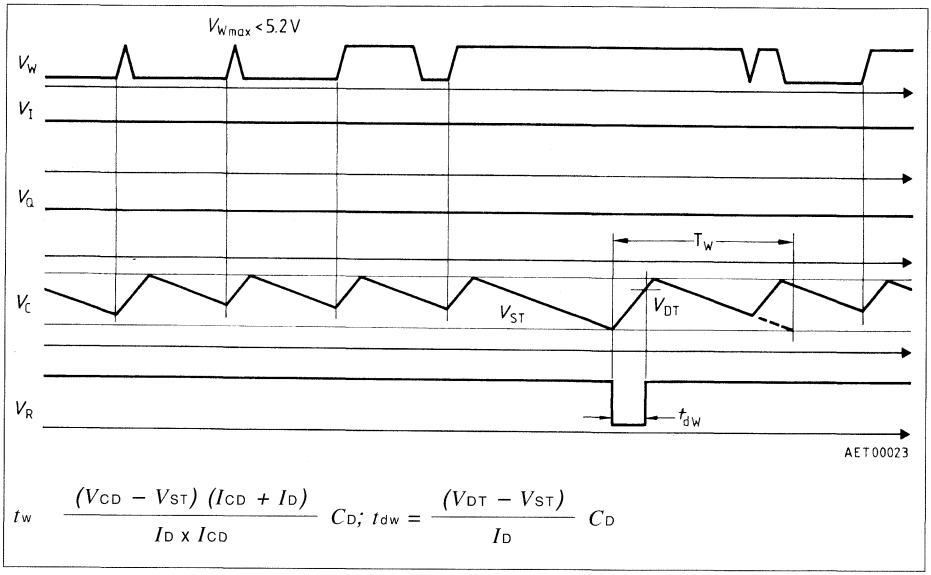
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reset Generator						
Switching threshold	V_{RT}	94	95.5	97	%	in % of V_Q I_Q > 500 mA; V_I = 6 V
Saturation voltage, reset output	V_R	–	0.25	0.40	V	I_R = 1 mA
Reverse current	I_R	–	–	1	µA	V_R = 5 V
Charge current	I_d	18.75	25	31.25	µA	V_C = 1.5 V
Switching threshold	V_{ST}	0.9	1	1.1	V	–
Delay switching threshold	V_{DT}	2.25	2.50	2.75	V	–
Saturation voltage, delay output	V_C	–	–	100	mV	V_I = 4.5 V and I_d
Delay time	t_D	–	10	–	ms	C_D = 100 nF
Delay time	t_1	–	2	–	µs	–
Watchdog						
Turn-OFF voltage	V_W	5.2	5.6	6.0	V	–
Discharge current	I_{CD}	5.6	7.5	9.4	µA	V_C = 1.5 V
Switching voltage	V_{CD}	2.95	3.05	3.15	V	–
Pulse interval	T_W	–	35	–	ms	C_D = 100 nF
General Data						
Turn-OFF voltage	V_{IOFF}	41	43	45	V	I_Q < 1 mA
Turn-OFF hysteresis	ΔV_I	–	6.5	–	V	–
Leakage current	I_{QS}	–	–	50	µA	V_Q = 0 V; V_I = 45 V
Reverse output current	I_{QR}	–	–	1.5	mA	V_Q = 5 V; V_I and V_2 open



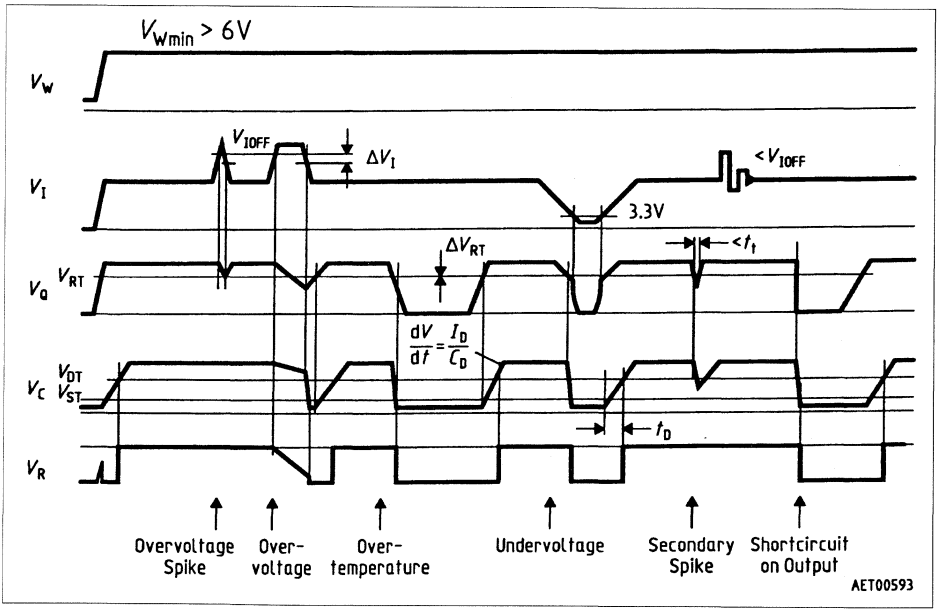
Application Circuit



Test Circuit



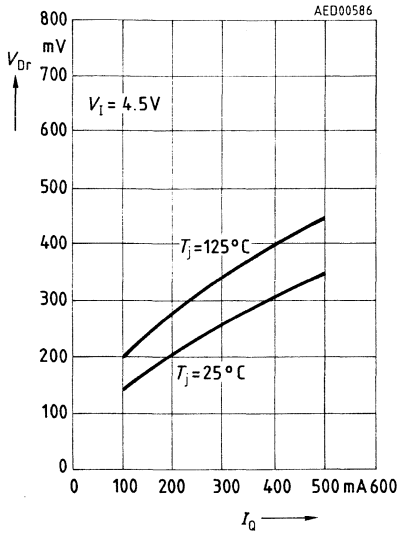
Time Response in Watchdog Condition



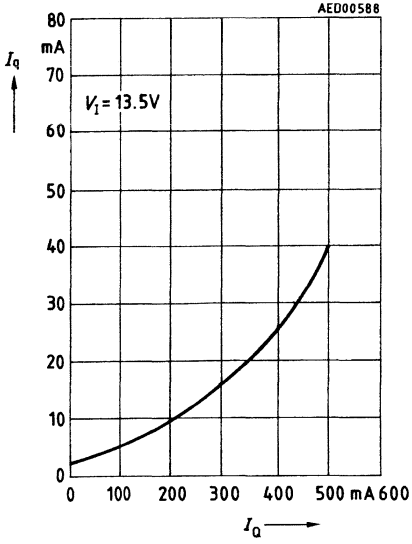
Timing with Watchdog OFF

4

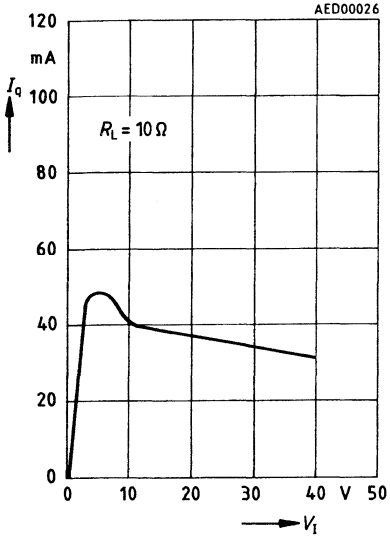
Drop Voltage versus Output Current



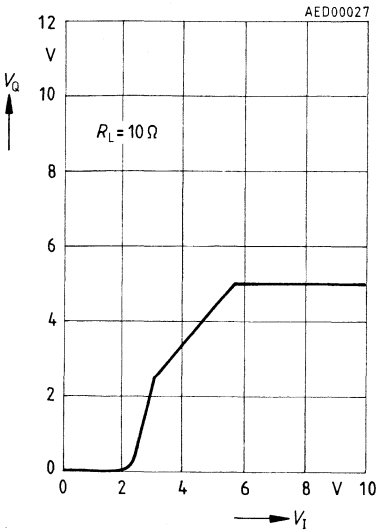
Current Consumption versus Output Current



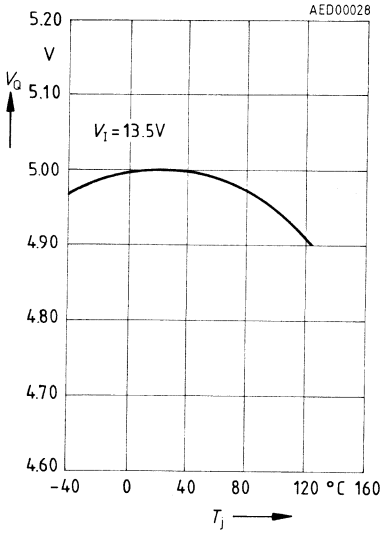
Current Consumption versus Input Voltage



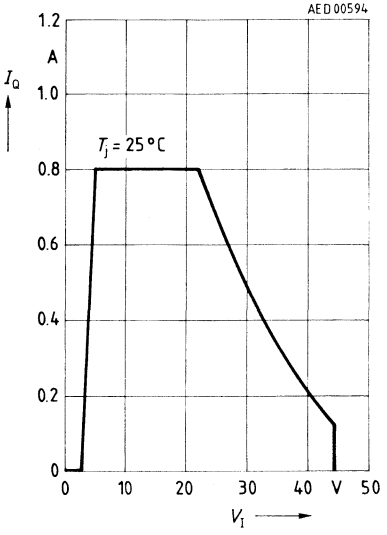
Output Voltage versus Input Voltage



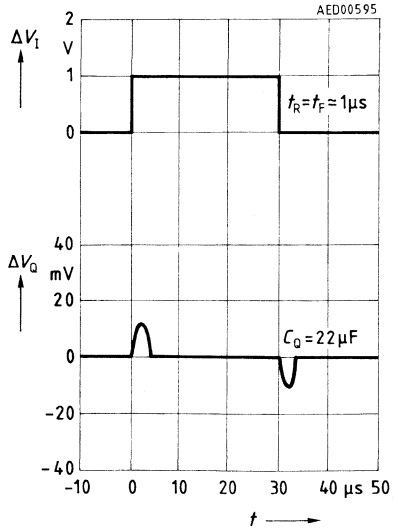
Output Voltage versus Temperature



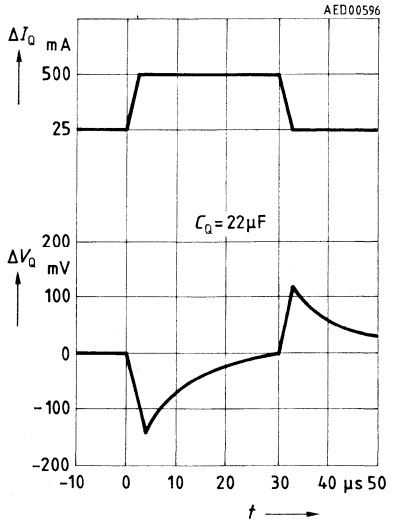
Output Current versus Input Voltage



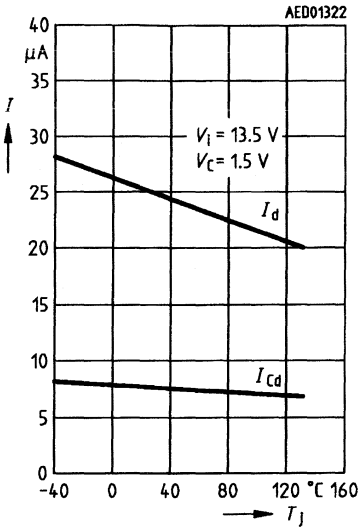
Input Step Response



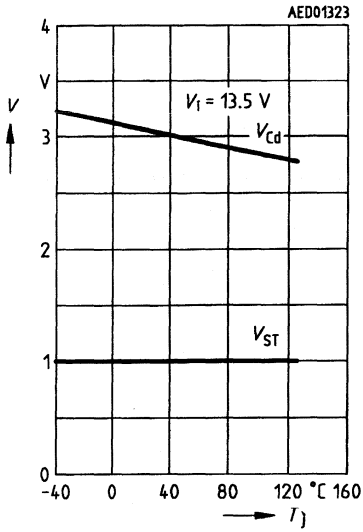
Load Step Response



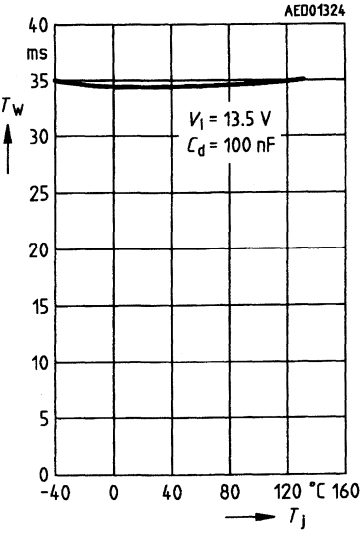
Charge Current I_D and Discharge Current I_{CD} versus Temperature



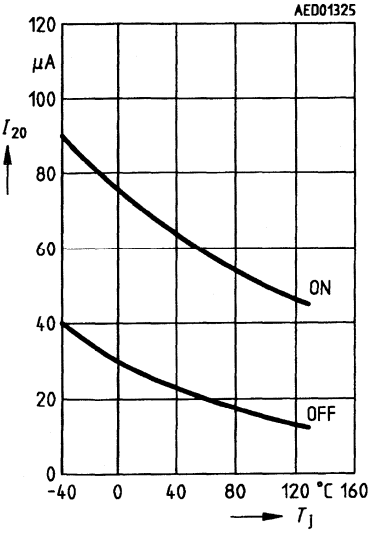
Switching Voltage V_{CD} and V_{ST} versus Temperature



Pulse Interval T_W versus Temperature



Current Consumption of Inhibit at the Switching Point Versus Temperature



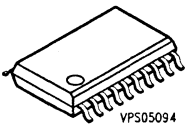
SIEMENS

5-V Low-Drop Voltage Regulator — TLE 4262

Preliminary Data — **Bipolar IC**

Features

- Output voltage tolerance $\leq \pm 2$ %
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Settable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics



P-DSO-20-1

Type	Ordering Code	Package
TLE 4262 G	Q67000-A9068	P-DSO-20-1 (SMD)

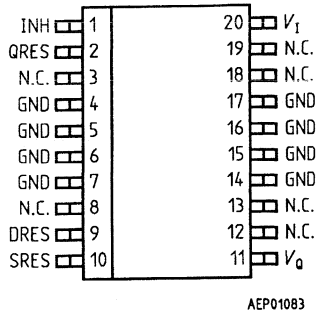
Functional Description

TLE 4262 G is a 5V low-drop voltage regulator in a P-DSO-20-1 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is shortcircuit-proof and incorporates temperature protection that disables the IC at overtemperature.

The IC regulates an input voltage V_I in the range of 6 V < V_I < 45 V to $V_{Q\text{rated}}$ = 5.0 V. A reset signal is generated for an output voltage of V_Q < 4.5 V. This voltage threshold can be decreased to 3.5V by external connection. The reset delay can be set externally with a capacitor. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 720 µA to < 50 µA.

Dimensioning Information on External Components

The input capacitor C_I is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay, the spread of the capacitance of the delay capacitor and its temperature coefficent should be noted.



Pin Configuration
(top view)

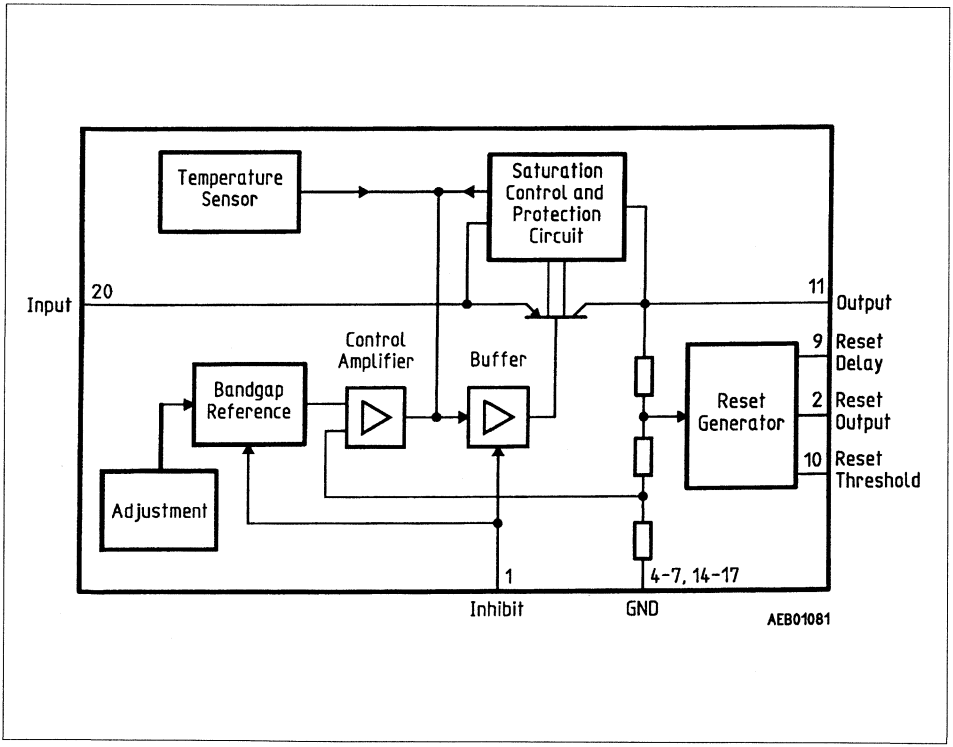
Pin Definitions and Functions

Pin	Symbol	Function
1	INH	**Inhibit;** TTL-kompatible, low-active input
2	QRES	**Reset output;** open-collector output internally connected to the output via a resistor of 30 kΩ.
4 - 7, 14 - 17	GND	**Ground**
9	DRES	**Reset delay;** connected to ground by a capacitor
10	SRES	**Reset threshold;** for setting the switching threshold connect by a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
11	V_Q	**5-V output voltage;** block to ground by a 22 µF capacitor
20	V_I	**Input voltage;** block to ground directly at the IC by a ceramic capacitor.
3, 8, 12, 13, 18,19	N.C.	Not connected

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is issued on the reset output and not cancelled again until the upper threshold V_{dT} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. The IC can be switched at the TTL compatible, low-active inhibit input. It also incorporates a number of internal circuits for protection against:

- Overload,
- Overtemperature,
- Reverse polarity.



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input					
Input voltage	V_I	– 42	45	V	–
Input current	I_I	–	–	–	internally limited
Reset Output					
Voltage	V_R	– 0.3	42	V	–
Current	I_R	–	–	–	internally limited
Reset Input					
Reset threshold	V_{RE}	–	–	–	–
Reset Delay					
Voltage	V_d	– 0.3	42	V	–
Current	I_d	–	–	–	internally limited
Output					
Voltage	V_Q	– 5.25	V_I	V	–
Current	I_Q	–	–	–	internally limited
Inhibit					
Voltage	V_e	– 42	45	V	–
Ground					
Current	I_{GND}	– 0.5	–	A	–
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Operating Range

Input voltage	V_I	5.2	45	V	*)
Junction temperature	T_j	– 40	150	°C	–
Thermal resistance					
junction-ambient	$R_{th\,JA}$	–	70	K/W	soldered
junction - case	$R_{th\,JC}$	–	25	K/W	–

*) Corresponds with characteristics of drop voltage, output current and power description **(see Diagrams)**.

Characteristics

V_I = 13.5 V; T_j = 25 °C; V_e > 3.5 V; (unless specified otherwise)

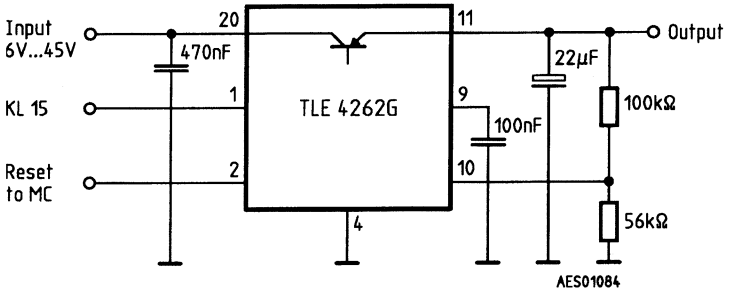
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.9	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V; – 40 °C ≤ T_j ≤ 125 °C
Output voltage	V_Q	4.95	5.00	5.05	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA
Output current limiting	I_Q	200	250		mA	–
Current consumption; $I_q = I_i - I_Q$	I_q	–	–	50	µA	V_e < 0.8 V
	I_q	–	720	–	µA	I_Q = 0 mA
	I_q	–	10	15	mA	I_Q = 150 mA
	I_q	–	15	20	mA	I_Q = 150 mA, V_i = 4.5 V
Drop voltage	V_{Dr}	–	0.35	0.6	V	I_Q = 150 mA *)
Load regulation	ΔV_Q	–	–	25	mV	I_Q = 5 mA to 150 mA
Supply-voltage regulation	ΔV_Q	–	15	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
Ripple rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Reset Generator						
Switching threshold	V_{RT}	4.2	4.5	4.8	V	V_{RE} = 0 V
Switching voltage	V_{RE}	1.28	1.35	1.42	V	V_Q > 3.5 V
Saturation voltage	V_R	–	0.10	0.40	V	I_R = 1 mA
Saturation voltage	V_C	–	50	100	mV	V_Q < V_{RT}
Charge current	I_d	7	10	14	µA	–
Delay switching thresh.	V_{dT}	1.5	1.7	2.1	V	–
Switching threshold	V_{ST}	0.2	0.35	0.55	V	–
Delay time	t_D	–	17	–	ms	C_d = 100 nF
Delay time	t_t	–	2	–	µs	C_d = 100 nF

*) Drop voltage $V_I \geq$ 4.5 V; drop voltage = $V_I - V_Q$ (below regulating range)

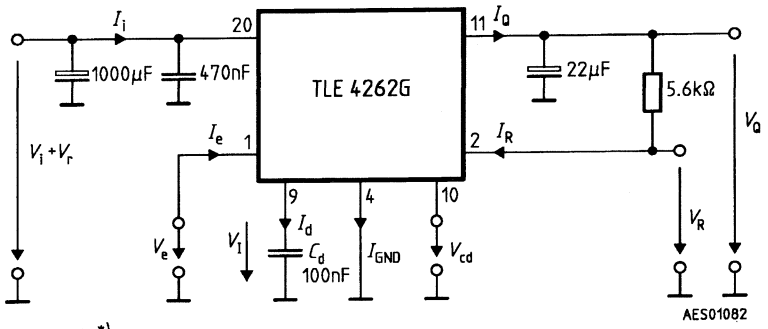
Note: The reset output is low within the range V_Q = 1 V to V_{RT}.

Characteristics (cont'd)
V_I = 13.5 V; T_j = 25 °C (unless specified otherwise)

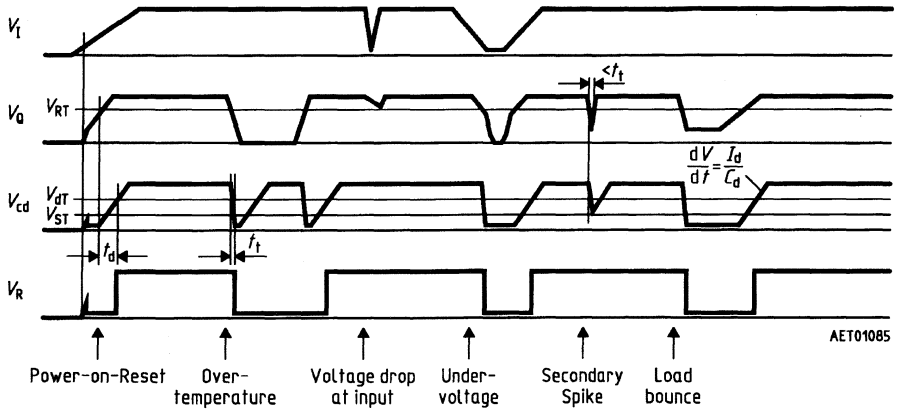
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inhibit						
Switch-ON voltage	$V_{e\,ON}$	3.5	–	–	V	IC turned on
Switch-OFF voltage	$V_{e\,OFF}$	–	–	0.8	V	IC turned off
Input current	I_e	5	10	15	µA	V_e = 5 V



Application Circuit

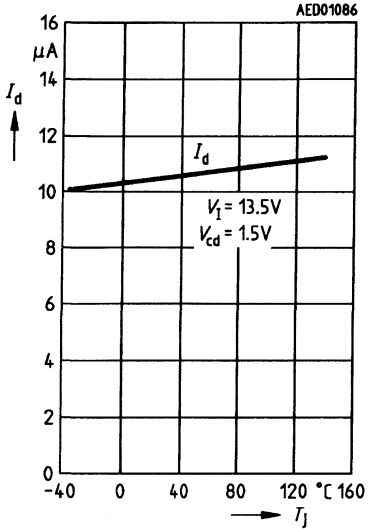


Test Circuit

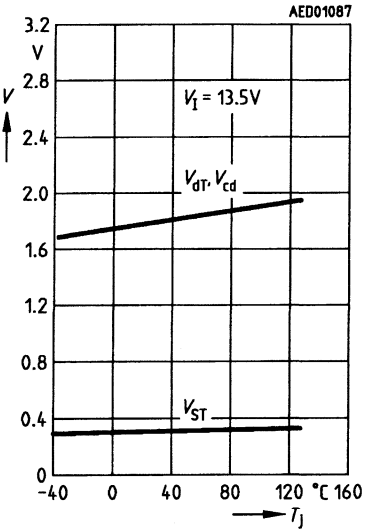


Time Response

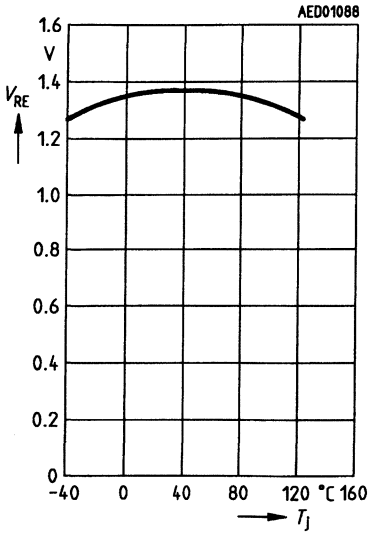
Charge Current versus Temperature



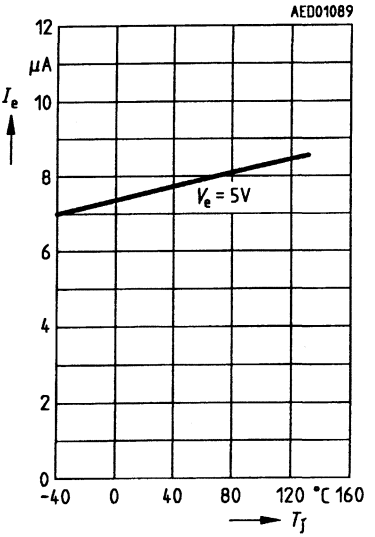
Switching Voltage V_{dT} and V_{ST} versus Temperature



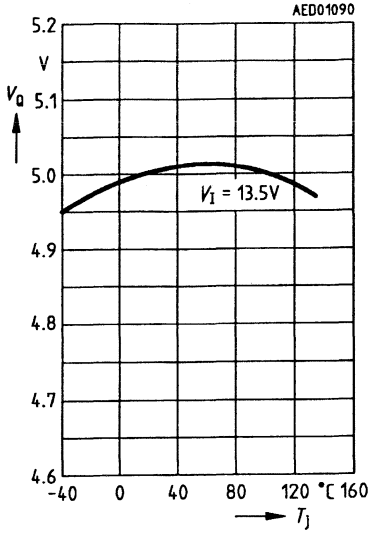
Reset Switching Threshold versus Temperature



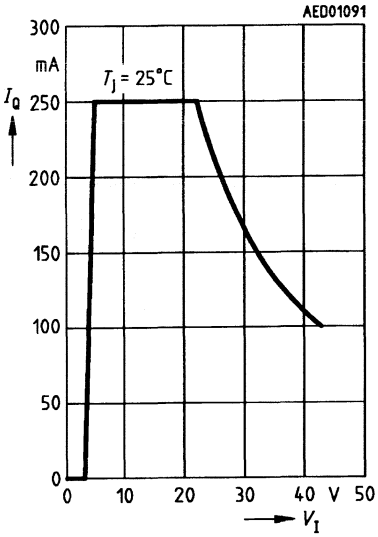
Current Consumption of Inhibit versus Temperature Output Current



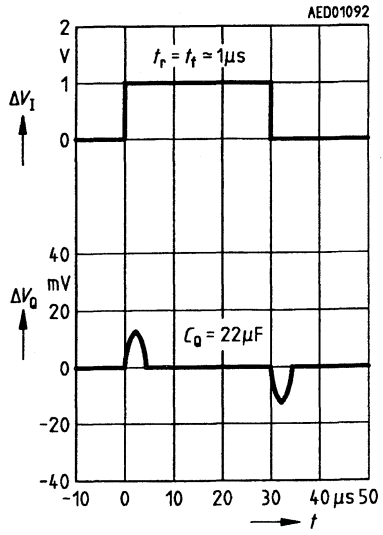
Output Voltage versus Temperature



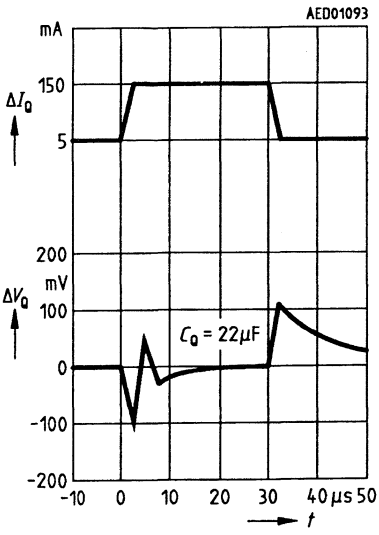
Output Current versus Input Voltage



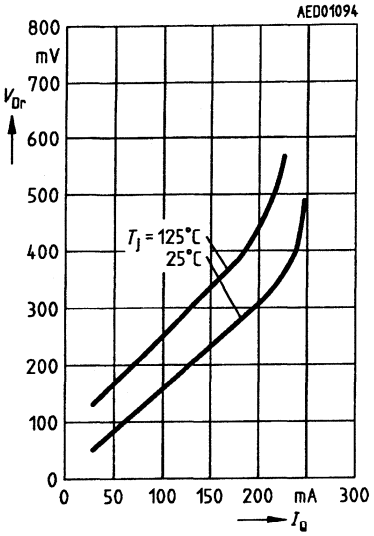
Input Response



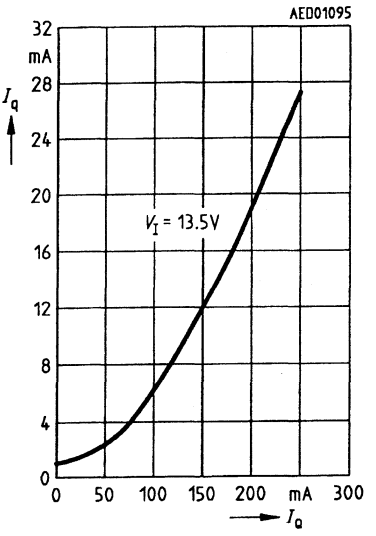
Load Response



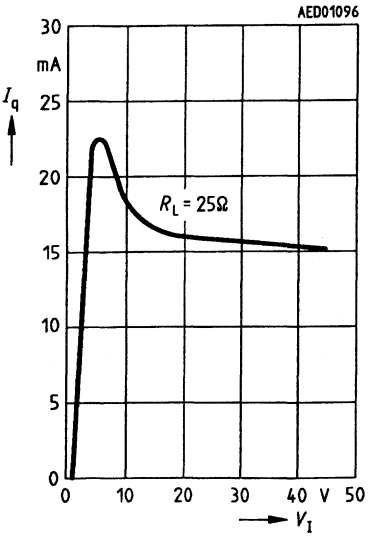
Drop Voltage versus Output Current



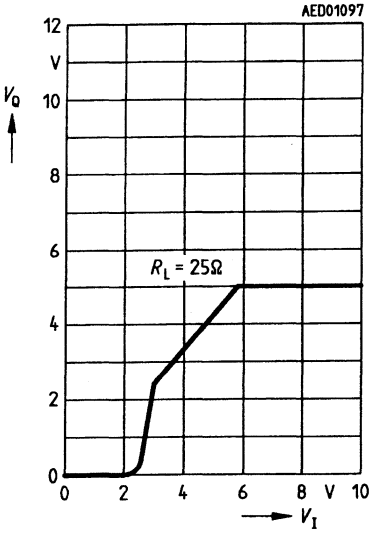
Current Consumption versus Output Current



Current Consumption versus Input Voltage



Output Voltage versus Input Voltage



SIEMENS

5-V Low-Drop Voltage Regulator

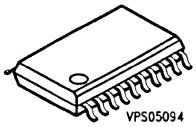
TLE 4263

Preliminary Data

Bipolar IC

Features

- Output voltage tolerance ≤ ± 2%
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Settable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics



P-DSO-20-1

Type	Ordering Code	Package
TLE 4263 G	Q67000-A9095	P-DSO-20-1 (SMD)

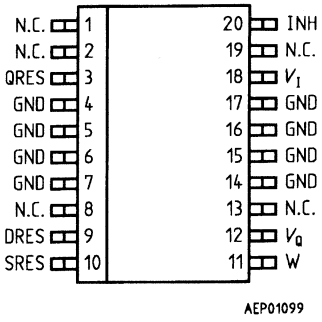
Functional Description

TLE 4263 G is a 5V low-drop voltage regulator in a P-DSO-20-1 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200mA. The IC is shortcircuit-proof and incorporates temperature protection that disables the IC at overtemperature.

The IC regulates an input voltage V_I in the range of 6 V < V_I < 45 V to V_{Qrated} = 5.0 V. A reset signal is generated for an output voltage of V_Q < 4.5 V. This voltage threshold can be decreased to 3.5V by external connection. The reset delay can be set externally by a capacitor. The integrated watchdog logic controls the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 800 µA to < 50 µA.

Dimensioning Information on External Components

The input capacitor C_I is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficent should be noted.



Pin Configuration
(top view)

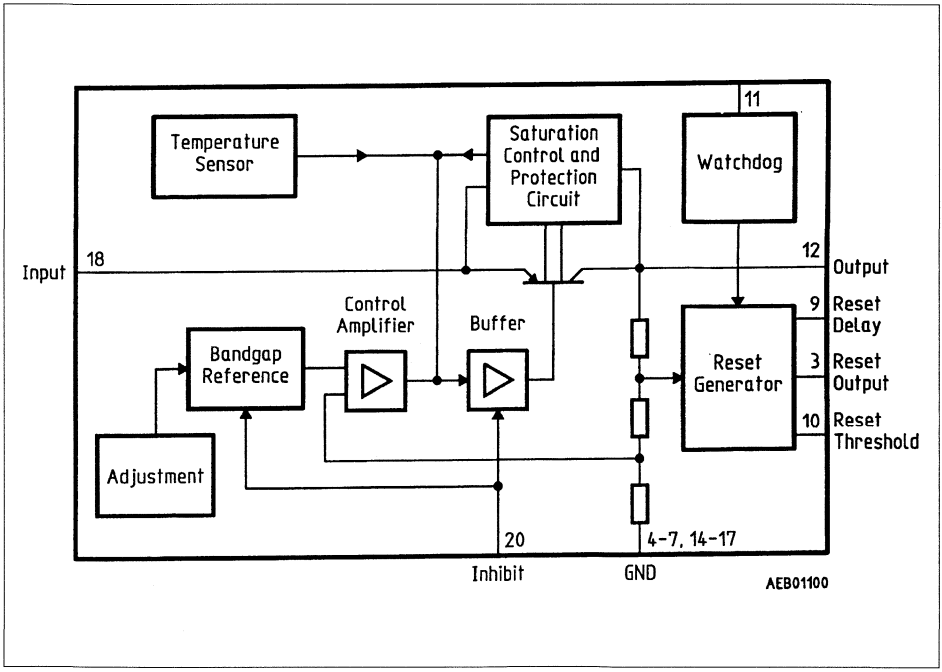
Pin Definitions and Functions

Pin	Symbol	Function
1,2,19,13	N.C.	Not connected
3	QRES	**Reset output;** open-collector output connected to the output via a resistor of 30 kΩ.
4 - 7, 14 - 17	GND	**Ground**
9	DRES	**Reset delay;** connect to ground with a capacitor
10	SRES	**Reset threshold;** for setting the switching threshold connect with a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
11	W	**Watchdog;** positive edge triggered input for monitoring a mirocontroller
12	V_Q	**5-V output voltage;** block to ground with a 22-µF capacitor
18	V_I	**Input voltage;** block to ground directly at the IC with a ceramic capacitor
20	INH	**Inhibit;** TTL-kompatible, low-active input

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold V_{ST}, a reset signal is issued on the reset output and not cancelled again until the upper threshold V_{dT} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. A connected microcontroller is controlled by the watchdog logic. If pulses are missing, the reset output is set to low. The pulse sequence time can be set within a wide range with the reset delay capacitor. The IC can be switched at the TTL compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against:

- Overload,
- Overtemperature,
- Reverse polarity.



Block Diagram

Absolute Maximum Ratings
T_j = - 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input					
Input voltage	V_I	– 42	45	V	–
Input current	I_I	–	–	–	internally limited
Reset Output					
Voltage	V_R	– 0.3	42	V	–
Current	I_R	–	–	–	internally limited
Reset Input					
Reset threshold	V_{RE}	– 0.3	6	V	–
Reset Delay					
Voltage	V_D	– 0.3	42	V	–
Current	I_D	–	–	–	internally limited
Output					
Voltage	V_Q	– 0.3	7	V	–
Current	I_Q	–	–	–	internally limited
Inhibit					
Voltage	V_e	– 42	45	V	–
Watchdog					
Voltage	V_W	– 0.3	6	V	–
Ground					
Current	I_{GND}	– 0.5	–	A	–
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	
Operating Range					
Input voltage	V_I	–	45	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal resistance					
junction-ambient	$R_{th\,JA}$	–	70	K/W	soldered
junction - case	$R_{th\,JC}$	–	25	K/W	–

Characteristics

V_I = 13.5 V; T_j = 25 °C; V_e > 3.5 V; (unless specified otherwise)

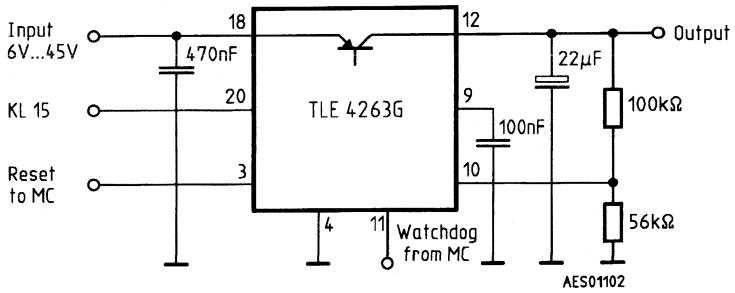
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V; – 40 °C ≤ T_j ≤ 125 °C
Output voltage	V_Q	4.95	5.00	5.05	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA T_j = 125 °C
Output current	I_Q	200	250	–	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	–	50	µA	V_e = 0
	I_q	–	800	1100	µA	I_Q = 0 mA
	I_q	–	10	15	mA	I_Q = 150 mA
	I_q	–	15	20	mA	I_Q = 150 mA, V_i = 4.5 V
Drop voltage	V_{Dr}	–	0.35	0.6	V	I_Q = 150 mA *)
Load regulation	ΔV_Q	–	–	25	mV	I_Q = 5 mA to 150 mA
Supply-voltage regulation	ΔV_Q	–	15	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
Ripple rejection	SVR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Reset Generator						
Switching threshold	V_{RT}	4.2	4.5	4.8	V	V_{RE} = 0 V
Switching voltage	V_{RE}	1.28	1.35	1.42	V	V_Q > 3.5 V;
Reset low voltage	V_R	–	0.10	0.40	V	I_R = 1 mA
Saturation voltage	V_C	–	50	100	mV	V_Q < V_{RT}
Delay switching thresh.	V_{dT}	1.5	1.7	2.1	V	–
Switching threshold	V_{ST}	0.2	0.35	0.55	V	–
Charge current	I_d	40	60	80	µA	–
Delay time	t_d	–	2.8	–	ms	C_d = 100 nF
Delay time	t_t	–	2	–	µs	C_d = 100 nF

Note: The reset output is low within the range V_Q = 1V to V_{RT}

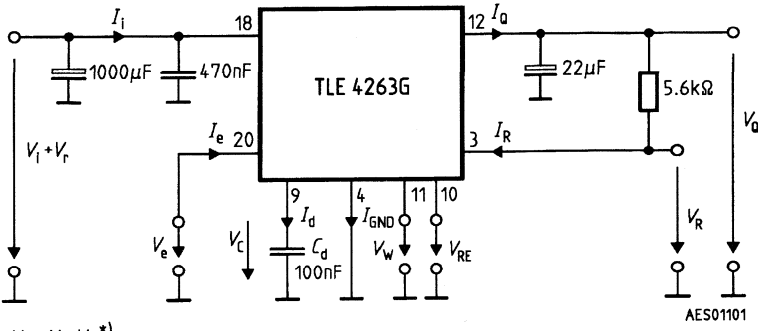
*) Drop voltage = V_i - V_Q (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Characteristics (cont'd)
V_I = 13.5 V; T_j = 25 °C (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog						
Discharge current	I_{Cd}	4.4	6.25	8.2	µA	V_C = 1.5 V
Switching voltage	V_{Cd}	1.5	1.7	2.1	V	–
Pulse time	T_W	–	22.5	–	ms	C_d = 100 nF
Inhibit						
Switching voltage	V_{eON}	3.5	–	–	V	IC turned on
Turn-OFF voltage	V_{eOFF}	–	–	0.8	V	IC turned off
Input current	I_e	5	10	15	µA	V_e = 5 V



Application Circuit

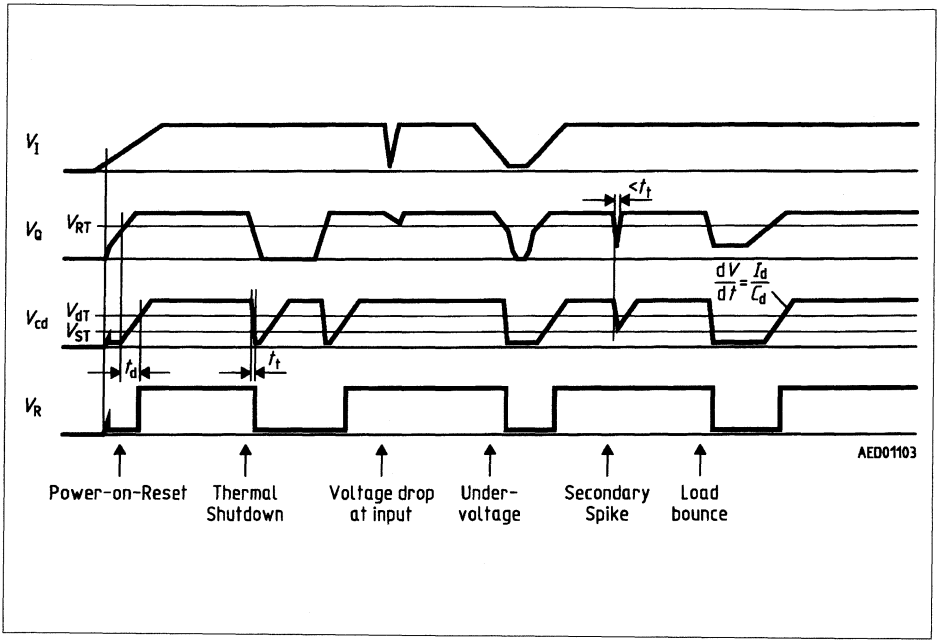


$V_{Dr} = V_I - V_Q$ *)

$SVR = 20\log \frac{V_r}{\Delta V_Q}$

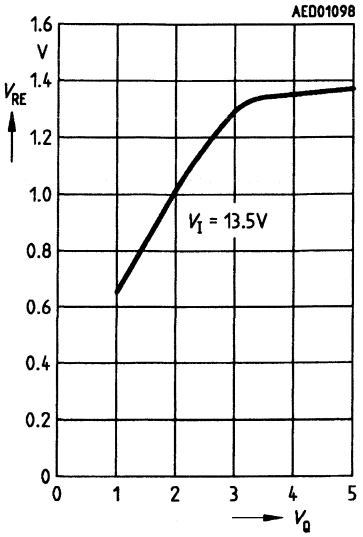
*) Outside control range

Test Circuit

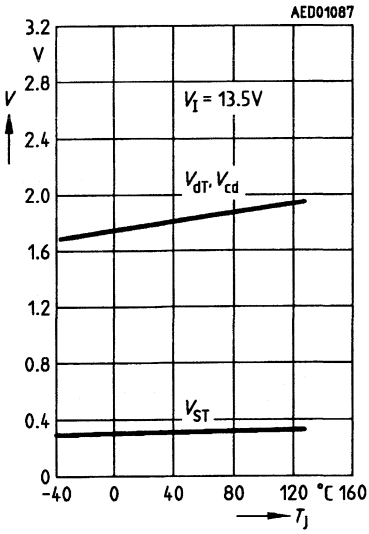


Time Response, Watchdog with High-Frequency Clock

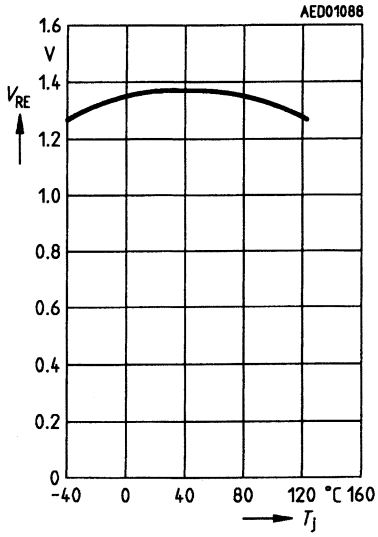
Reset Threshold versus Output Voltage



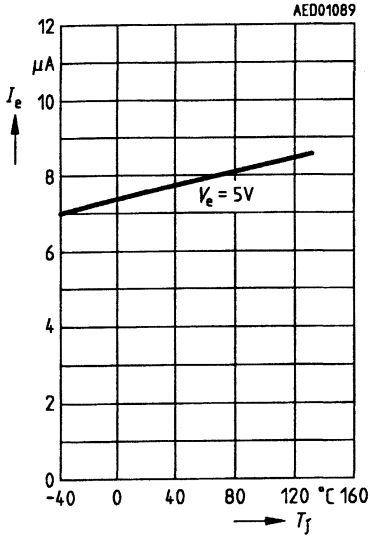
Switching Voltage V_{Cd}, V_{dT} and V_{ST} versus Temperature



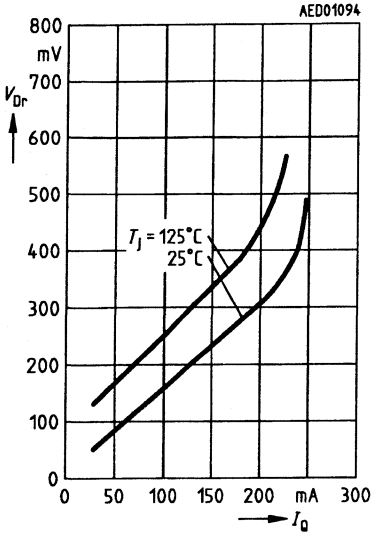
Reset Switching Threshold versus Temperature



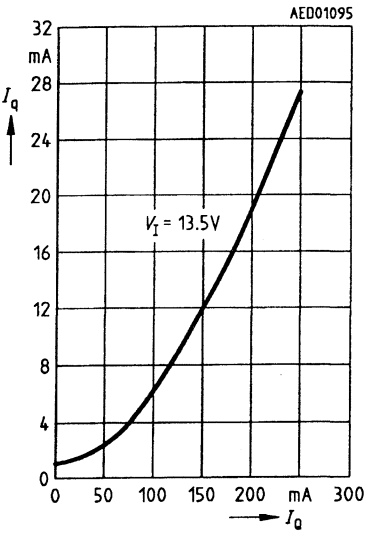
Current Consumption of Inhibit versus Temperature



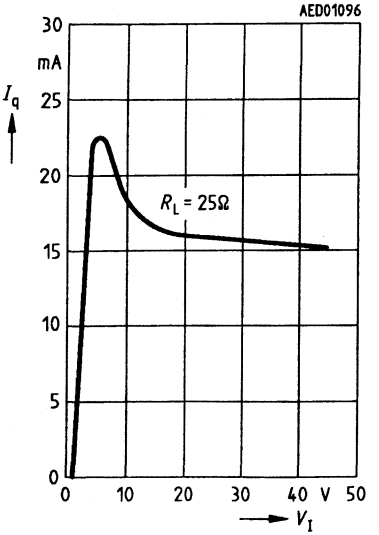
Drop Voltage versus Output Current



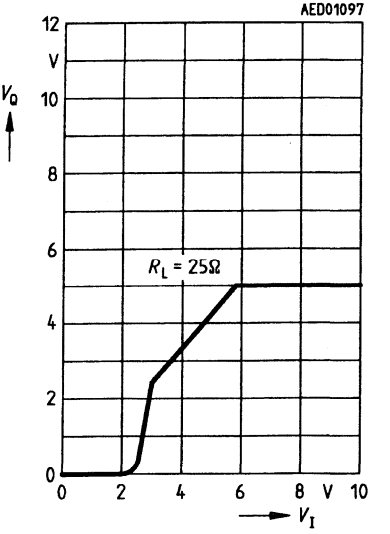
Current Consumption versus Output Current



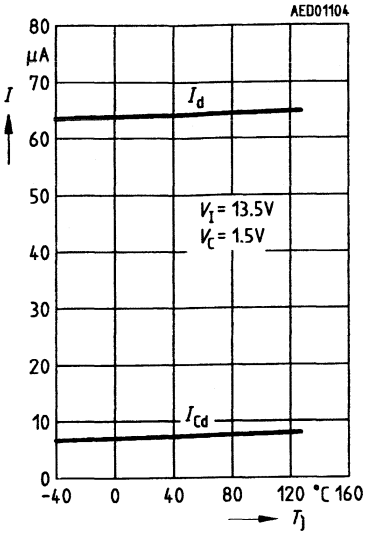
Current Consumption versus Input Voltage



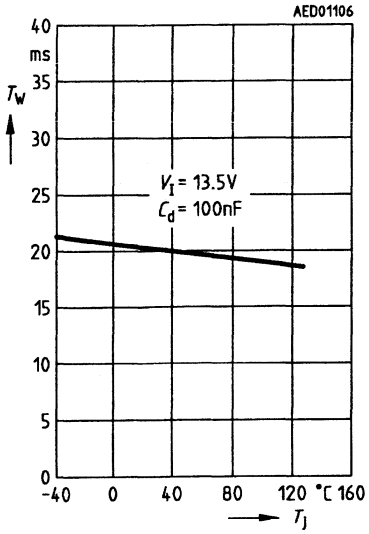
Output Voltage versus Input Voltage



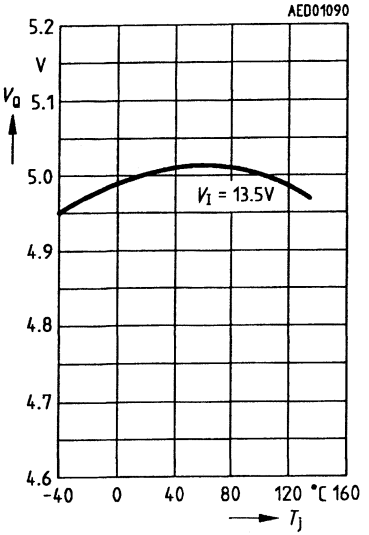
Charge Current and Discharge Current versus Temperature



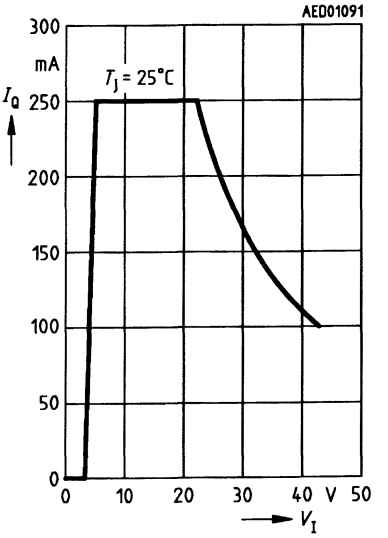
Pulse Time versus Temperature



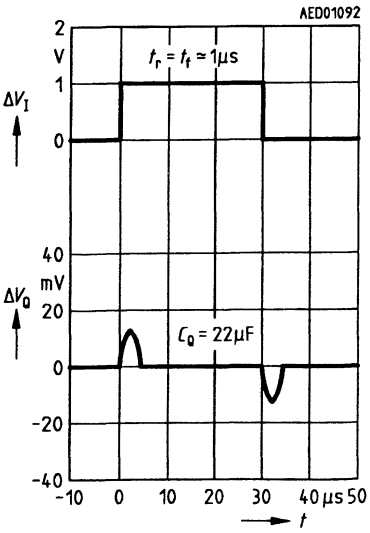
Output Voltage versus Temperature



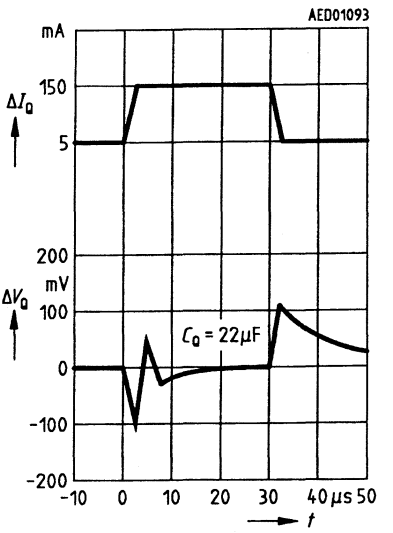
Output Current versus Input Voltage



Input Response



Load Response



Selector Guide

Type	Package	Function	Supply Voltage V_S (V_{CEO}) V	Temperature Range T_A °C	Page
Driver and Interface Circuits					
FZL 4145 D	P-DIP-18-1	Short-circuit proof driver for power transistors with short-circuit signaling output	4.5 to 35	– 25 to 85	263
FZL 4146 G	P-DSO-20-1		4.5 to 40	– 25 to 85	271

= SMD

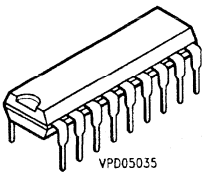
Quad Driver Incl. Short-Circuit Signaling

FZL 4145 D

Bipolar IC

Features

- Short-circuit shutdown with clock generator
- Four driver circuits for controlling power transistors
- Overload and short-circuit signaling



P-DIP-18-1

Type	Ordering Code	Package
S FZL 4145 D	Q67000-H8437	P-DIP-18-1

General Description

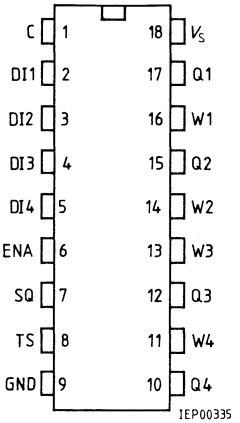
The IC comprises four driver circuits capable of driving power transistors for high output currents. The output transistors are protected against short-circuit to ground and supply voltage. The input threshold can be adjusted between 1.5 V and 7 V. Overload or short-circuit failure at an output will be indicated at pin SQ (signaling output).

Functional Description

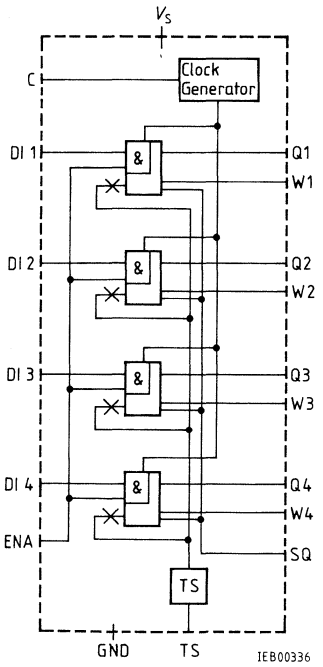
Each driver circuit has one active high driver input DI and a common enable input (ENA) (active high) is provided for all stages. The (Q) outputs are designed to drive the output transistors. The load current is sampled via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-on again is provided by the built-in clock generator. Its operation requires an external capacitor C_T at pin C. If C_T is bridged by a break-key, switching on can only be carried out by operating a key. The duty cycle of the clock generator is 1:50 (e.g. 40 µs/2 ms with C_T = 33 nF).

In case of overcurrent or short-circuit failure at any output stage the signaling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching on by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload exists. SQ is an open-collector output.

Unused W pins must be connected to V_S. Open W pins would simulate a short-circuit and activate the signaling output.



Pin Configuration
(top view)



DI Driver inputs
ENA Enable input
C Clock capacitor
Q Outputs
TS Input for threshold switching
W Input for output current limiter
SQ Signaling output
GND Ground

Block Diagram

The switching threshold at inputs DI and ENA can be adjusted between 1.5 V and 7 V via connection TS:

V_{TS} = 0 V;	input threshold = 1.5 V (for 5 V logic)
V_{TS} = 0 to 5 V;	input threshold = V_{TS} + 1.5 V
V_{TS} = V_S:	input threshold = 7 V (for 12/15 V and 24/28 V logic)

If the output is disabled due to the logic states of inputs DI or ENA this disable is effective over the total supply voltage range between V_S = 0 V and V_S = 35 V.

The inputs are protected with clamp diodes.

5

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	35	V	
	V_S	– 0.3	45	V	100 ms duration, 1 s interval
Input voltage at DI and ENA	$V_{DI, ENA}$	– 0.3	35	V	1)
Voltage at TS and SQ	$V_{TS, SQ}$	– 0.3	45	V	
Output voltage V_Q and voltage at C	V_Q, V_C	– 0.3	V_S	V	
	V_W	V_S – 5	V_S	V	3)
Input current at DI and ENA	$I_{DI, ENA}$	– 3	1	mA	2)
	$I_{DI, ENA}$	– 6	2	mA	2) 100 ms duration, 1 s interval
	$I_{DI, ENA}$	– 6	5	mA	2) 100 µs duration, 1 ms interval
Output current at SQ	I_{SQ}		8	mA	
Power dissipation of all input diodes	P_{tot}		50	mW	
Storage temperature	T_{stg}	– 65	125	°C	
Thermal resistance system - air	$R_{th\ SA}$		65	K/W	
system - case	$R_{th\ SC}$		45	K/W	

Operating Range

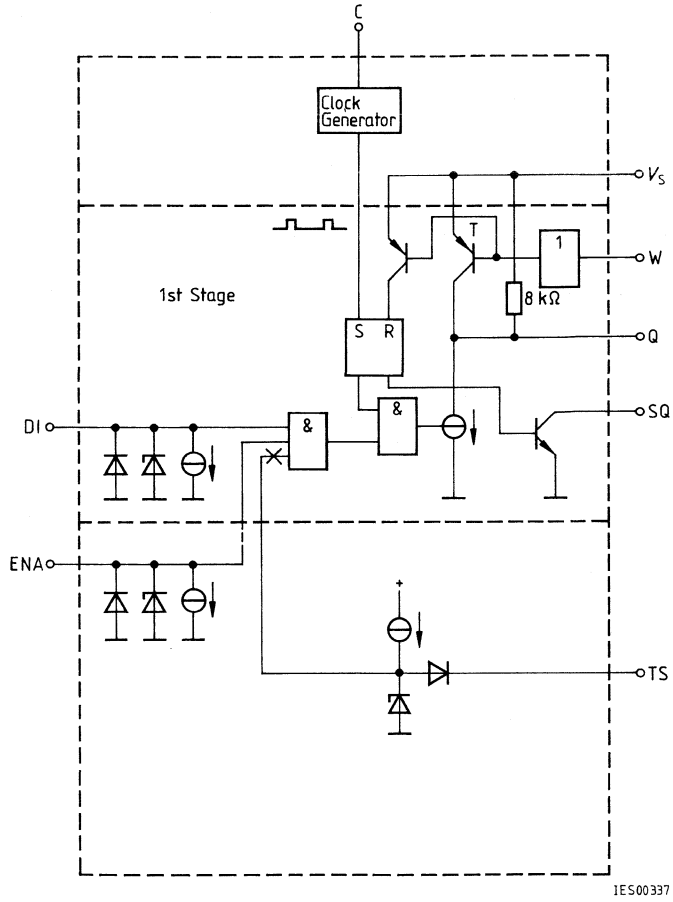
Supply voltage for input threshold 1.5 V	V_S	4.5	35	V	V_{TS} = 0 V
1.5 V to 6.5 V	V_S	V_{TS}+4.5	35	V	V_{TS} = 0 V to 5 V
7 V	V_S	10	35	V	V_{TS} = V_S
Ambient temperature	T_A	– 25	85	°C	

Notes: 1) $V_{DI, ENA}$ > 35 V requires a protective resistor before DI, ENA.
2) $V_{DI, ENA}$ may increase to more than 35 V during current nodes.
3) Unused W connections must be connected to V_S.

Characteristics
Supply voltage 4.5 V ≤ V_S ≤ 30 V

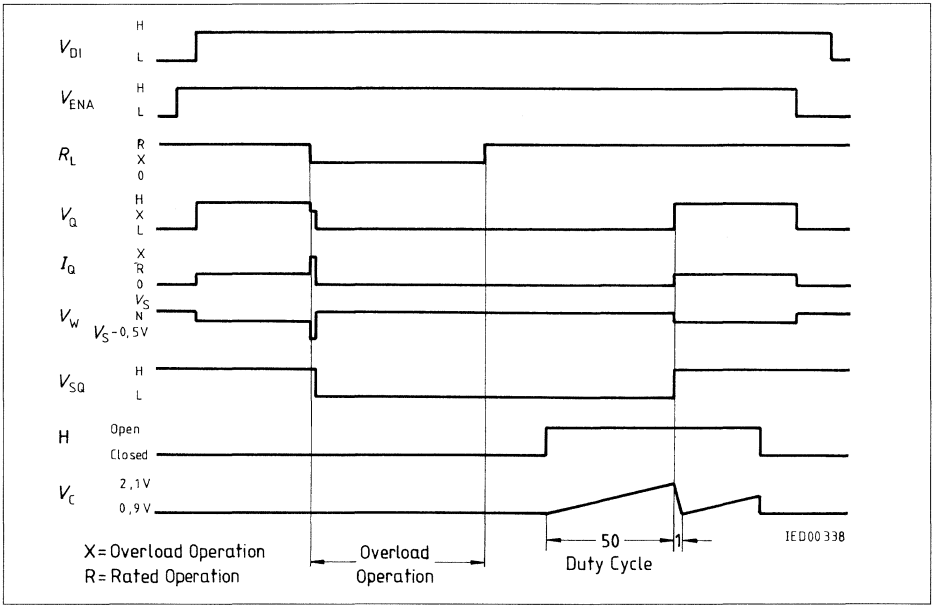
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S		6	8.5	mA	V_{ENA} = 0 V, V_W = V_S
H-input voltage at DI, ENA	V_{IH}	2			V	V_{TS} = 0 V
H-input voltage at DI, ENA	V_{IH}	8			V	V_{TS} = V_S
L-input voltage at DI, ENA	V_{IL}			0.7	V	V_{TS} = 0 V
L-input voltage at DI, ENA	V_{IL}			6	V	V_{TS} = V_S
Input current at DI, ENA	$I_{DI, ENA}$	50		200	µA	0.5 V ≤ $V_{DI, ENA}$ ≤ 30 V
L-output voltage at SQ	V_{SQL}			0.5	V	I_{SQ} = 5 mA
Output current available [1]	I_Q	1.5	2.5		mA	V_Q = V_S – 1.5 V
	I_Q	1.7			mA	T_A = 0 °C, V_Q = V_S – 1.5 V
Current from TS	$-I_{TS}$		2	10	µA	V_{TS} = 0 V
Switching threshold at W	V_W	V_S–0.6	V_S–0.5	V_S–0.4	V	
Current in W	I_W			100	µA	
Current from C	$-I_C$	12	20	34	µA	T_A = 20 °C
Current in C	I_C	0.6	1	1.7	mA	T_A = 20 °C
Upper switching threshold at C	V_{CU}	1.6	2.1	1.7	V	T_A = 20 °C
Lower switching threshold at C	V_{CL}	0.6	0.9	1.2	V	T_A = 20 °C
Saturation voltage at T [2]	V_{QR}		V_S–0.3		V	V_W = V_S – 2 V, I_Q = 0
H-output voltage	V_{QH}	V_S–0.25	V_S–0.02		V	V_{ENA} = 0 V

1) The actual output current is typically 0.5 mA higher, a value which is required as current for the short-circuit protection. However, only the value specified above is available to drive the external output transistors.
2) See block diagram

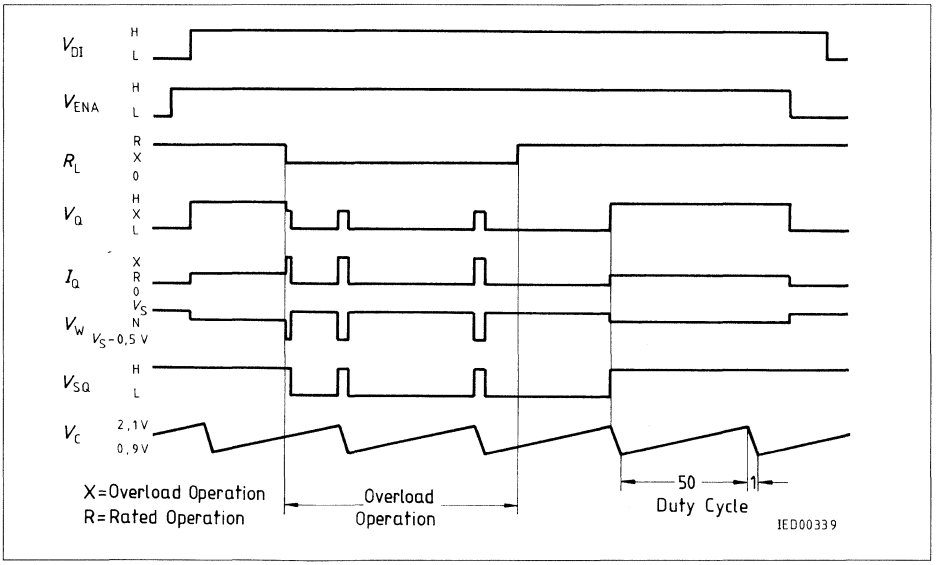


DI	Driver input
ENA	Enable input
C	Clock capacitor
SQ	Signaling output
Q	Output
TS	Input for threshold switching
W	Input for output current limiter

Schematic Circuit Diagram of One Stage



Mode of Operation: Switching-ON again after Overload with Key H



Mode of Operation: Automatic Switching-ON again after Overload

Typical Application Circuits

The load conditions at Q depend on the permissible power dissipation of the used power transistors. The pulsed power dissipation in case of a short circuit must be observed.

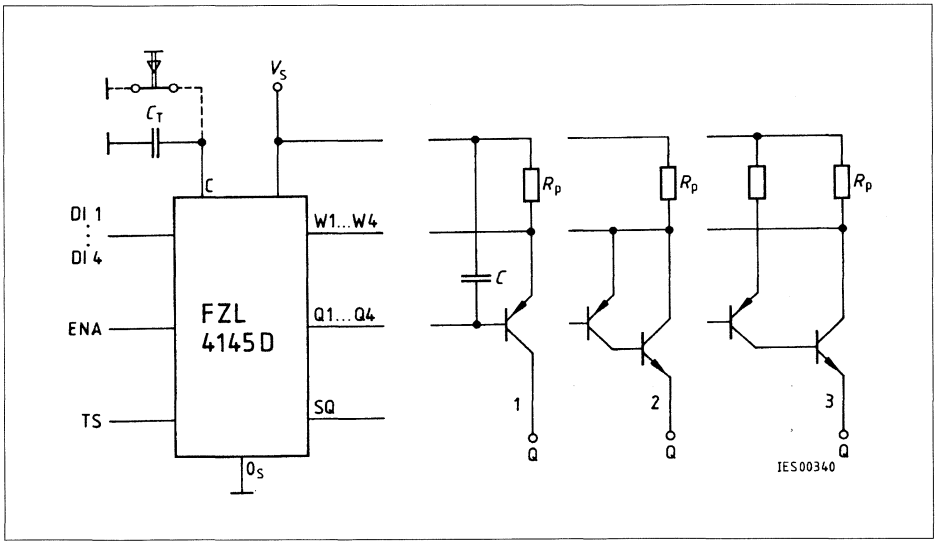
In order to suppress oscillations of the power stage in case of a short circuit, a capacitor C at Q1 to Q4 is necessary if e.g. fast switching transistors are used.

Typical value X of C: approx. 20 nF.

The output circuit 1 is suited for currents up to approx. I_Q = 100 mA.

The output circuit 2 and 3 are suited for currents up to approx. I_Q = 2 A. A minimum power dissipation can be achieved with circuit 3.

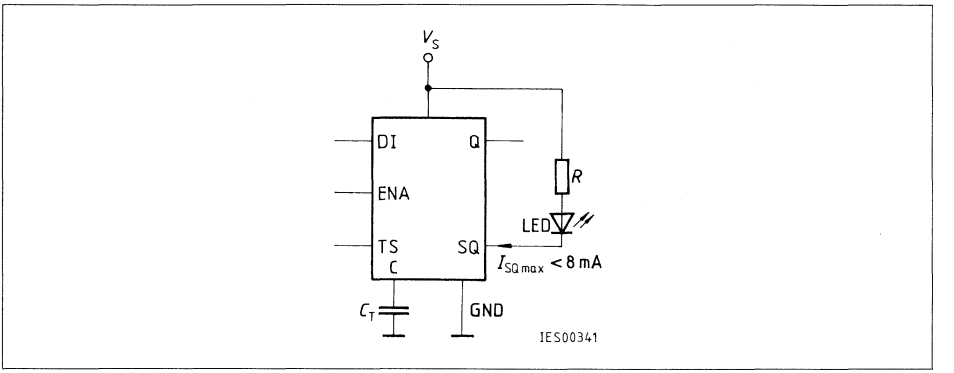
A break key in parallel to C_T allows a manual switch-on in case of short-circuit.



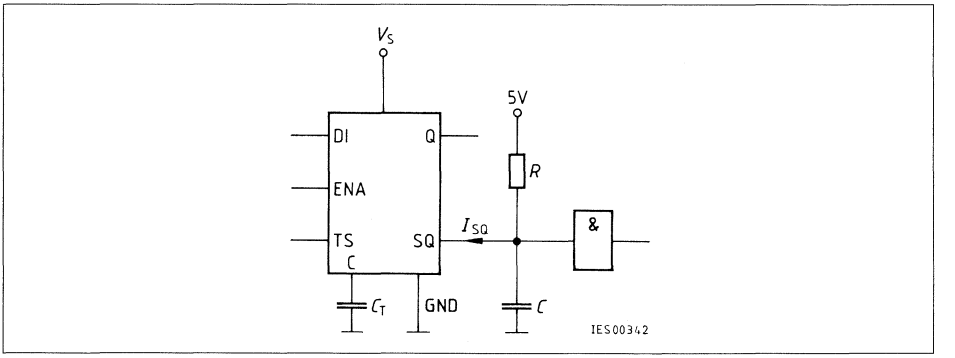
R_P = Precision resistor (current measurement)
$C_T = 0.8 \times t_p$ (nF, µs)
t_p = Short-circuit current pulse length

Note: *Circuit 1 does not permit a capacitor between Q1 and Q4 and the collector.*
Circuit 2 does not permit a capacitor between Q1 and Q4 and base or emitter, respectively.
Otherwise too high current spikes would arise in case of a short circuit.

Typical Application of Short-Circuit Signaling Output SQ



1. LED Display



2. TTL/CMOS/LSL Driving

If the pulses appearing at SQ during clocked operation disturb the remainder of the circuit, a lowpass filter will be necessary. For a load current of I_{SQ} = 1 mA a capacitor C of approx. 10 nF is necessary to limit the output pulses of up to 10 µs (depending on C_T) to 1 V. Signaling occurs after approx. 50 µs.

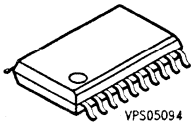
Quad Driver Incl. Short-Circuit Signaling

FZL 4146

Bipolar IC

Features

- Short-circuit signaling
- Four driver circuits for driving power transistors
- Turn-ON threshold setting from 1.5 to 7 V



P-DSO-20-1

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Type	Ordering Code	Package
FZL 4146 G	Q67000-H8743	P-DSO-20-1 (SMD)

General Description

The IC comprises four driver circuits capable of driving power transistors (PNP or PMOS). The output transistors are protected against short-circuit to ground and supply voltage. The turn-ON threshold can be set from 1.5 V to 7 V. Overload at one or several outputs will be indicated at pin SQ (signaling output). The corresponding power transistors are then protected by changeover to clock-governed operation.

Circuit Description

Each driver circuit has one active high driver input DI and a common enable input ENA (active high) is provided for all stages. The Q output is designed to drive the output transistors. The load current is sampled and, if necessary, limited via pin W. If the load current exceeds the preset value, the output stage switches off. Switching-ON again is provided by the built-in clock generator T. Its operation requires an external capacitor C_e at pin CE. If C_e is bridged by a break-key, switching-ON can only be carried out by operating a key. The duty cycle of the clock generator is 1:47 (e.g. 45 µs/2.1 ms with C_e = 10 nF). The clock generator is previleged versus the current sensor shut down. When the supply is connected, the internal RS-FF goes into the state corresponding to the released output.

The turn-ON threshold at input DI and ENA can be set via pin TS from 1.5 to 7 V.

V_{TS} = 0V ... 1.5 V	Turn-ON threshold = 1.5 V
V_{TS} = 1.5 V ... 1.5 V	Turn-ON threshold = V_{TS}
V_{TS} = V_S	Turn-ON threshold = 7 V

Inputs DI, ENA and W are proof against line break, i.e. an open input at DI or ENA corresponds to input L, open input W corresponds to overcurrent. If input TS is open, the highest turn-ON threshold is provided.

The internal current supply B and the undervoltage monitor UV ensure that in case of a supply voltage that is below the V_S turn-OFF threshold, ouputs Q and SQ are disabled and the inputs go high-impedance. Basic functioning is possible within the range from V_S turn-OFF threshold to 4.5V.

In case of overcurrent or short-circuit to ground at any output stage the signaling output (SQ) will go low. In clock-governed operation (i.e. when there is automatic switching-ON by the clock and not by a key), SQ goes high and low at the clock rate as long as a short-circuit or overload is present. SQ is an open-collector output.

Any input and output is ESD proof within the limit values.

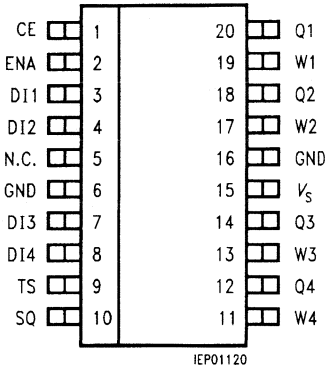


Figure 1
Pin Configuration (top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	CE	Pin for C_e
2	ENA	Enable input for drivers 1 to 4
3	DI1	Input, driver 1
4	DI2	Input, driver 2
5	N.C.	Not connected
6	GND	Ground
7	DI3	Input, driver 3
8	DI4	Input, driver 4
9	TS	Threshold changeover for all inputs
10	SQ	Short-circuit signaling, output for drivers 1 to 4
11	W4	Output, current sensor driver 4
12	Q4	Output, driver 4
13	W3	Output, current sensor driver 3
14	Q3	Output, driver 3
15	V_S	Supply voltage
16	GND	Ground
17	W2	Output, current sensor driver 2
18	Q2	Output, driver 2
19	W1	Output, current sensor driver 1
20	Q1	Output, driver 1

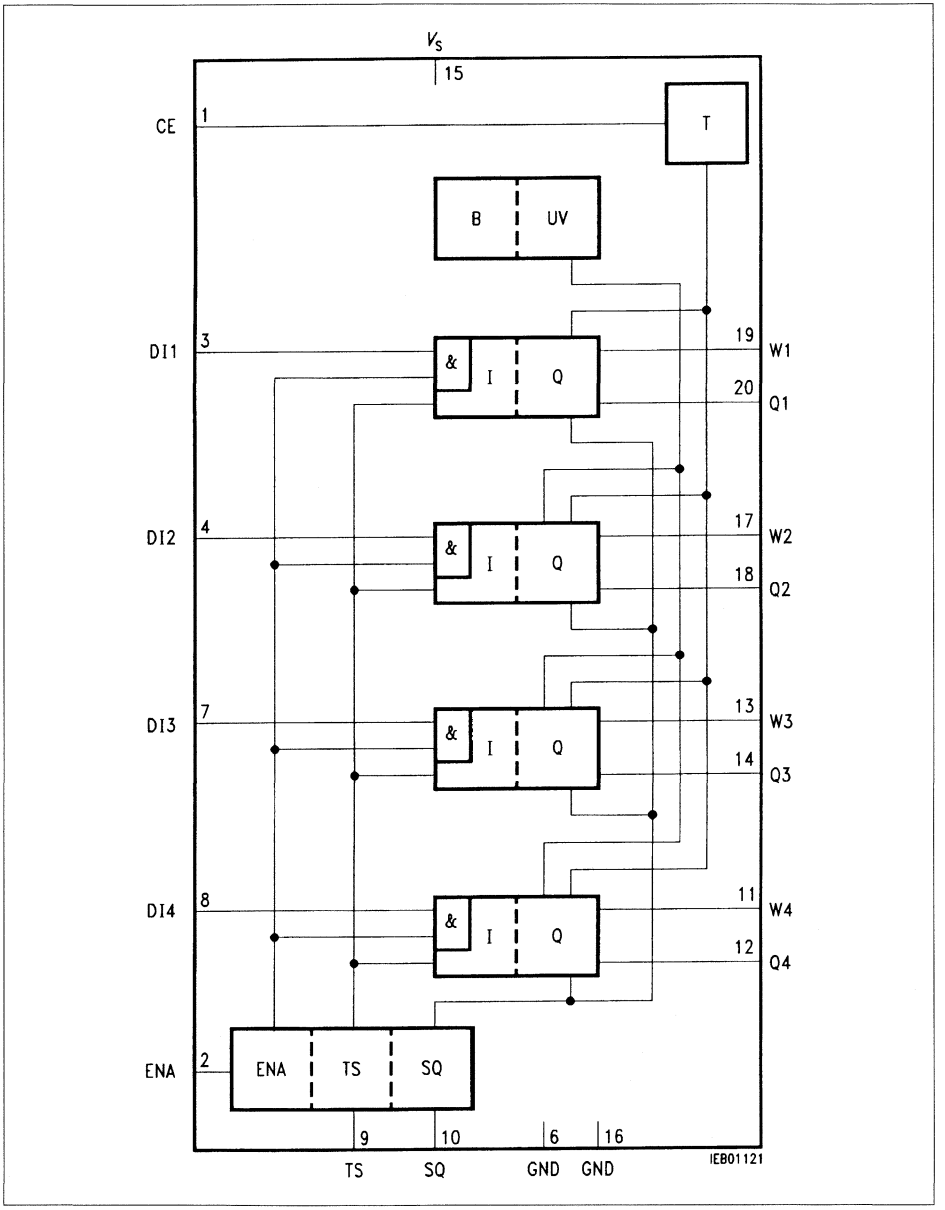


Figure 2
Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	40	V	
Supply voltage	V_S	– 0.3	45	V	100 ms, 5s interval
Supply voltage	V_S	– 0.3	48	V	120 µs
Reverse supply current in GND	I_{GND}		0.5	A	1) 4)
Input voltage at DI and ENA, TS	$V_{DI\ ENA,TS}$	– 5	40	V	
Input voltage at DI and ENA, TS	$V_{DI\ ENA,TS}$	– 5	45	V	100 ms, 5s interval
Output voltage Q	V_Q	V_S – 8	V_S	V	min. (– 0.3 V)
Current in Q	I_Q	– 10	3	mA	18)
Voltage on W	V_W	V_S – 6.5	V_S + 5	V	min. - 0.3V, max. 45V
Voltage on W	V_W	V_S – 12	V_S + 5	V	min. - 0.3V, max. 45V 2)
Voltage on CE	V_C	– 0.3	V_S	V	min. - 0.3V, max. 45V 3)
Voltage on SQ	V_{SQ}	– 0.5	45	V	Output high
Input current DI, ENA, TS	$V_{DI,\ ENA,T}$	– 3	3	mA	4)
Input current DI, ENA, TS	$V_{DI,\ ENA,T}$	– 5	5	mA	100 ms, 5 s interval
Input current DI, ENA, TS	$V_{DI,\ ENA,T}$	– 10	10	mA	10 µs, 500 µs interval
Current in SQ	I_{SQ}	– 3	8	mA	Output low
Current in W	I_W	– 5	5	mA	1ms, 50 ms interval5)
Current in W	I_W	– 10	10	mA	10 µs, 500 µs interval5)
Junction temperature	T_j	– 40	150	°C	
Storage temperature	T_{stg}	– 50	150	°C	
Therm. resistance,system-ambient	$R_{th\ SA}$		95	K/W	
Therm. resistance,system-packag.	$R_{th\ SP}$		25	K/W	6)
ESD strength acc. to MIL - hrs.883 Meth. 3015(100pF/1.5 kΩ, 5 discharges/polarity)	V_{ESD}	– 2	2	kV	

Notes:
1) An adequate resistor in the GND-line can provide protection in case of polarization of V_S. It should be noted, however, that in this case all pins may become conductive across GND.
2) Loading may lead to degradation and thus to a shift of the switching threshold at W. (Characteristics: switching threshold at W). Short loading may lead to a deviation of approx. 20 mV.
3) In case of short-circuit of V_S, the capacitance stored in C_e during previous operation will not damage the IC.
4) Note the power loss.
5) Loading may lead to degradation and thus to a shift of the switching threshold at W. Unfrequent loading leads to a deviation of approx.20 mV.
6) Related to GND; the GND pins are connected with the chip carrier via the leadframe.
7) If it can be prooved with samples.
8) During normal operation, the failure rate is ≤ 100 fit acc. to SN 29500 at a junction temperature of 75°C.

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Burst strength of the inputs/outputs Q and W connected to the power transistors (in acc. with IEC publ. 801-4)	V_{Burst}	300		V	7)
Junction temperature in normal operation during 15 years with 100 % ED	T_{j15}		125	°C	8)

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		9)
Supply voltage 11)	V_S	4.5	40	V	V_{TS} = 0 ... 1.5 V
Supply voltage 12)	V_S	V_S + 3	40	V	V_{TS} = 1.5 ... 7 V
Supply voltage 13)	V_S	10	40	V	$V_{TS} = V_S$
Supply voltage rise	dV_S/dt	– 1	1	V/ µs	20)
Junction temperature	T_j	– 25	150	°C	
Time-determining capacitor of the clock generator	C_e	1	100	nF	10)
Input voltage	$V_{DI,ENA,TS}$	– 2	40	V	14) 15) 16) 17) 19)
Current at output SQ	I_{SQ}	– 1	6	mA	

Notes:

9) W-pins that remain open, must be connected to V_S.

10) The C_e value depends on the desired pulse width tp during short circuit. It applies: C_e = 0.25 ms x tp.

11) At an input threshold = 1.5 V

12) At an input threshold = 1.5 V to 7 V

13) At an input threshold = 7 V

14) This function is also ensured for 40 V ≤ V_S ≤ 45 V and - 40 °C ≤ T_j ≤ - 25 °C as long as 0 V ≤ $V_{DI, ENA, TS}$ ≤ 40 V

15) The outputs Q are disabled even if - 3 V ≤ $V_{DI,ENA}$ ≤ - 2 V or - 1mA ≤ $V_{DI,ENA}$ ≤ 50 µA and V_S - 5 V ≤ V_W ≤ V_S + 5 V, max 45.

16) The outputs Q are enabled even if 40 V ≤ $V_{I, ENA}$ ≤ 45 V and V_S - 0.2 V ≤ V_W ≤ V_S + 5 V, max. 45 V.

17) Current limiting and disabling of outputs Q are ensured even if 40 V ≤ $V_{DI,ENA}$ ≤ 45 V and V_S - 5 V ≤ V_W ≤ V_S - 0.4 V.

18) Dynamic charge reversal of a 2 nF capacitor as in **figure 3** is permissible (corresponds to short circuit to conducting output in P-channel MOSFET)

19) Proper working of the IC is also ensured if, before V_S is turned-On, an input voltage $V_{DI,ENA}$ is present in the permissible range (footnote 15).

20) Brief dynamic malfunction possible at 10 V/µs, but no latch-up.

Characteristics
Supply voltage 4.5 V ≤ V_S ≤ 40 V, junction temperature - 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max		
Current consumption	$I_{S, off}$			5	mA	V_{ENA} = 0 V, $V_W = V_S$ [4]
Current consumption	$I_{S, on}$			13.5	mA	$V_{ENA} = V_{DI} = V_W = V_Q = V_S$; V_{TS} = 0 V [3]
H-input voltage at DI, ENA	V_{IH}	2			V	V_{TS} = 0 V
H-input voltage at DI, ENA	V_{IH}	6.8			V	$V_{TS} = V_S$
L-input voltage at DI, ENA	V_{IL}			0.7	V	V_{TS} = 0 V
L-input voltage at DI, ENA	V_{IL}			4.8	V	$V_{TS} = V_S$
Input hysteresis	V_{HI}	50		200	µA	0 V ≤ V_{TS} ≤ V_S
Input current DI, ENA [1), 7)]	$I_{DI, ENA}$	50		200	µA	1.5 V ≤ $V_{DI, ENA}$ ≤ 30 V
Input current DI, ENA	$I_{DI0, ENA0}$			100	µA	0 V ≤ $V_{DI, ENA}$ ≤ 30 V, V_S = 0 V
L-output voltage at SQ	$V_{SQ L}$			0.5	V	I_{SQ} = 5 mA, $V_W = V_S$ – 2V
Leakage current output SQ	$I_{SQ H}$			10	µA	$V_W = V_S$
Output current Q	I_{Q0}	0.6		1.6	mA	V_S -2V ≤ V_Q ≤ V_S
Current from TS	$-I_{TS}$	2	5	10	µA	V_{TS} = 07 V
Current in W	I_W			100	µA	V_S –2V≤ V_W ≤ V_S
Switching threshold at W [2)]	V_W	V_S– 0.25	V_S– 0.3	V_S –0.35	V	
Current in W	I_W			100	µA	
Current from CE	$-I_{Ce}$	12	20	34	µA	T_A = 20 °C
Current in CE	I_{Ce}	0.6	1	1.7	mA	T_A = 20 °C
Charge current from CE	$-I_{Ce}$			5	µA	
Discharge current from CE	V_{C0}			235	µA	
Upper switching threshold at CE	V_{CU}			2.4	V	
Lower switching threshold at CE	V_{CL}			1.4	V	

For footnotes, see 2 pages hereafter.

Characteristics (cont'd)
Supply voltage 4.5 V ≤ V_S ≤ 40 V, junction temperature - 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_Q at overcurrent	V_{QR} 6)	V_S-0.4V			V	$V_W = V_S$ -2V, = -20 uA
V_Q at output disabled	V_{QL} 6)	V_S-0.4V			V	V_{ENA} = 0 V, I_Q = - 20 µA, 0 V ≤ V_S ≤ 40 V
Signal run time LH	t_{PLH}			50	µs	
Signal run time LH	t_{PHL}			50	µs	
Pulse width	t_P	33	45	65	µs	C_e = 10 nF
Duty cycle	t_P/t_0	1:55	1:47	1:40		C_e = 10 nF
Delay time of the short-circuit signaling	t_{PWM} 5)			10	µs	V_C = 0 V
Duration of the negative spikes at input W, which do not result in switching off	t_{VZ}	1			µs	
Difference between V_{TS} and input switching threshold ENA, DI during transition from L to H	V_{DIH} - V_{TS}	– 0.2		0.2	V	V_{TS} = 2 ... 4.8 V
Idling voltage at output Q	V_{QH}	V_S –13	V_S–11.5	V_S –10	V	V_S ≥ 18V
V_S turn-Off threshold	V_{TSV}	2.5		4.5	V	$V_Q > V_{QL}$; I_Q = -20 µA
Resistance across Q and V_S	R_Q	8	13	19	kΩ	V_{ENA} = 0 V; I_Q = -100 µA $R_Q = (V_S - V_Q)$ /0.1 mA
Z-diode internal resistance	R_Z		20	50	Ω	V_{ENA} = 0 V; I_{Q1} = -3 mA I_{Q2} = -8 mA, $R_Q = \Delta V_Q$/5 mA

Footnotes for the Characteristics

1) The given limit values apply to inputs DI, ENA, if they are not measured, from 0 to 40 V.
2) The layout provides an adaption of $V_{W\,typ.}$ from V_S –0.3V to V_S –0.4 V or V_S –0.48 V by simply changing of the ALU mask.
3) All inputs DI1 to DI4 and W1 to W4 as well as Q1 to Q4
I_{SON} means the sum of all currents flowing from the voltage source V_S into the IC, i.e.
$I_{SON} = I_S + \Sigma I_{DI} + \Sigma I_{ENA} + \Sigma I_W + \Sigma I_Q$
4) All other pins are open
5) The delay time of loop W → I regulator → RS-FF AND → current source → Q is unaccessable for measurement without external wiring due to fast reaction of the current regulator. For this reason, in case of overload, the above mentioned switch-OFF delay time is replaced by the delay time for input W → output SQ.
Measurement: jump function at W from $V_W = V_S$ to $V_W = V_S$ –1V
6) IQ = leakage current I_{CBO} of the external PNP driver transistor
7) For $V_{ID,TS} < 1.5$ V, $I_{DI,ENA}$ remains below its minimum value; it is however ensured that in case of open inputs the corresponding outputs will be safely disabled.

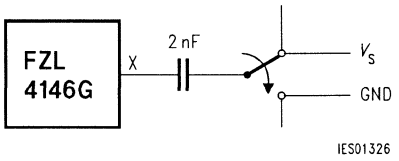


Figure 3

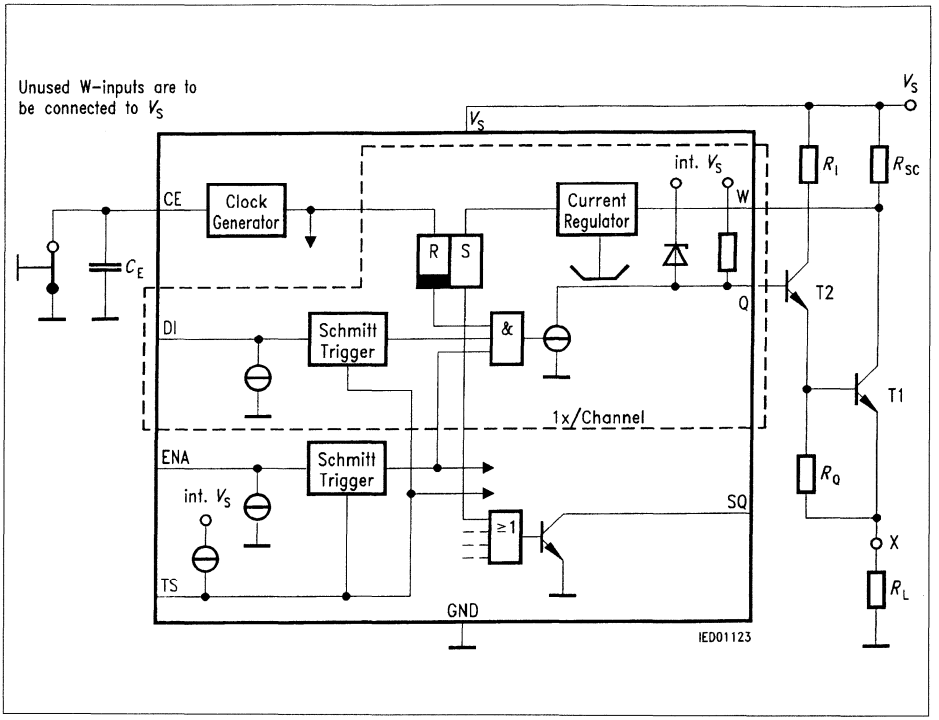


Figure 4
Application Circuit

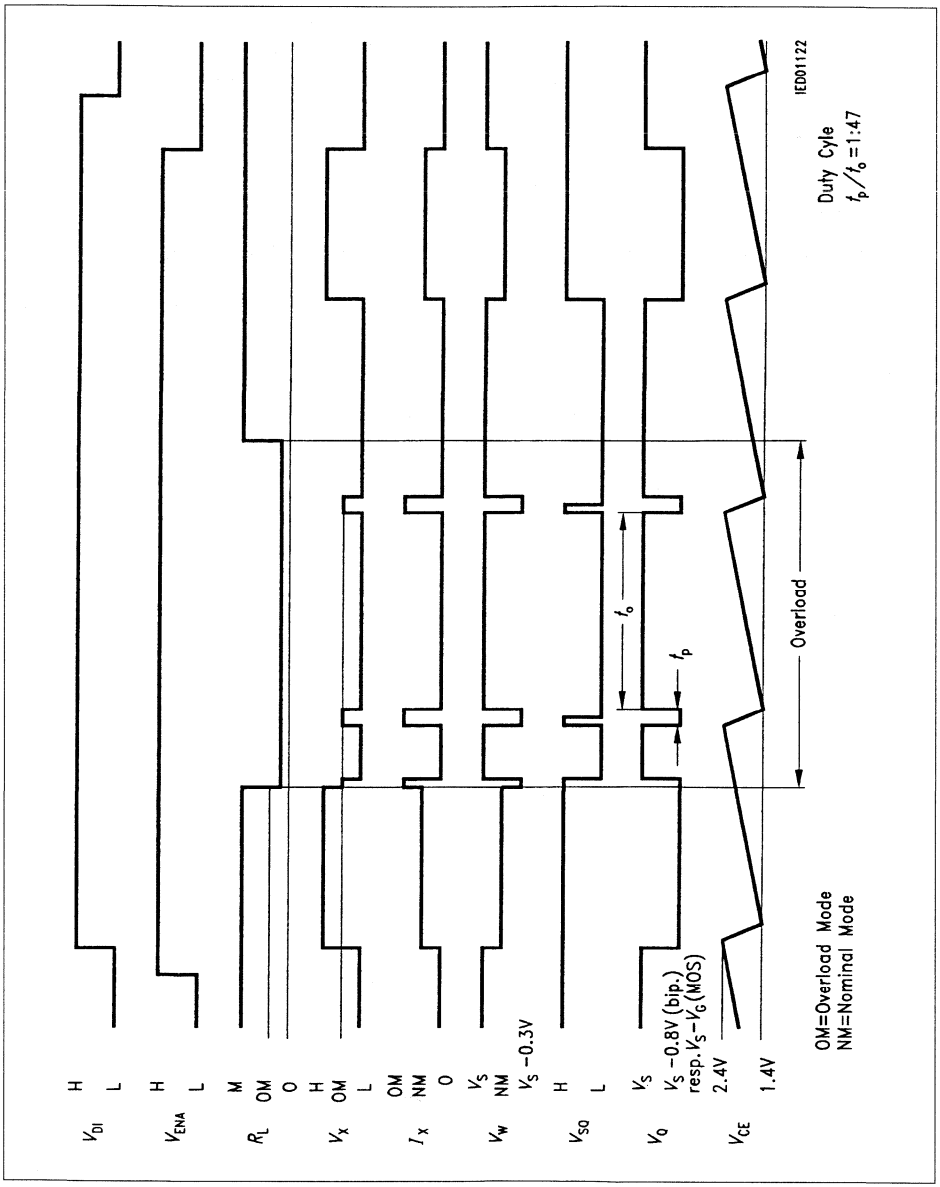


Figure 5
Operating Mode: Automatic Turn-ON after Overload

Selector Guide

Type	Package	Function	Supply Voltage V_S (V_{CEO}) V	Temperature Range T_A °C	Page
TCA 785	P-DIP-16	Phase control for thyristors, triacs, transistors Output current max. 400mA	8 to 18	– 25 to 85	285
SLB 0586 A	P-DIP-8	Dimmer IC (Incandescent Lamps)	– 5.6 to – 4.5	0 to 80	301
SLB 0586 G	P-DSO-8-1	Dimmer IC (Incandescent Lamps)	– 5.6 to – 4.5	0 to 80	301
SLB 0587	P-DIP-8	Dimmer IC (Incandescent + Halogen Lamps)	– 5.6 to – 4.5	0 to 100	318
SLB 0587 G	P-DSO-8-1	Dimmer IC (Incandescent + Halogen Lamps)	– 5.6 to – 4.5	0 to 100	318

= SMD

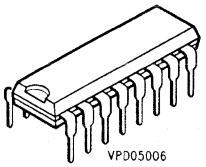
Phase Control IC

TCA 785

Bipolar IC

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Wide temperature range



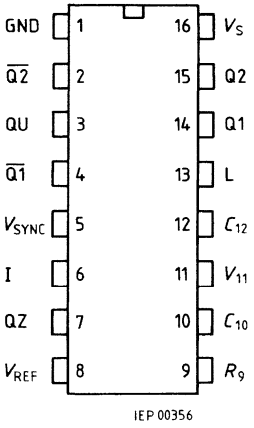
P-DIP-16

6

Type	Ordering Code	Package
S TCA 785	Q67000-A2321	P-DIP-16

This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0 ° and 180 °. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	$\overline{Q2}$	Output 2 inverted
3	QU	Output U
4	$\overline{Q1}$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	QZ	Output Z
8	V_{REF}	Stabilized voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q1	Output 1
15	Q2	Output 2
16	V_S	Supply voltage

Functional Description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator, the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q 1 and Q 2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

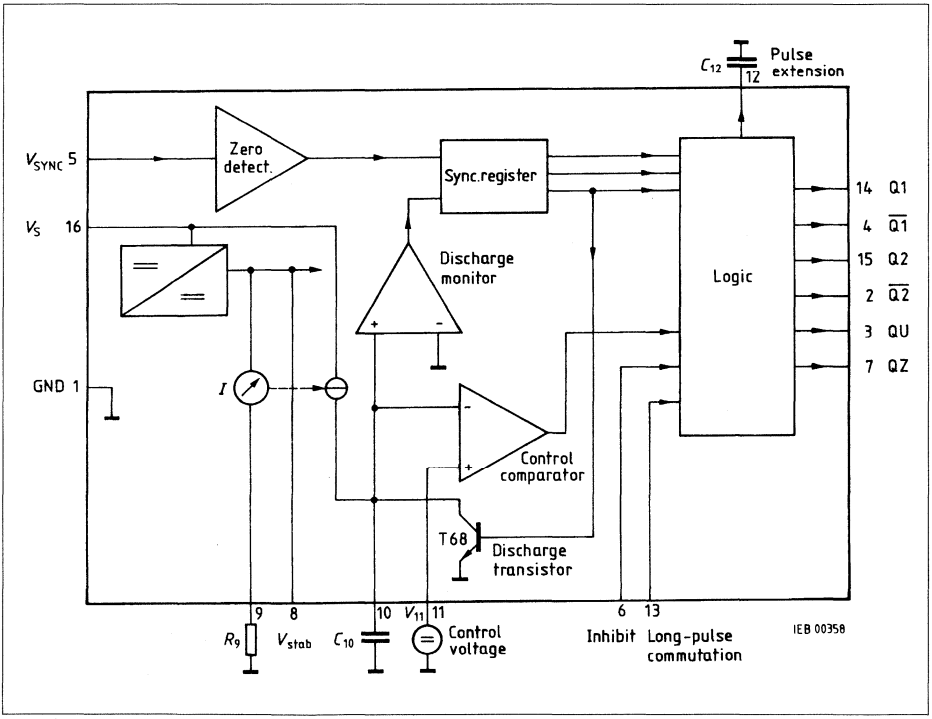
Outputs $\overline{Q\,1}$ and $\overline{Q\,2}$ supply the inverse signals of Q1 and Q2.

A signal of φ +180° which can be used for controlling an external logic,is available at pin 3.

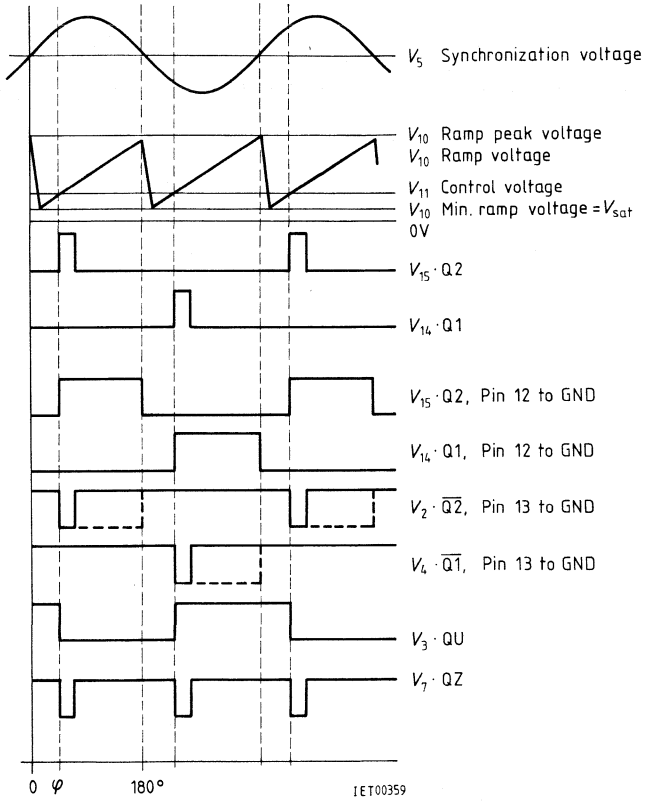
A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

The inhibit input can be used to disable outputs Q1, Q2 and $\overline{Q\,1}$, $\overline{Q\,2}$.

Pin 13 can be used to extend the outputs $\overline{Q\,1}$ and $\overline{Q\,2}$ to full pulse length (180° – φ).



Block Diagram



Pulse Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.5	18	V
Output current at pin 14, 15	I_Q	– 10	400	mA
Inhibit voltage Control voltage Voltage short-pulse circuit	V_6 V_{11} V_{13}	– 0.5 – 0.5 – 0.5	V_S V_S V_S	V V V
Synchronization input current	V_5	– 200	± 200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature Storage temperature	T_j T_{stg}	 – 55	150 125	°C °C
Thermal resistance system - air	$R_{th\ SA}$		80	K/W

Operating Range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature	T_A	– 25	85	°C

Characteristics

$8 \leq V_S \leq 18$ V; -25 °C $\leq T_A \leq 85$ °C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Supply current consumption S1 ... S6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	4.5	6.5	10	mA	1
Synchronization pin 5 Input current R_2 varied Offset voltage	 $I_{5\ rms}$ ΔV_5	 30 	 30	 200 75	 µA mV	 1 4
Control input pin 11 Control voltage range Input resistance	 V_{11} R_{11}	 0.2 	 15	 $V_{10\ peak}$ 	 V kΩ	 1 5

Characteristics (cont'd)
$8 \le V_S \le 18$ V; -25 °C $\le T_A \le 85$ °C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Ramp generator						
Charge current	I_{10}	10		1000	µA	
Max. ramp voltage	V_{10}			$V_2 - 2$	V	1
Saturation voltage at capacitor	V_{10}	100	225	350	mV	1.6
Ramp resistance	R_9	3		300	kΩ	1
Sawtooth return time	t_f		80		µs	1
Inhibit pin 6						
switch-over of pin 7						
Outputs disabled	V_{6L}		3.3	2.5	V	1
Outputs enabled	V_{6H}	4	3.3		V	1
Signal transition time	t_r	1		5	µs	1
Input current $V_6 = 8$ V	I_{6H}		500	800	µA	1
Input current $V_6 = 1.7$ V	$-I_{6L}$	80	150	200	µA	1
Deviation of I_{10} R_9 = const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	-5		5	%	1
Deviation of I_{10} R_9 = const. $V_S = 8$ V to 18 V	I_{10}	-20		20	%	1
Deviation of the ramp voltage between 2 following half-waves, V_S = const.	$\Delta V_{10\,max}$		± 1		%	
Long pulse switch-over pin 13						
switch-over of S8						
Short pulse at output	V_{13H}	3.5	2.5		V	1
Long pulse at output	V_{13L}		2.5	2	V	1
Input current $V_{13} = 8$ V	I_{13H}			10	µA	1
Input current $V_{13} = 1.7$ V	$-I_{13L}$	45	65	100	µA	1
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CEO}			10	µA	2.6
Saturation voltage $I_Q = 2$ mA	V_{sat}	0.1	0.4	2	V	2.6

6

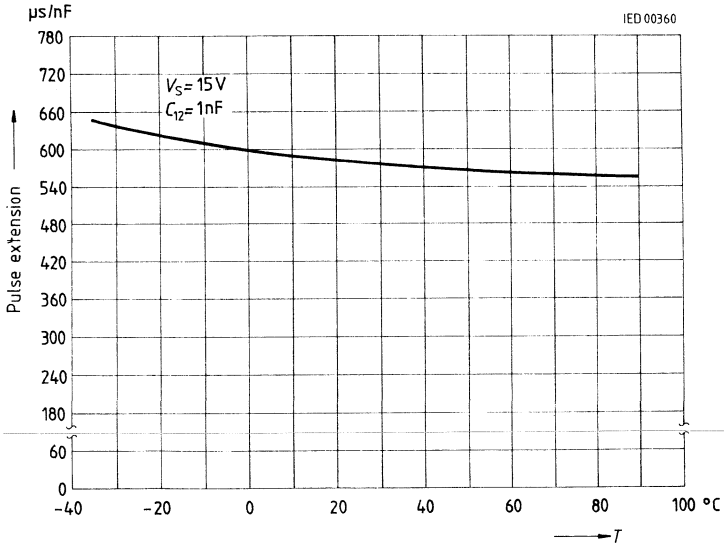
Characteristics (cont'd)
$8 \leq V_S \leq 18$ V; -25 °C $\leq T_A \leq 85$ °C; $f = 50$ Hz

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Outputs pin 14, 15						
H-output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	$V_S - 3$	$V_S - 2.5$	$V_S - 1.0$	V	3.6
L-output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	0.3	0.8	2	V	2.6
Pulse width (short pulse) S9 open	t_p	20	30	40	µs	1
Pulse width (short pulse) with C_{12}	t_p	530	620	760	µs/ nF	1
Internal voltage control						
Reference voltage Parallel connection of 10 ICs possible	V_{REF}	2.8	3.1	3.4	V	1
TC of reference voltage	α_{REF}		2×10^{-4}	5×10^{-4}	1/K	1

Application Hints for External Components

		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{REF} \times K}$		[2]	
Charge current	$I_{10} = \frac{V_{REF} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2\,V$ $V_{10} = \frac{V_{REF} \times K \times t}{R_9 \times C_{10}}$ [2]

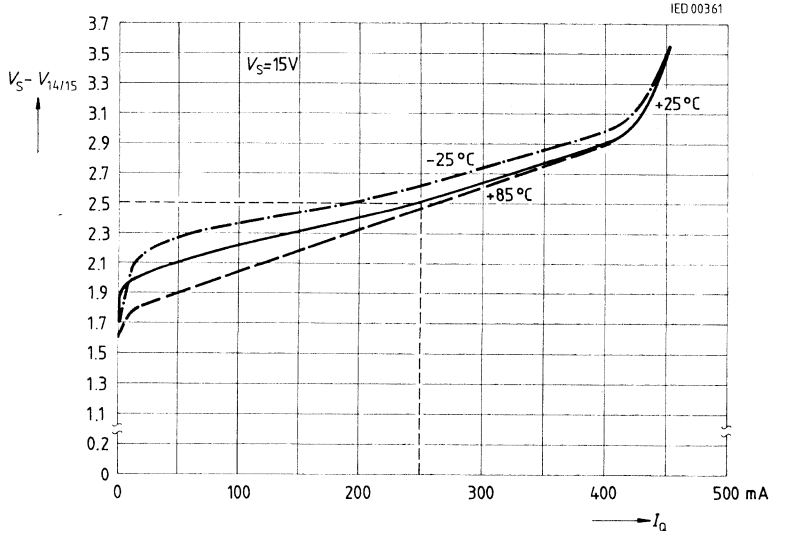
Pulse Extension versus Temperature



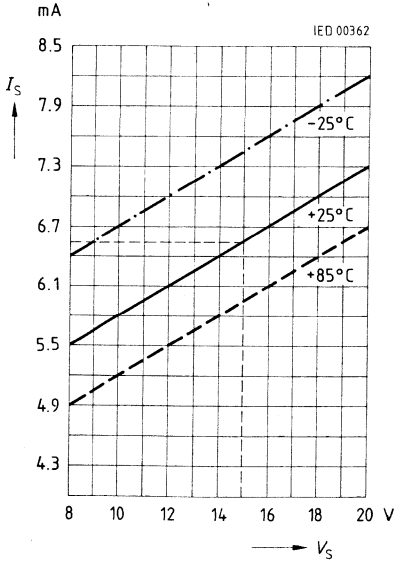
[1] Attention to flyback times

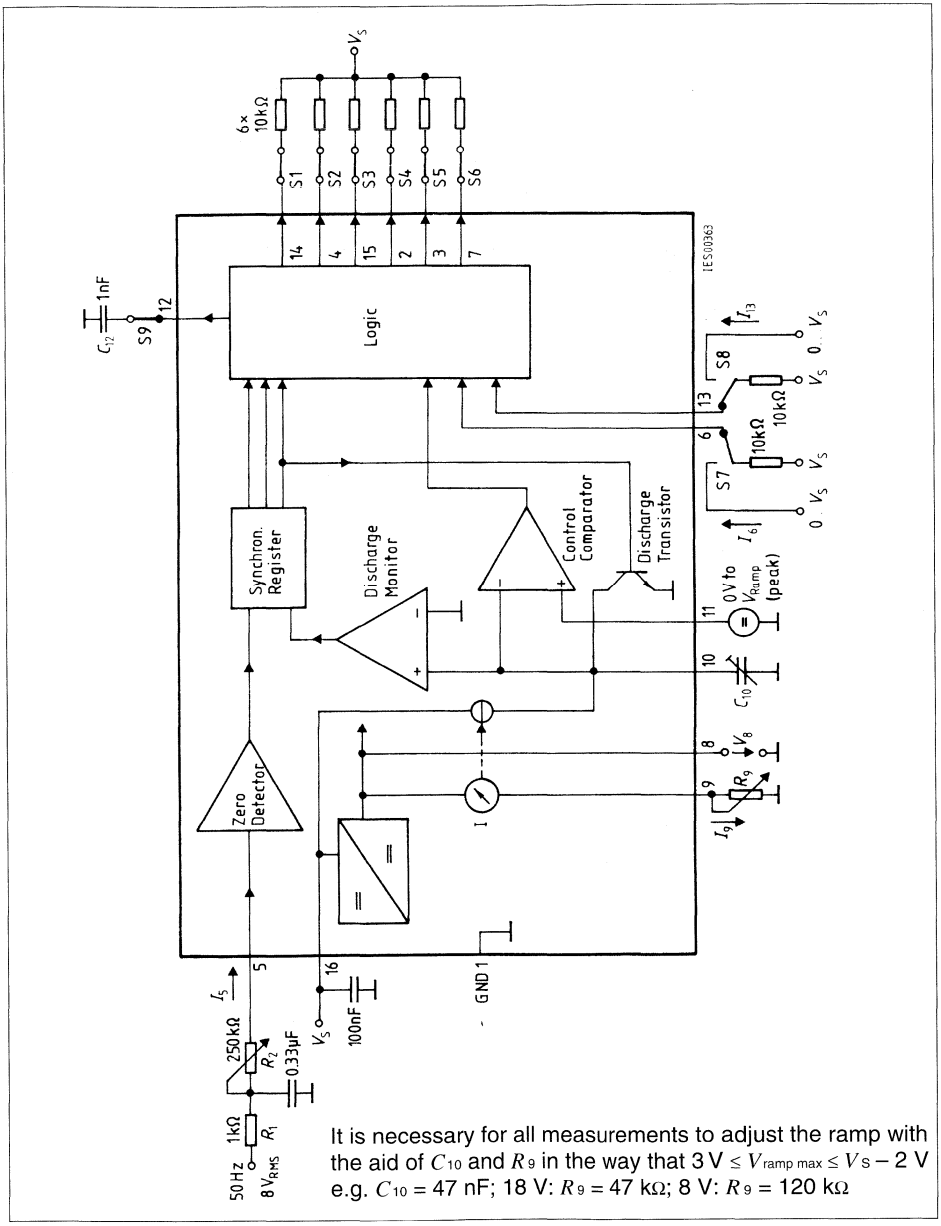
[2] $K = 1.10 \pm 20\,\%$

Output Voltage measured to + V_S



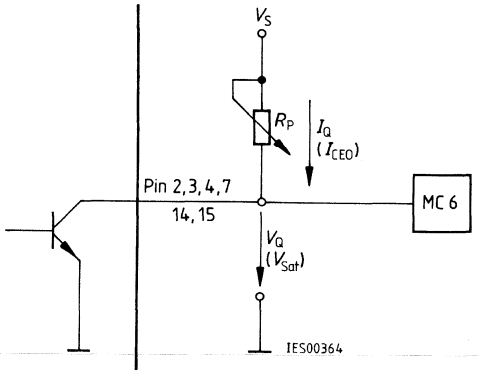
Supply Current versus Supply Voltage





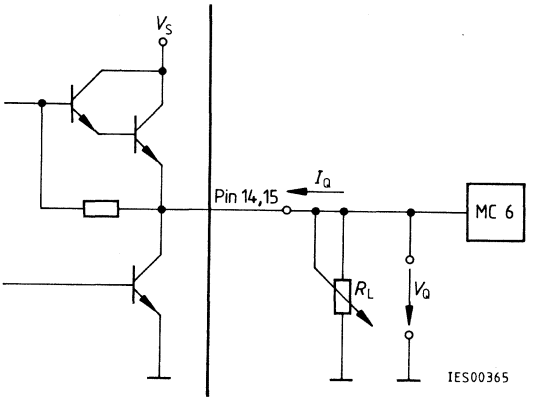
It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\,V \leq V_{ramp\,max} \leq V_S - 2\,V$ e.g. C_{10} = 47 nF; 18 V: R_9 = 47 kΩ; 8 V: R_9 = 120 kΩ

Test Circuit 1



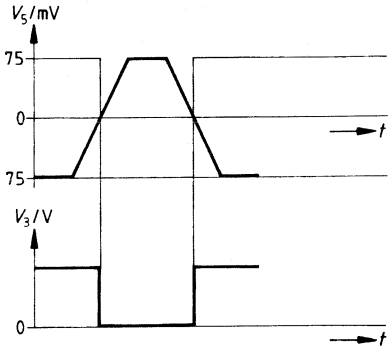
The remaining pins are connected as in test circuit 1

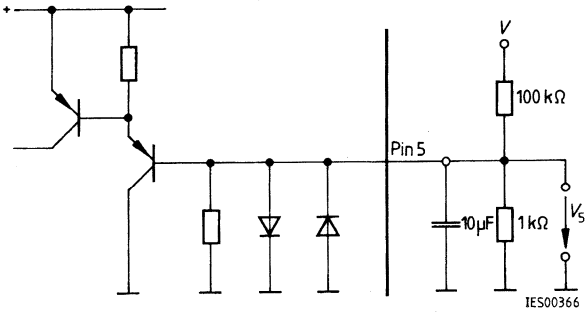
Test Circuit 2



The remaining pins are connected as in test circuit 1

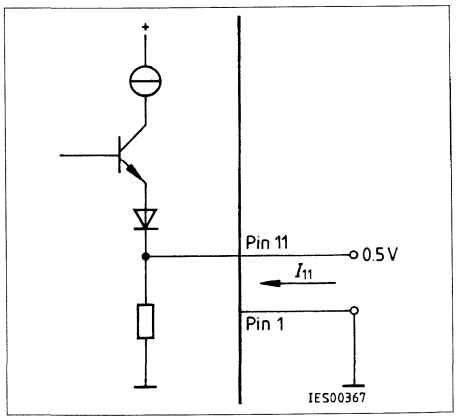
Test Circuit 3



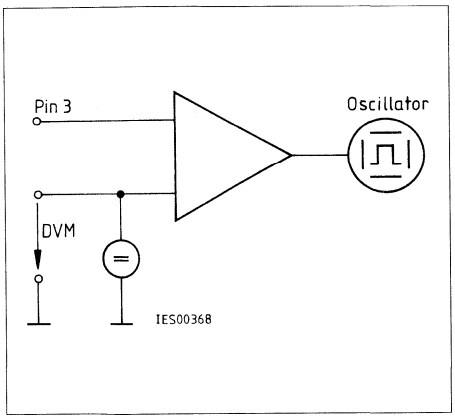


Remaining pins are connected as in test circuit 1
The 10 µF capacitor at pin 5 serves only for test purposes

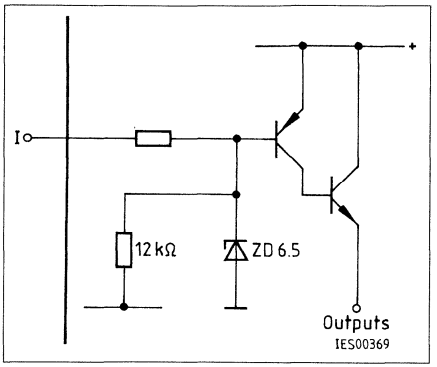
Test Circuit 4



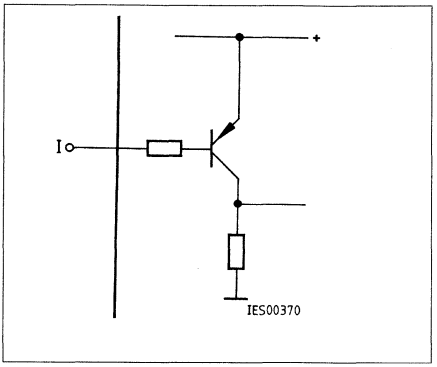
Test Circuit 5



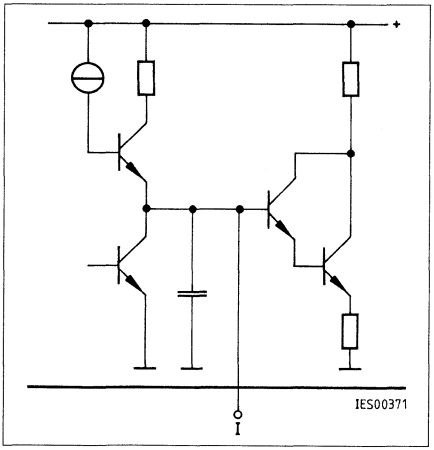
Test Circuit 6



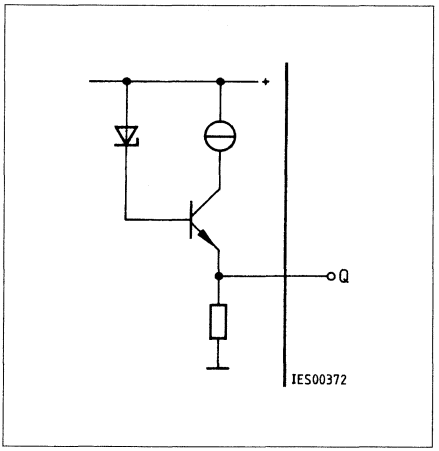
Inhibit 6



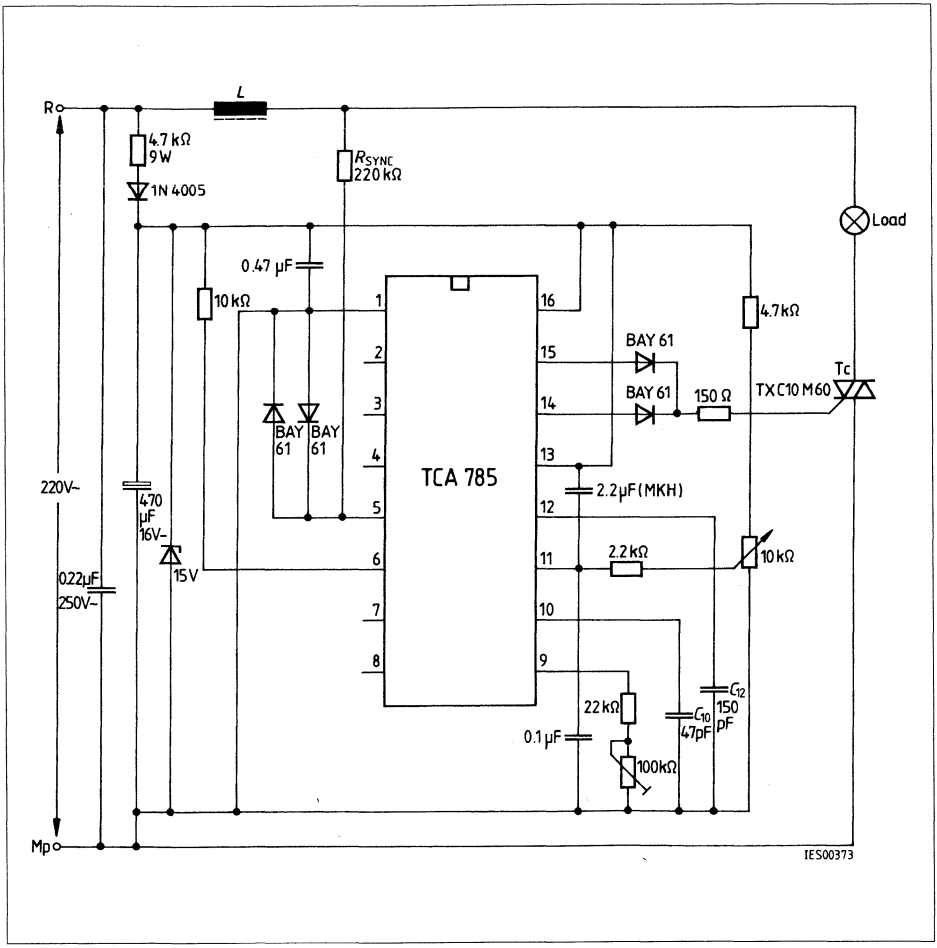
Long Pulse 13



Pulse Extension 12



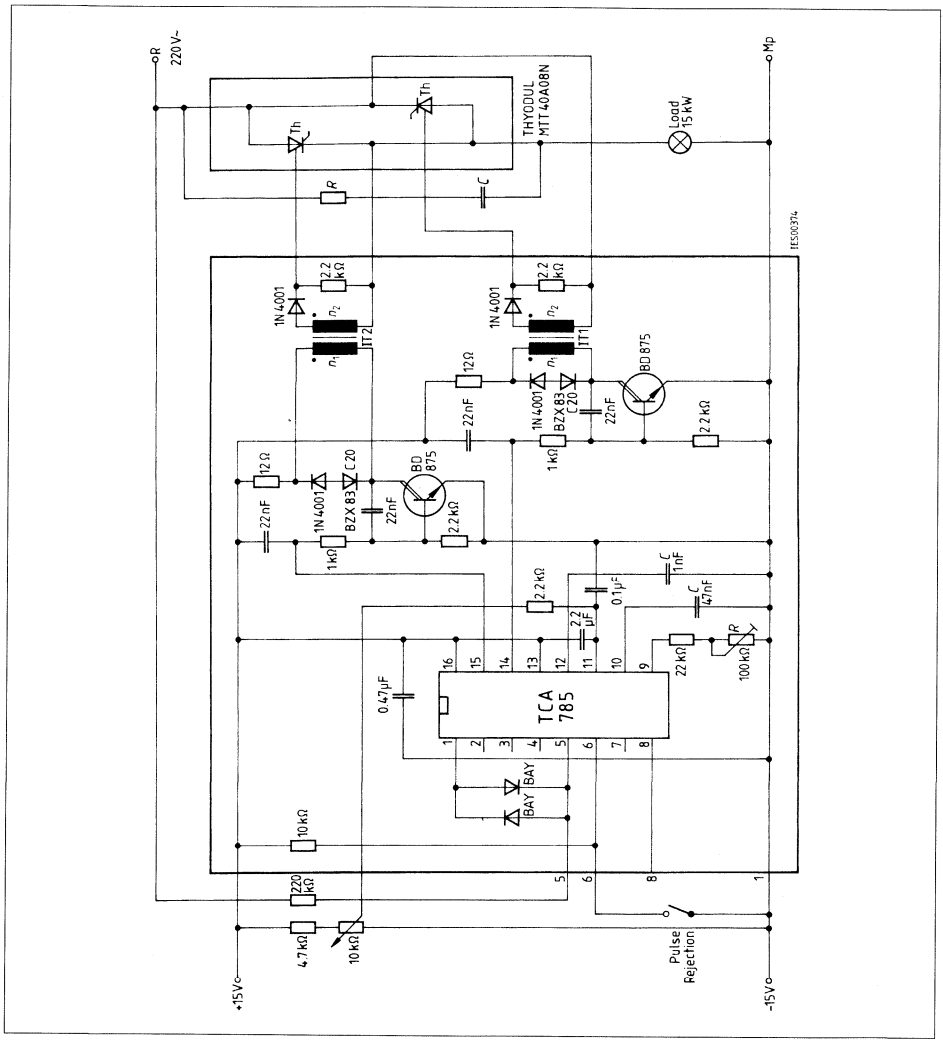
Reference Voltage 8



Application Examples

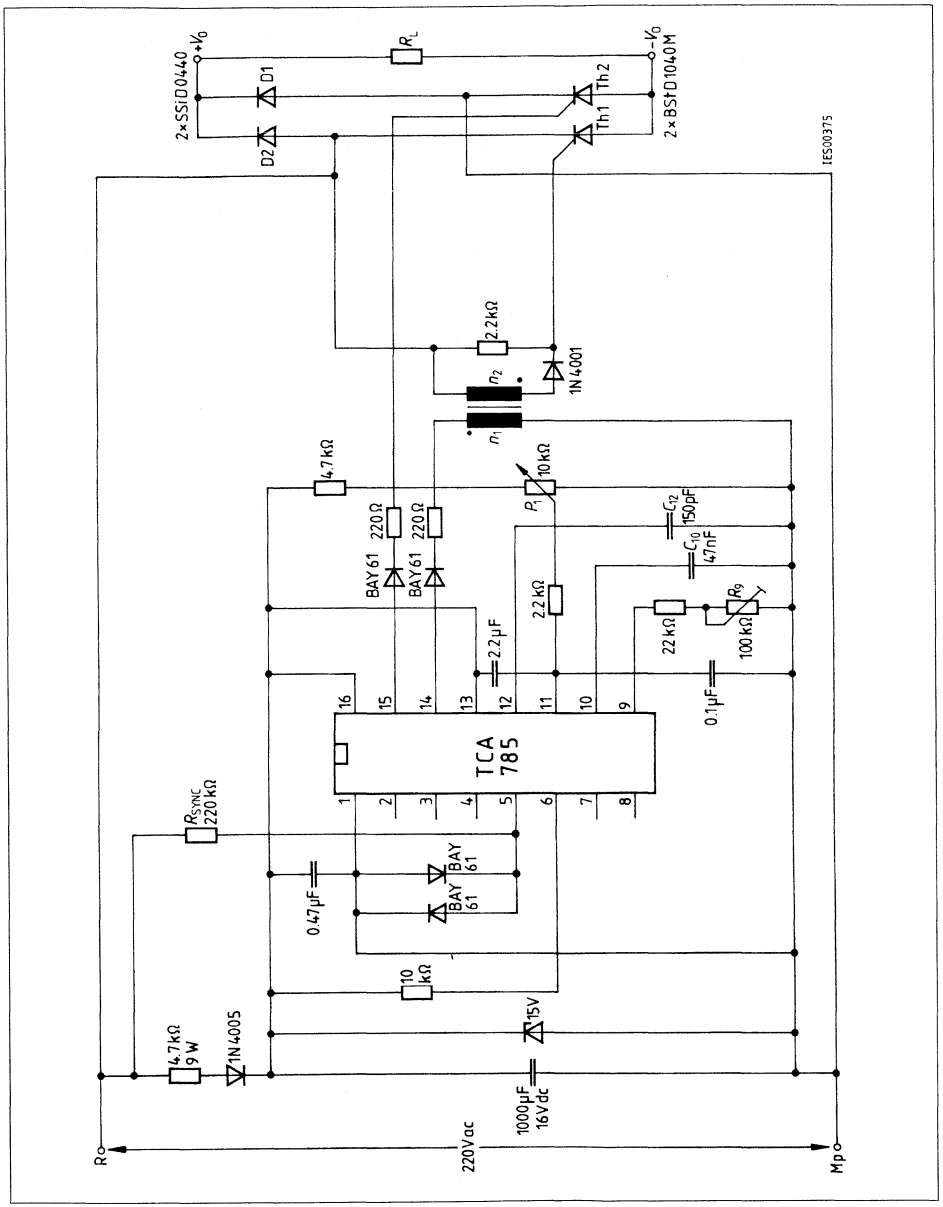
Triac Control for up to 50 mA Gate Trigger Current

A phase control with a directly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half-wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half-wave, it also receives a positive trigger pulse from pin 14. The trigger pulse width is approx. 100 µs.

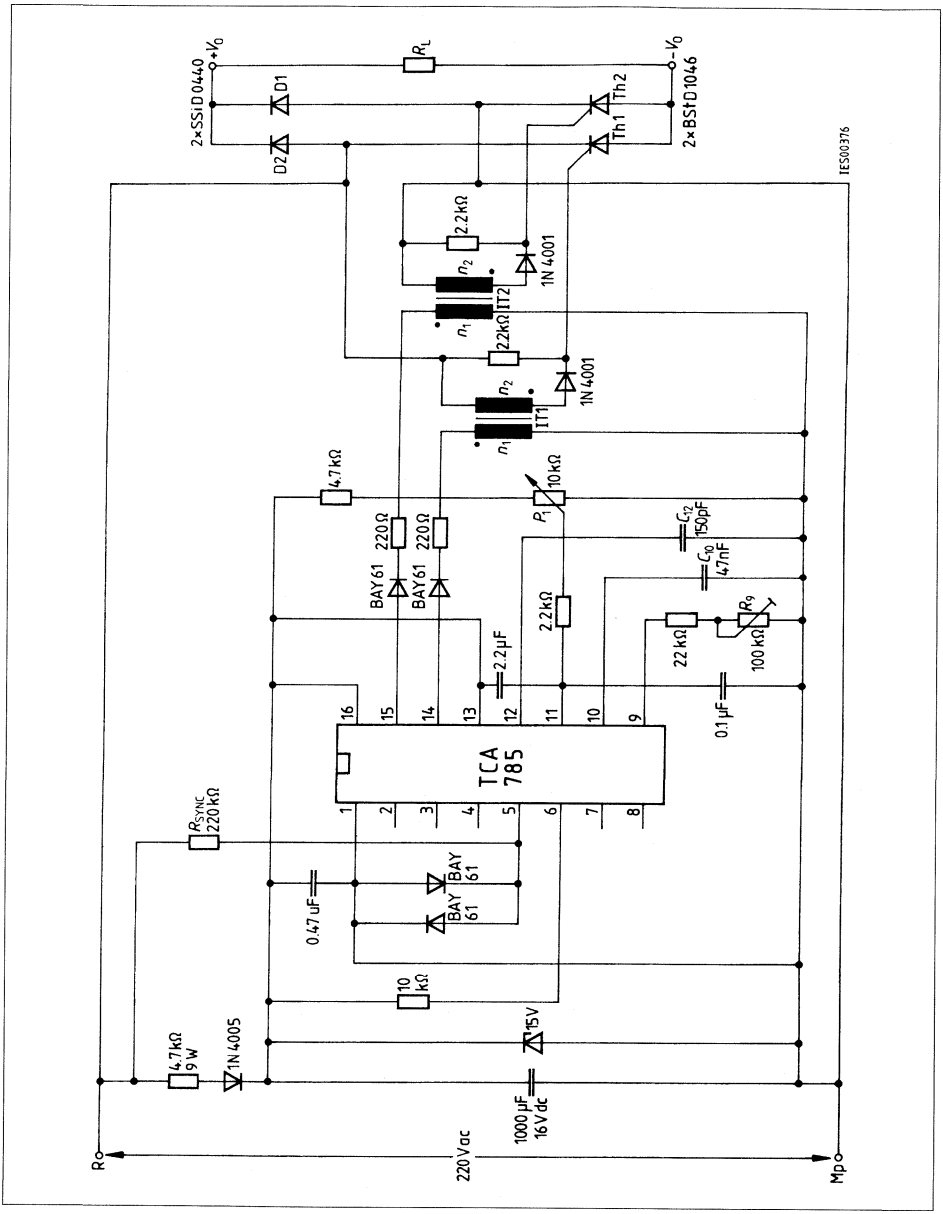


Fully Controlled AC Power Controller
Circuit for Two High-Power Thyristors

Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulse can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half-wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half-wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.



Half-Controlled Single-Phase Bridge Circuit with Trigger Pulse Transformer and Direct Control for Low-Power Thyristors



Half-Controlled Single-Phase Bridge Circuit with Two Trigger Pulse Transformers for Low-Power Thyristors

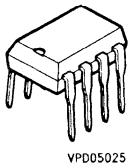
Dimmer IC

SLB 0586

CMOS IC

Features

- Sensor operation - no mechanically moved switching elements
- Operation is also possible from several extensions by means of sensors or push buttons
- Can replace electromechanical wall switches in conventional light installations
- Brightness control with a physiologically approximated linear characteristic
- Very high interference immunity, also against ripple control signals
- Very few peripheral components
- Programming input permits selection of three different functions (MODE A/B/C)
- "Soft" turn-ON with MODE A and C

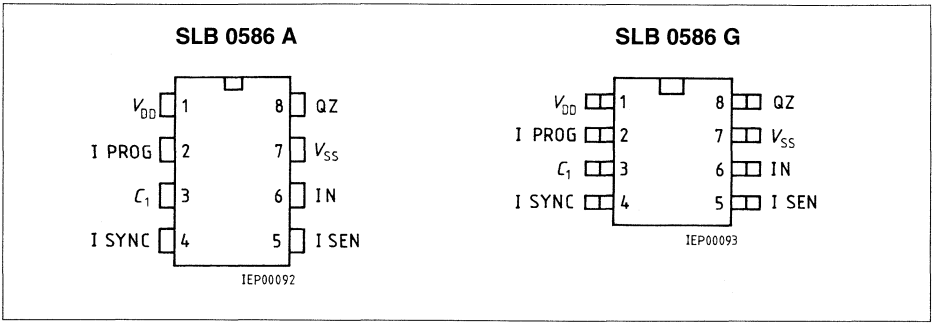


P-DIP-8

P-DSO-8-1

	Type	Ordering Code	Package
S	SLB 0586 A	Q67000-H8721	P-DIP-8
S	SLB 0586 G	Q67000-H8720	P-DSO-8-1 (SMD)

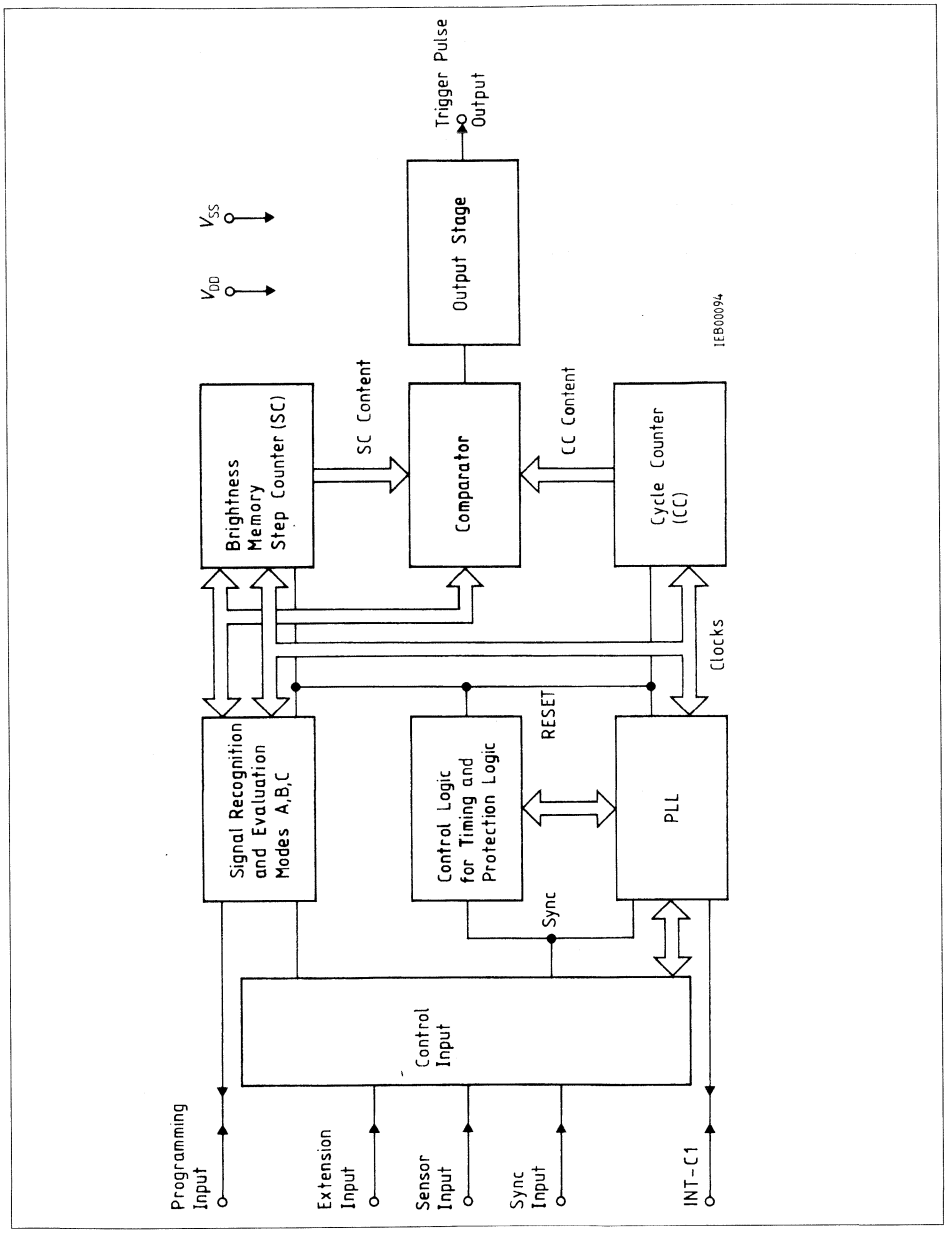
The SLB 0586 A and SLB 0586 G are integrated circuits in CMOS technology that permit the design of digital electronic dimmers. A single sensor or an equivalent extension input are used to turn the dimmer ON and OFF and to set the required brightness.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	V_{DD}	Ground
2	I PROG	Programming input
3	C_1	C_1 integrator
4	I SYNC	Sync input
5	I SEN	Sensor input
6	IN	Extension input
7	V_{SS}	Supply voltage
8	QZ	Trigger pulse output



Block Diagram

Functional Description

The SLB 0586 A permits the design of fully electronic dimmers for light bulbs (resistive loads) which are operated via a single sensor.

The integrated circuit replaces mechanical wall switches in conventional light circuit installations. All functions can be selected from several switching points (extensions).

The brightness is set by phase control. Its digital logic is synchronized with the line frequency (**see Block Diagram**).

It is possible to supply the IC via a two-wire connection, as the angle of current flow is limited to a maximum of 152 °C of the half wave.

Operation

The integrated circuit can distinguish the instruction "ON/OFF" and "Dimming" by the duration for which control input is operated i.e. the sensor is touched (**refer to figure 1**).

Turning ON/OFF

Short touching (50 to 400 ms) of the sensor area turns the lamp ON or OFF, depending on its preceding state. The switching process is activated as soon as the sensor is released.

Setting of the Brightness (Dimming)

If the sensor is touched for a longer period (> 400 ms), the angle of current flow will be varied continuously. It runs across its control loop in approximately 7.6 s (e.g. bright-dark-bright) and continues this sequence until the sensor is released.

Easy operation, even in the lower brightness range, is enabled by the following procedure: the phase control angle is controlled such that the lamp brightness varies physiologically-linear with the operating time and pauses for a short period when the minimum brightness is reached.

Using R_2 and C_4 in the application circuit the angle of current flow can be controlled between 40° and 148°.

Control Behavior

The three operating MODES A, B, C, differ in their control behavior. The required MODE is set with the programming input.

MODE A With turn-ON, the maximum brightness level is set; with dimming, control starts from the minimum brightness level. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

MODE B With turn-OFF, the selected brightness is stored and set again when the switch is turned on. Dimming starts at this stored value and the control direction is reversed with repeated dimming.

MODE C With turn-ON, the maximum brightness is set; with dimming, control is started from the minimum brightness. The control direction is reversed with repeated dimming.

Programming of the MODES

MODE A: $V_{I2} = V_{SS}$ (L)

MODE B: V_{I2} = open (tristate)

MODE C: $V_{I2} = V_{DD}$ (H)

V_{I2} = Level at pin 2

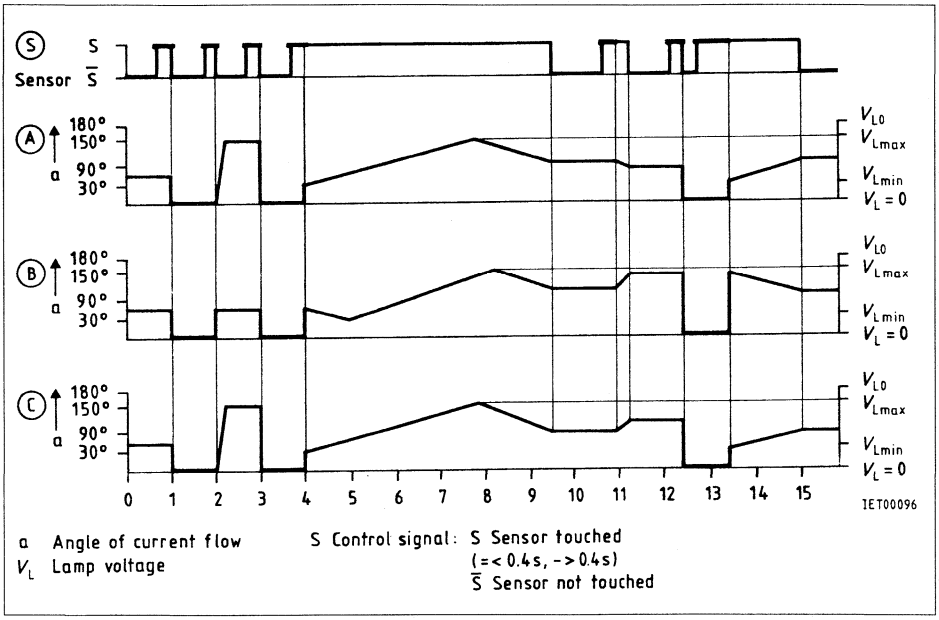


Figure 1
Control Behavior of Operating MODES
(schematic)

MODES A and C permit "soft" turn-ON; i.e. brightness is increased from 0 to maximum within 380 ms.

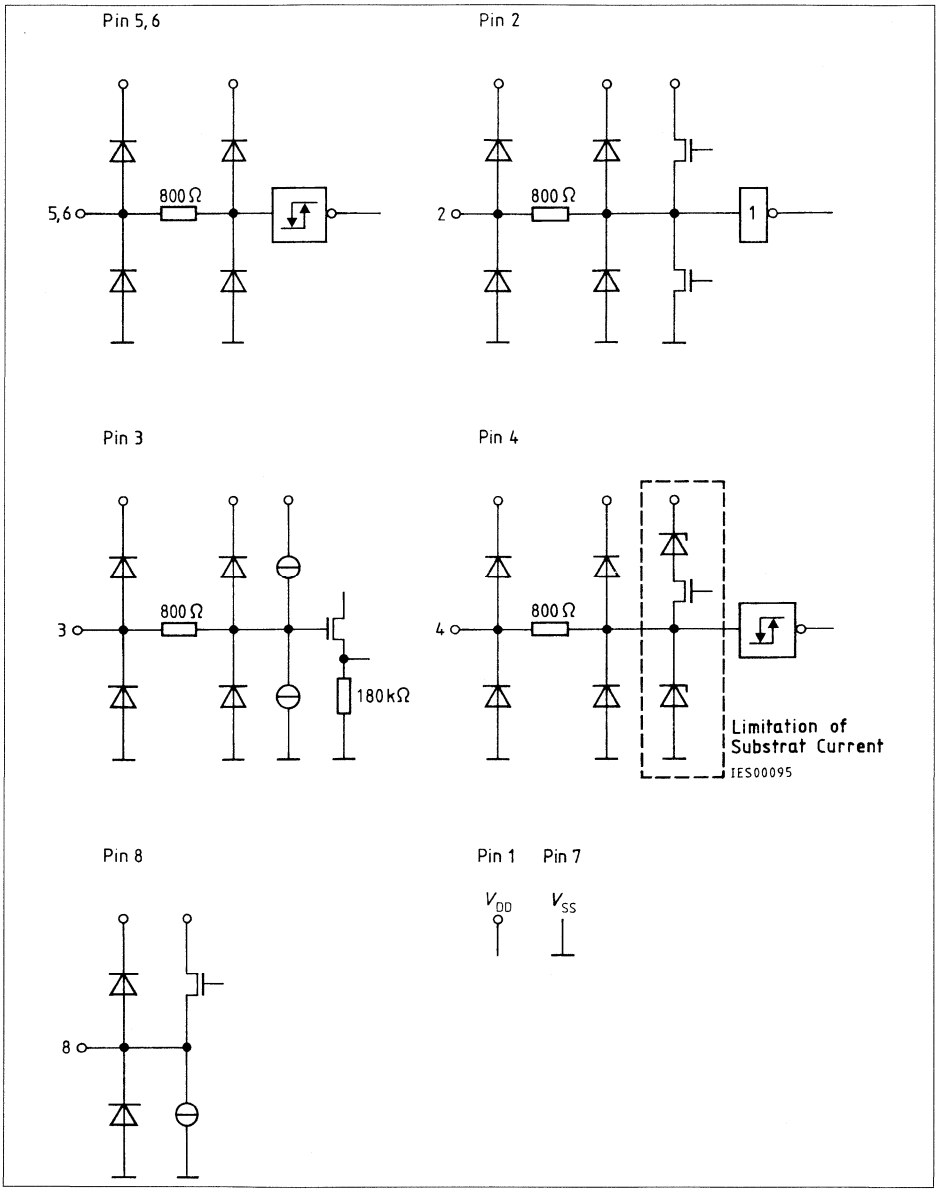


Figure 2

Internal Wiring of Pins

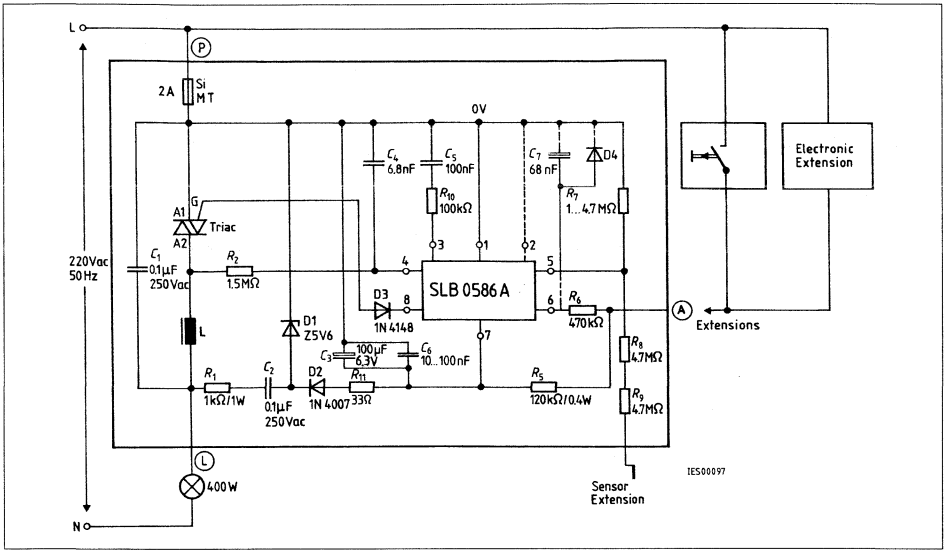


Figure 3
Application Circuit

The suggested circuit design of the SLB 0586 A performs the following functions:

- Current supply for the circuit (R_1, C_2, D1, D2, C_3).
- Filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4). For specific applications C_4 can be increased up to 33 nF, so that the lamp gets darker (**refer to figure 3**).
- Integration unit for internal PLL circuit (C_5, R_{10})
- Protection of the user (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in the case of reverse polarity of the extension (R_5, R_6).
  Both resistors can be omitted, if no extension is connected. In this case pin 6 must be interconnected with V_{SS} (pin 7).
- D3: Reduction of positive voltages which may arise during the triggered state at the gate of some triacs to values below V_{DD} + 0.3 V by diode forward voltage. If suitable triacs are used, diode D3 can be omitted.
- Dr: The choke and the capacitor C_1 are used for EMI suppression.
  Depending on the application, the EMI suppression is to be dimensioned in acc. with
  VDE 0875/part 1 (general)
  VDE 0550/part 6 (chokes)
  or corresponding to national regulations
  e.g. 1.4...2 mH, Q = 11...24

- The components C_6 10...100 nF ceramic
  C_7 33...68 nF
  D_4 Ge or Schottky diode
  R_{11} 33...68 Ω
  serve to improve interference immunity under special conditions like for example:
  - high-frequency line interferences
  - long extension lines with high earth capacitances
  - supply line resistances in the load circuit
    and can therefore be dropped for normal operating conditions.
- At 110 V/60 Hz line:
  C_2: 150 nF/160 Vac
  R_2: 680 kΩ

Application Notes

1.Synchronization

Interference of the synchronization can be suppressed by setting the C_4 filter capacitor at the sync input between 3.3 and 33 nF. By increasing the C_4 value the range of the controllable conduction angles goes to less minimum brightness. At the same time, the immunity against superimposed interference from the line improves, so that, for example, with C_4 = 33 nF an interference amplitude of 30 V does not cause any synchronization errors in the range of 150 to 1500 Hz.

C_4 (nF)	Conduction angle (°)	Interference amplitude (V)
3.3	151 to 43	20
6.8	148 to 40	↓
10.0	147 to 39	↓
15.0	144 to 36	↓
33.0	136 to 28	30

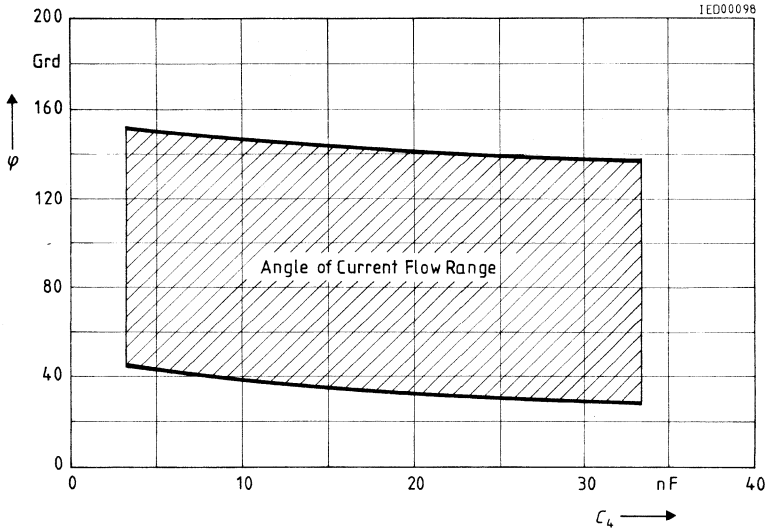
2. PLL Circuit

The PLL circuit at pin 3 can be varied to reach a minimum of flickering and a maximum of noise immunity. The PLL circuit is adjusted to a capacitor value of 100 nF.

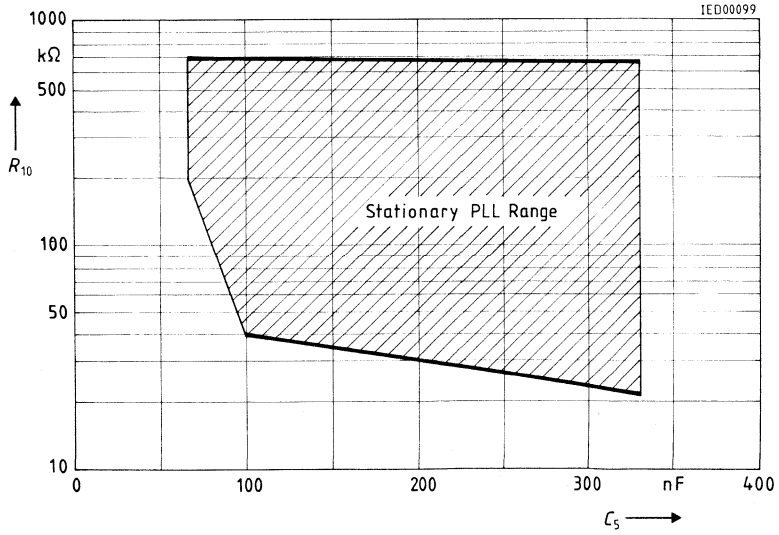
R_{10} can be varied in the range of 22 kΩ to 680 kΩ (**figure 5**). Here higher resistances speed up the response of the PLL circuit.

Hence it is possible to reduce the jitter of the trigger pulse to below 0.5 ms by a low-resistance R_{10} at low interference frequencies (≤ 400 Hz) and a high-resistance R_{10} at high interference frequencies. This will greatly reduce brightness modulations through interferences.

3. Dependence of C_4 and Angle of Current Flow (Figure 4)



4. Range of Value of the RC-Component at Pin 3 for Stationary PLL-Operation (Figure 5)



5. Extensions

All switching and control functions can also be performed from extensions which are connected to the extension input. The main sensor input and the extension inputs have equal priority. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation "H" potential must be applied to the extension input for both half cycles.

Note

The extension input must be connected to V_{SS}, if this input is not required.

Operation of the Control Inputs

Input potential during both half waves of the line phase:

Function	Line Half Wave	Sensor Input	Extension Input		
Operated	positive	L	H		
	negative	0	H		
Not operated	positive	H	L	or	0
	negative	0	0		L

Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0586 A can be performed with the aid of a single transmission channel.

6. Interference Immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs and additionally allows almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In case of power failure the set switching state with the recommended external circuitry remains stored. After prolonged power failure ($V_{SS} > -3.6$ V) the circuit turns into OFF-state.

The control characteristic of the synchronous oscillator (PLL circuit) is designed such that interference due to ripple control signals may cause slight variations in brightness. However, they will not lead to a malfunction of the dimmer.

7. General Information

All time specifications refer to a line frequency of 50 Hz. In case of a line frequency of 60 Hz, the times are reduced accordingly.

8. Functional Description of Evaluation Logic for Sensor and Extension Inputs

The logic status at the sensor and extension inputs are sampled by latches L1 and L2 using the time slot pattern shown in the timing diagram (**figure 6**).

For operation (ON/OFF or DIMMING) "1" must be present at the D input of FF1 for two consecutive rising edges of the 50 Hz clock pulse of the internal PLL. The flipflops FF1 and FF2, are reset by two logic zeros occurring at the same time at latch outputs L1 and L2.

For operation via the extension input five consecutive sampling values must be "1". The minimum immunity time is therefore approx. 24 ms. Due to the different sampling rates, two sampling values of "1" must follow at the sensor input for an operation to be recognized. In this case the minimum immunity time is approx. 39 ms.

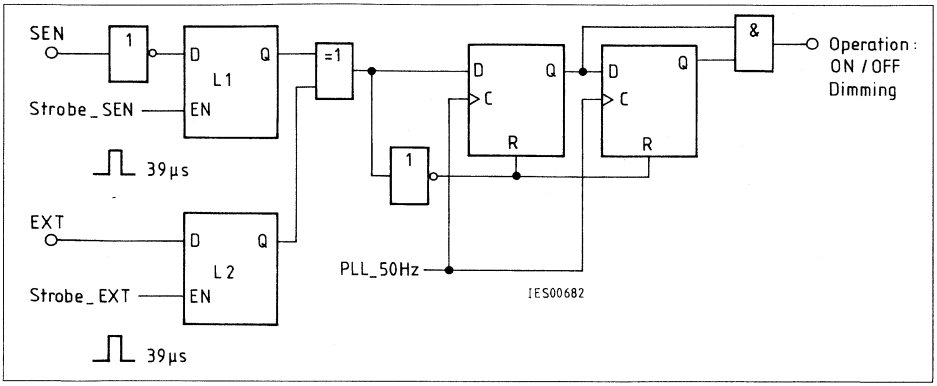


Figure 6

Schematic Circuit Diagram of Evaluation Logic for Sensor and Extension Inputs

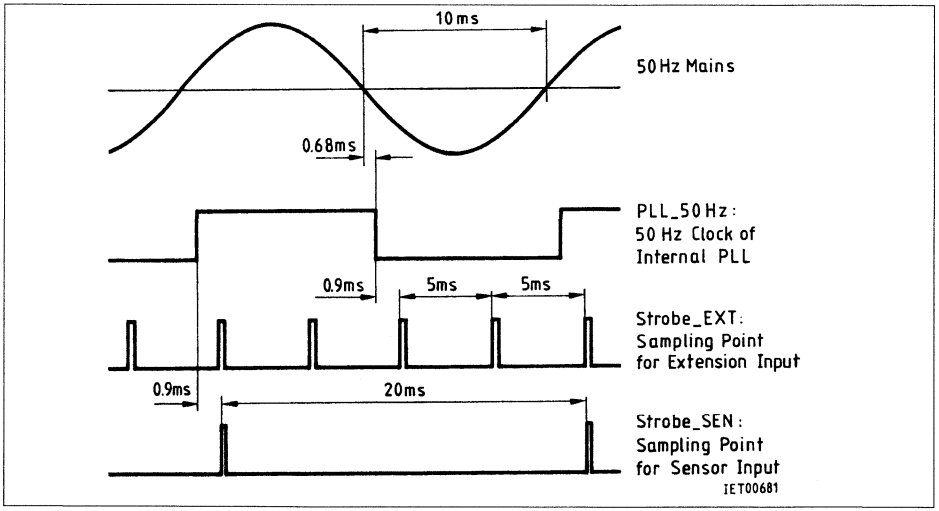


Figure 7

Timing Diagram of Evaluation Logic for Sensor and Extension Inputs

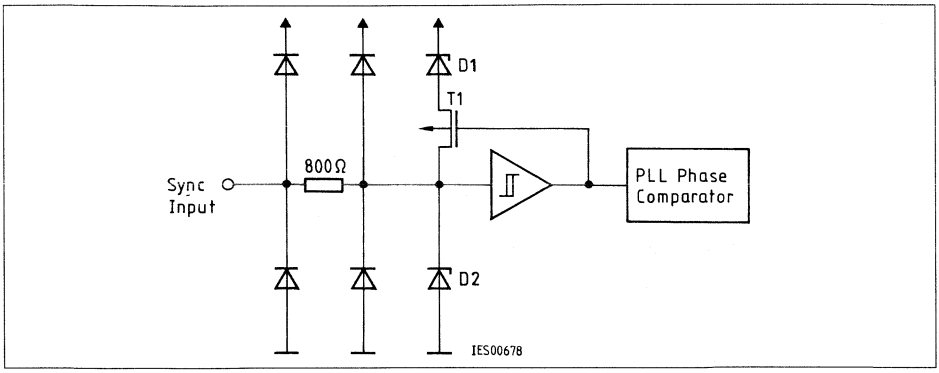


Figure 8

Schematic Circuit Diagram at Synchronous Input

Functional Description

Diodes D1 and D2 have characteristics similar to Z-diodes and start conducting at about 2.5 V.

In spite of the line voltage at the triac it is ensured - by using R_2 - that the voltages present at the synchronous input of SLB 0586 A remain within the supply voltage level.

To obtain a highly stable trigger point for the phase comparator, T1 becomes conductive only after recognizing the synchronization edge.

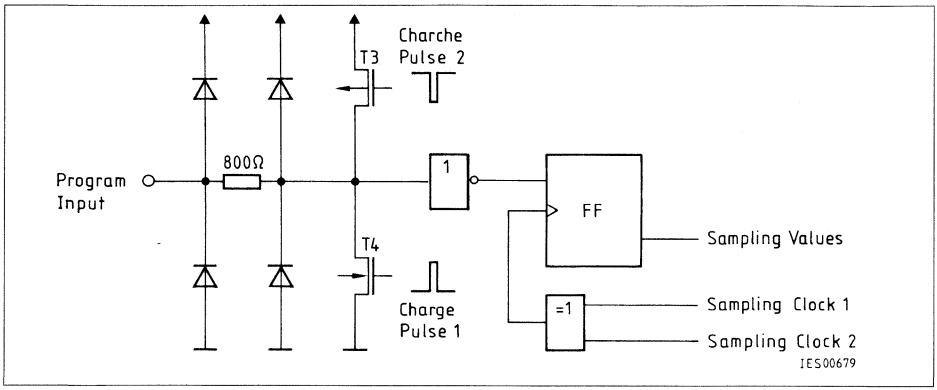


Figure 9

Schematic Circuit Diagram at Programming Input (Pin 2)

Functional Description of Pin 2 (Programming Input)

The SLB 0586 A provides the possibility of differentiating between types A, B, and C by appropriate connection of pin 2.

Depending on the charge pulses shown in **figure 9** transistors T3 and T4 alternate in becoming conductive. The currents flowing during the conductive phase of the transistors are sufficient for a charge reversal of the load capacitance of 7 pF max. present at pin 2.

It is important that no major discharge of the capacitance present at pin 2 occurs from the time of charge reversal until the sampling of the voltage level by the two sampling clocks.

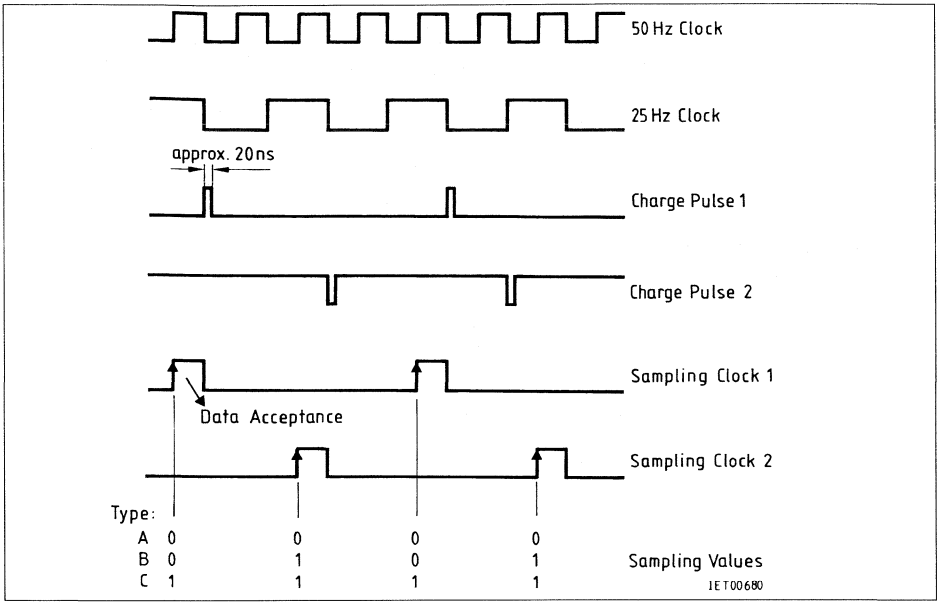


Figure 10

Internal Timing for Differentiating between the three Possible Modes A, B, and C

Absolute Maximum Ratings

V_{DD} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SS}	– 7.5	0.3	V
Input voltage	V_I	V_{SS} – 0.3	0.3	V
Input current	I_I	– 0.5	0.5	mA
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 55	125	°C
Total power dissipation (T_A = 25 °C)			10	mW
Thermal Resistance				
System-air P-DIP-8	$R_{th\ SA}$		135	K/W
System-air P-DSO-8	$R_{th\ SA}$		231	K/W
Operating Range				
Supply voltage	V_{SS}	– 5.6	– 4.5	V
Line frequency	f	47.5	63	Hz
Ambient temperature	T_A	0	80	°C

Characteristics

T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current (Pin 1)	I_{DD}			0.45	mA	f_{sync} = 50 Hz
Sensor Input (pin 5)						
H-input voltage	V_{IH}	1/2 V_{SS}+1.1			V	
L-input voltage	V_{IL}			1/2 V_{SS}-1.1	V	
Input current	I_{IH}		33	37	µA	220 V at sensor input and series resistor
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		line sine wave			
Frequency with active signal	f		50/60		Hz	synchronized with 50/60 Hz clock at sync input

Characteristics (cont'd)
T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Extensions (pin 6)						
H-input voltage	V_{IH}	1/2 V_{SS}+1.1			V	
L-input voltage	V_{IL}			1/2 V_{SS}-1.1	V	
Input current	I_{IH} I_{IL}	– 1 0		0 1	µA µA	V_I = 0 V V_I = V_{SS}
Sync Input (pin 4)						
H-input voltage L-input voltage Input current	V_{IH} V_{IL} I_{IH}	1/2 V_{SS}+1.8	 207	1/2 V_{SS}-1.8	V V µA	with series resistor 1.5 MΩ from 220 V line*)
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}		supply sine wave			
Frequency	f		50/60		Hz	
Programming Input (pin 2)						
Load capacitance through board with tristate	C_L			7	pF	
Integrator (pin 3)						
Application circuit	C_5 R_{10}	68 22	100 100	330 680	nF kΩ	
Output (pin 8)						
L-output current	I_Q	25			mA	V_{QL} = – 3 V
L-pulse width	t_{QL}			39.0 32.6	µs µs	50 Hz supply 60 Hz supply
HL transition time	t_{HLQ}			5	µs	
LH transition time	t_{LHQ}			5	µs	

*) see Application Circuit

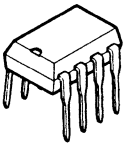
SIEMENS

Dimmer IC for Halogen Lamps — SLB 0587

Preliminary Data — **CMOS IC**

Features

- Phase control for resistive and inductive loads
- Sensor operation – no machanically moved switching elements
- Operation possible from several extensions
- Capable of replacing electromechanical wall switches in conventional light installations
- High interference immunity, even against ripple control signals
- Programming input for selection of three different functions (mode A/B/C)
- Soft start
- Safety turn-OFF



P-DIP-8

P-DSO-8-1

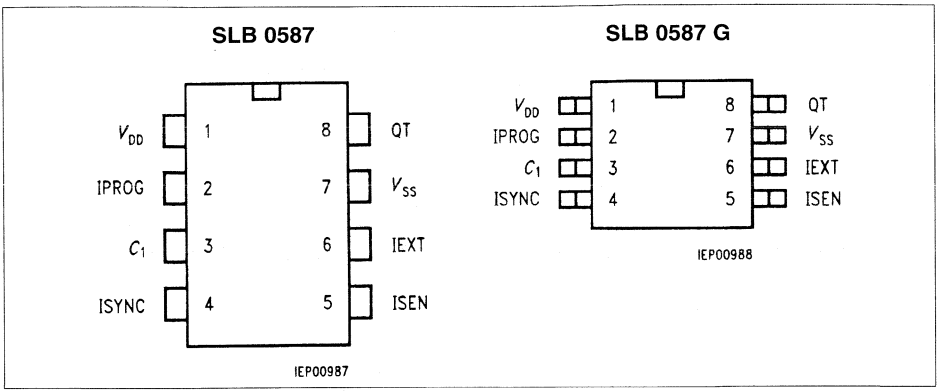
	Type	Ordering Code	Package
S▼	SLB 0587	Q67100-A8310	P-DIP-8
S▼	SLB 0587 G	Q67106-A8315	P-DSO-8-1 (SMD)

▼ New Type

For applications where the SLB 0586 A has been used, it is possible to replace the SLB 0586 A by the SLB 0587 if the appropriate external wiring in accordance with the data sheet is maintained.

The SLB 0587 is a CMOS IC and the advanced version of the version SLB 0586 A.

The IC permits the design of digital electronic phase controls for operation of incandescent lamps, low-voltage halogen lamps with in-series connected transformers, and universal as well as split-pole motors.



Pin Configuration (top view)

6

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	Reference point (OV)
2	IPROG	Programming input
3	C_1	C_1 integrator
4	ISYNC	Synchronizing input
5	ISEN	Sensor input
6	IEXT	Extension input
7	V_{SS}	Supply voltage
8	QT	Trigger pulse output

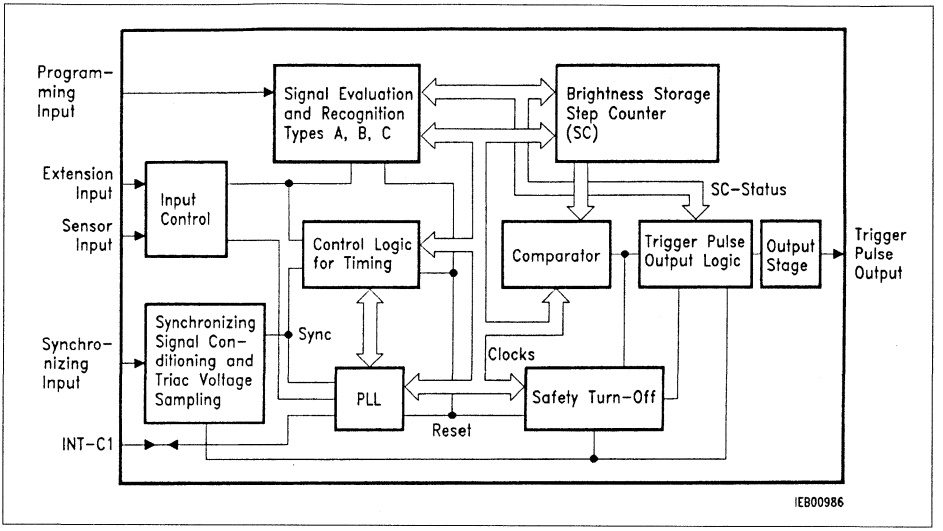


Figure 1
Block Diagram

Functional Description

With the SLB 0587 it is possible to generate one defined current pulse per line half cycle. Together with a triac and a few extra passive components, a line-powered phase-control circuit can be designed. The phase-control angle (turn-ON time of the triac) can be set on the two control inputs, pins 5 and 6, of the IC.
The voltage supply to the IC in a two-wire connection is ensured by limiting the angle of current flow to approx. 152°. This makes it simple to exchange mechanical wall switches in conventional lighting installations. The IC's internal logic is synchronized with the line by PLL. Thus a phase control range independent of the line frequency is obtained.

Operation with Low-Voltage Halogen Lamps

In normal, resistive operation of a phase control circuit there is alternately part of the positive and negative line-voltage half cycle applied to the load via the triac that has started to conduct because of the trigger pulse. Operation of the circuit with a transformer and low-voltage halogen lamp connected is largely identical to the operation of a normal filament lamp due to the primarily resistive nature of the load. In operation with resistive and inductive portions of load, the zero crossing of the current compared to that of the line voltage line is delayed.
In operation with heavily inductive loads (eg an idling transformer after lamp failure), a highly lossy state (half cycle operation) can occur after a fault, leading to thermal destruction of the transformer. Control mechanisms integrated into the SLB 0587 serve to protect the load from this situation.

If, for instance, a trigger pulse is missing in a half cycle because of a fault, there will be a considerable increase in current in the transformer into the line shortly after the zero crossing of a voltage wave – after the next firing of the triac at large phase-control angles. If the next trigger pulse comes into phase when the triac is still conducting because of the inductive current lag, it has no effect. It is only the subsequent trigger pulse that will fire the triac again.

The case described above, where only one trigger pulse per line cycle leads to firing of the triac, can turn into a steady-state condition in the absence of further measures.

The SLB 0587 provides the following features to prevent Steady-State Half-Cycle Operation:

1) Allowance for the conducting state of the triac when setting the trigger pulses. If a trigger pulse, determined by the set firing angle and status of the internal PLL, coincides with the conducting phase of the triac, the trigger pulse will not be output to the triac until after the zero crossing of the current wave.

2) Detection of high saturation currents at angles of current flow of more than 180° by sampling the synchronizing input levels.
If the frequency of such peak situation current exceeds a value defined in the IC, there will be a safety cut-out.

3) Retriggering if the triac does not remain triggered after the trigger pulse.This can occur in particular on highly inductive loads (idling transformer with a small magnetizing current) and insensitive triacs. Approx. 1.5 ms after each trigger pulse from SLB 0587 the conducting state on the triac is sampled via pin 4 of the IC. If the triac still remains turned off, one-shot retriggering will follow. If the frequency of retriggering exceeds an internally defined limit value, there will be a cutout.

Safety Cutout

The purpose of the safety cutout is to prevent thermal destruction of primarily inductive loads (idling transformer) in the event of very lossy instances of operation. Despite the safety precautions that are integrated, you should only use transformers with thermal protection.

Safety cutout occurs when the count of an 4-bit up/down counter reaches 15. The count is determined by the ratio of the up/down counting rates. The up-counting rate is the appearance of high saturation currents and retriggering. A down counting increment is produced when the count is other than zero at every fifteenth line half-wave. The count is zeroed in the off state and when short line outages are detected.

Operation (Figure 3)

The integrated circuit can distinguish the instructions ON/OFF and Change of Phase Control Angle by the duration of sensor touching.

Turning ON/OFF

Short touching (50 to 400 ms) of the sensor area turns the lamp ON or OFF, depending on its preceding state. The switching process is activated as soon as the sensor is released.

Setting of the Phase Control Angle

If the sensor is touched for a longer period (exceeding 400 ms) the angle of current flow will be varied continuously. It runs accross the control loop in approximately 7.6 s up and down (e.g. bright – dark – bright) until the sensor is released.

Easy operation, even in the lower brightness range of incandescent lamps, is enabled by the following procedure:
The phase control angle is controlled such that the lamp brightness varies physiologically linear with the operating time and pauses for a short period when the minimum brightness is reached.
Using R_2 and C_4 (synchronizing input) in the application circuit **(figure 4)**, the angle of current flow can be controlled for purely resistive loads between 45° and 152° of the half-wave.

Control Modes of Operation

Mode	Period of Touching the Sensor/Extension			
	Short (60 to 400 ms)		Long (more than 400 ms)	
	Pre-Touch Status	Post-Touch Status	Pre-Touch Status	Post-Touch Status
A (Pin 2 at V_{SS})	OFF Max. Intermediate	Softstart to Max. OFF OFF	OFF Max./Intermediate Repeated dimming	Starts varying at min. Starts varying at pre-touch brightness Same dimming direction
B (Pin 2 open)	OFF Max. Intermediate	Softstart to stored brightness from last turn-OFF OFF OFF	OFF Max./Intermediate Repeated dimming	Softstart to stored brightness and varying Starts varying at pre-touch brightness Reversed dimming direction
C (Pin 2 at V_{DD})	OFF Max. Intermediate	Softstart to Max. OFF OFF	OFF Max./Intermediate Repeated dimming	Starts varying at min. Starts varying at pre-touch brightness Reversed dimming direction

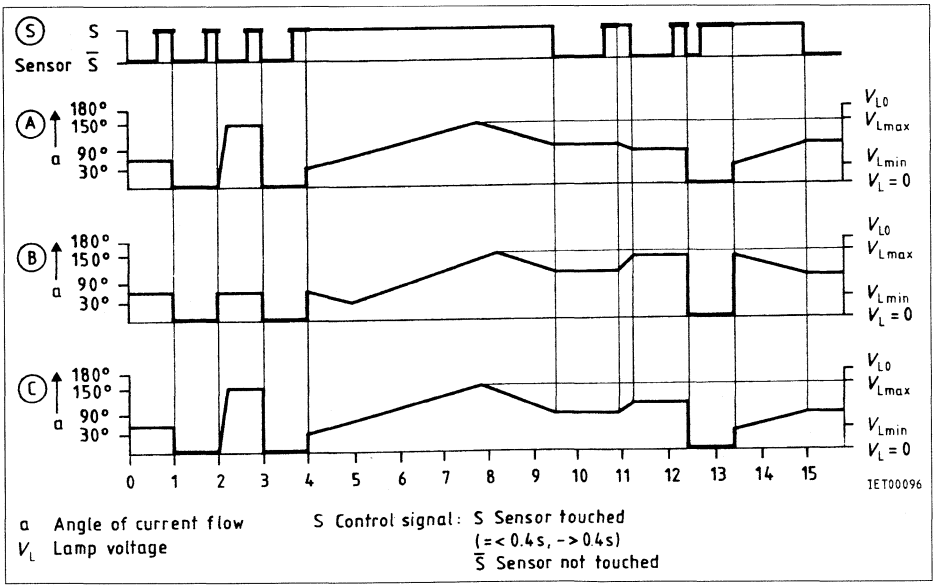


Figure 3
Control Behaviour of the 3 Operating Modes

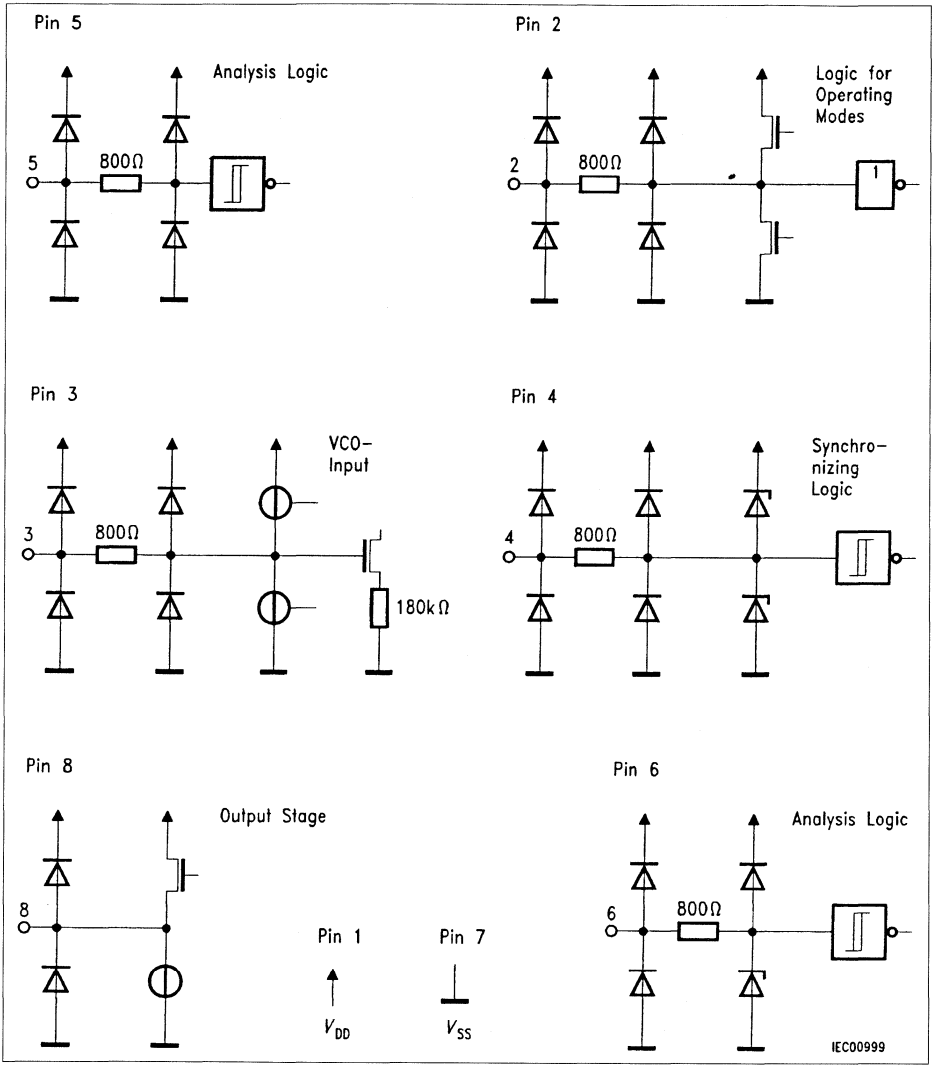


Figure 2
Internal Wiring of Pins

Interference Immunity

Components C_3, C_6 and R_3 **(figure 4)** provide for a stable operating voltage and thus for error-free working of the circuit, even in the presence of high frequency line interferences (e.g. caused by cutting in and out of mainly active loads).

In the event of short line interruption ($\leq$ 200 ms) the set circuit state with the external wiring shown in **figure 4** will be maintained. After prolonged line outages ($V_S \leq -3.6$ V) the circuit will go into the OFF-state.

Upon line outage the synchronization of the internal logic with the line is lost. If the line outage lasts less than three line cycles, the phasing in of the PLL becomes visible by a brief flickering. The setting of the PLL can be influenced within certain limits by the selection that is made with C_5 and R_{10}. In general terms, smaller ratings for C_5 and larger ratings for R_{10} will produce shorter settling times of the PLL.

With more inert PLL characteristics there are slightly better values for rippe-control stability (visible fluctuations in brightness when operating incandescent lamps and with ripple-control signal on the line).

If line outages last more than three line cycles, there is blanking for approx. 200 ms after the line recovers so that the settling process of the PLL is not visible.

Operation of Extensions

Long extension lines in installations cause voltages to be coupled in because of their stray capacitances and phase capacitances. Internal limiting structures and appropriate evaluating logic ensure that the circuit can work without interference for stray and phase capacitances up to 100 nF. Even voltage drops up to 10 V in the phase conductor between the circuit and the extension button being in phase with the dimming voltage have no effect on the working of the circuit.

Especially at operation with long extension lines, the RC-network R_{10}, C_5 should be connected between pins 3 and 7 **(figure 4)**.

Application Circuit (Figure 4)

The suggested circuit design of the SLB 0587 performs the following functions:

- Current supply for the circuits (R_1, R_3, C_2, C_3, C_6, D1, D2).
- Filtered signal for synchronization of the internal time base (PLL circuit) with line frequency (R_2, C_4).
- For specific applications C_4 and R_2 can be varied according to **figure 5**. An increase for C_4 and R_2 causes a slight reduction of the lamp brightness but at the same time an improvement of interference immunity of the internal PLL against line voltage spikes.
- Integration unit for internal PLL circuit (C_5, R_{10})
  Combining R_{10} and C_5 **(figure 6)** determines within certain limits the following factors
  - Start-up behaviour of internal PLL after line failure
  - Ripple control behaviour (periodic shifts of lamp brightness if ripple control signals represent)
- Protection of the user (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in the case of reverse polarity of the extension (R_5, R_6)
  Both resistors can be omitted if no extension is connected. In this case pin 6 must be connected to V_{SS} (pin 7).
- D3: Reduction of positive voltages which may arise during the triggered state at the gate of some triacs, to values below V_{DD} + 0.3 V by diode forward voltage. If suitable triacs are used, diode D3 can be omitted.
- Dr, C_1 are used for EMI suppression.
  Depending on the application the EMI suppression is to be dimensioned in acc. with
  VDE 0875/part 1 (general)
  VDE 0550/part 6 (chokes)
  or corresponding the national regulations e.g. 1.4....2 mH, Q = 11....24

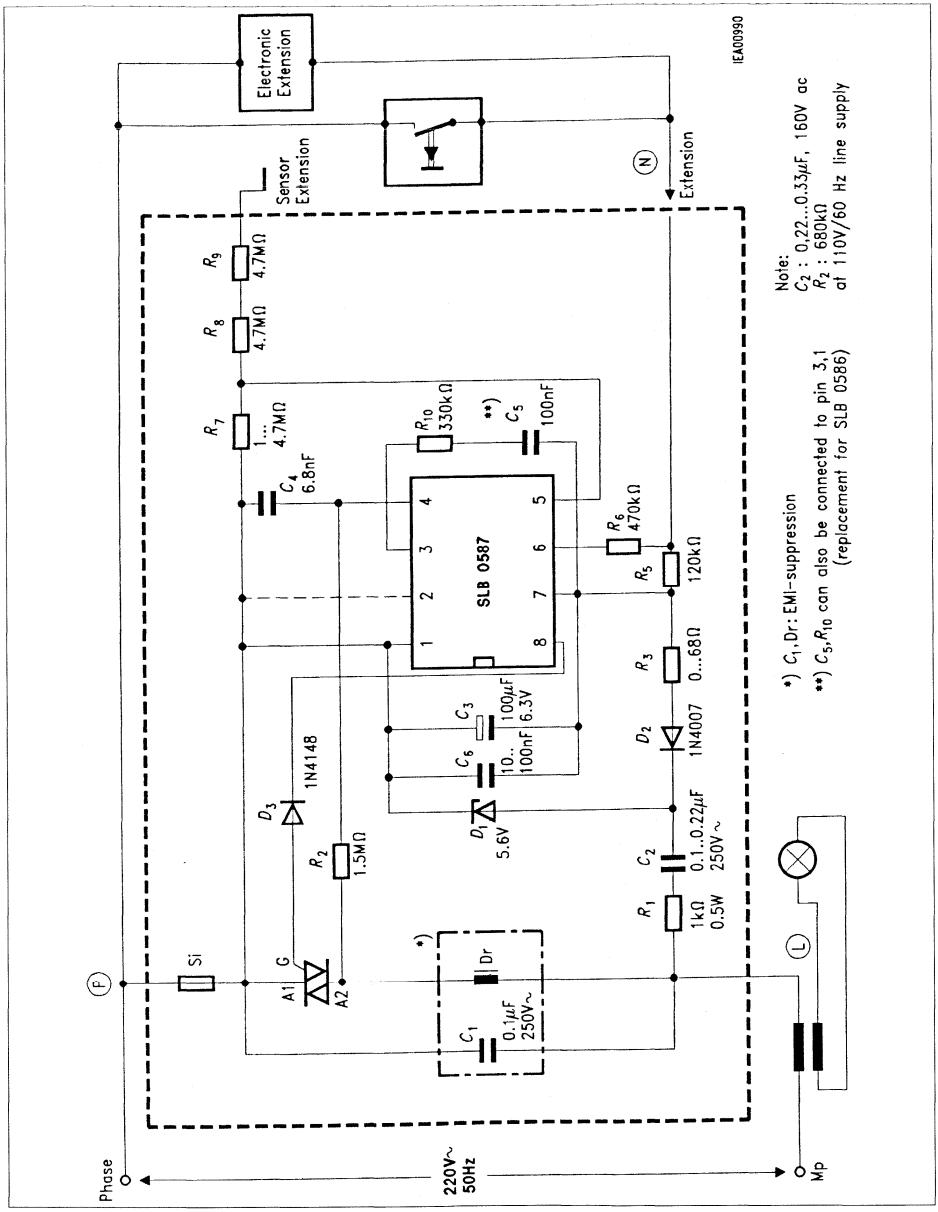


Figure 4
Application Circuit

Application Notes

Figure 5
Dependence of C_4 and Angle of Current Flow

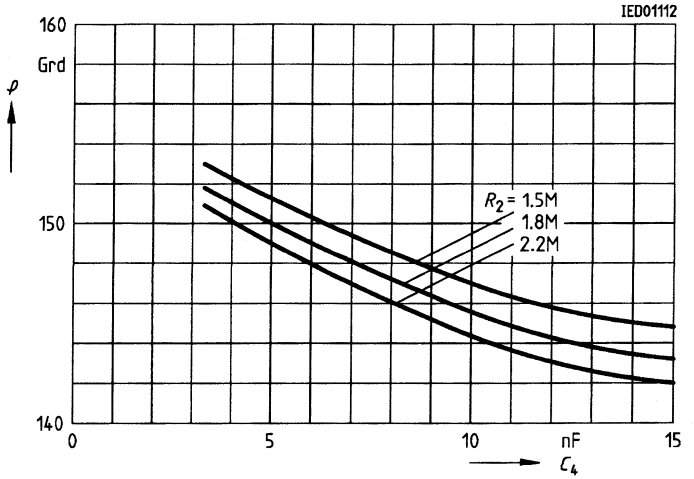


Figure 6
Range of Value of the RC-Component at Pin3 for Stationary PLL-Operation

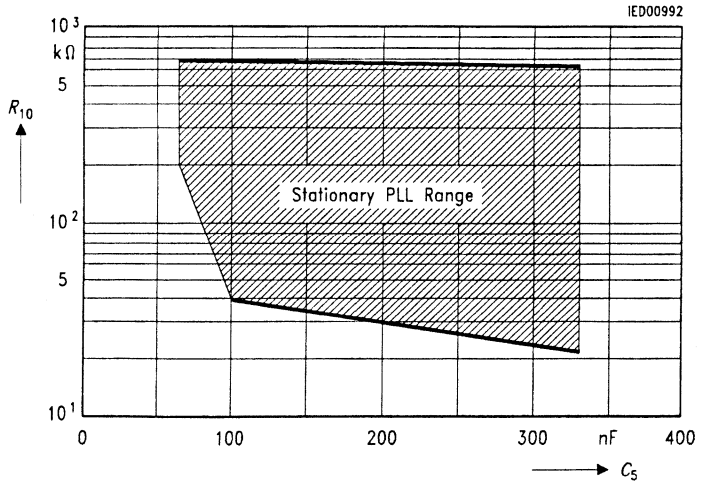
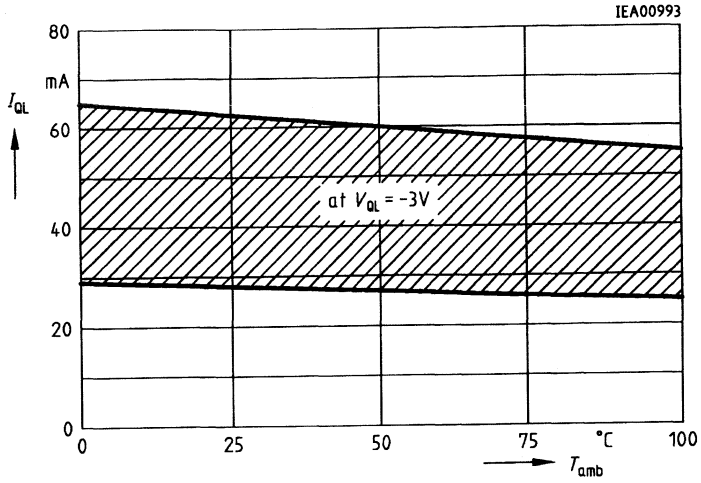


Figure 7
Range of Value for Trigger Current of Pin 8 over Temperature Range



6

Operation of Control Inputs

All switching and control functions can also be performed from extensions which are connected to the extension input. The main sensor input and the extension inputs have equal priority. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions.

Input potential during both half waves of the line phase:

Function	Line Half Wave	Sensor Input	Extension Input		
Operated	positive	L	H		
Not operated	negative	don't care			
Operated	positive	H	L	or	don't care
Not operated	negative	don't care	don't care		L

Functional Description of the Evaluation Logic for Sensor and Extension Inputs

The logic levels at the sensor and extension inputs are sampled by latches L1 and L2 using the timing pattern shown in the timing diagram of **figure 8**.

For operation (ON/OFF or change of brightness) flipflops FF1 to FF3 must be "1".

Minimum ON/OFF Times

Extension Input: approx. 40 to 60 ms
Sensor Input: approx. 40 to 60 ms

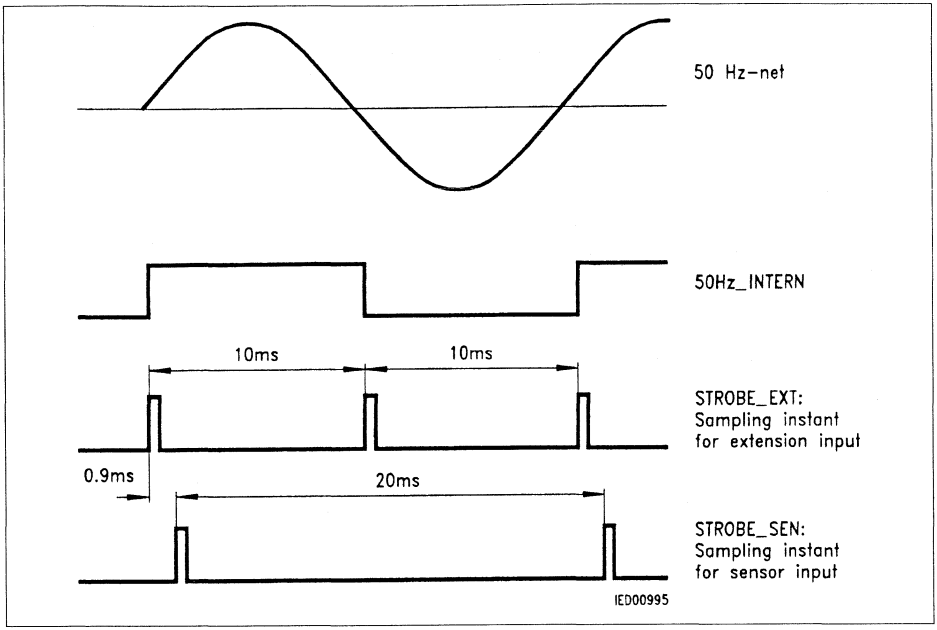


Figure 8
Timing Diagram of the Evaluation Logic for the Sensor and Extension Inputs

Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0587 can be performed with the aid of a single transfer channel.

General Information

All time specifications refer to a line frequency of 50 Hz. In case of a line frequency of 60 Hz, the times are reduced accordingly.

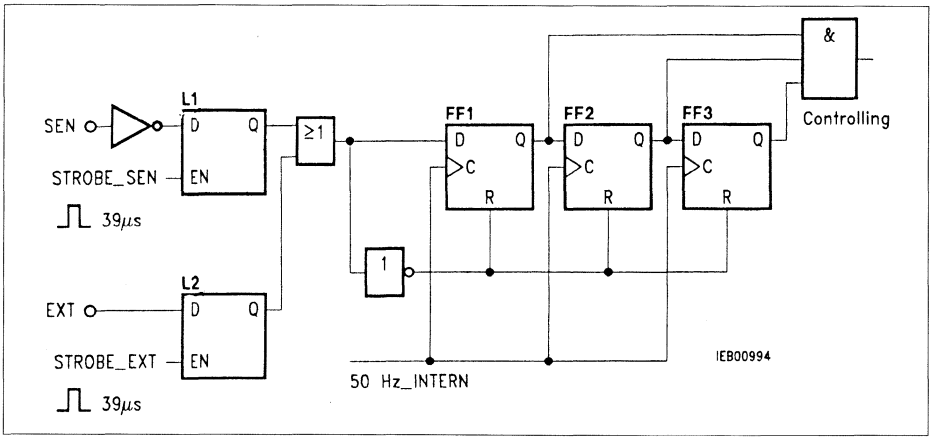


Figure 9
Circuit Principle of the Evaluation Logic for the Sensor and Extension Inputs

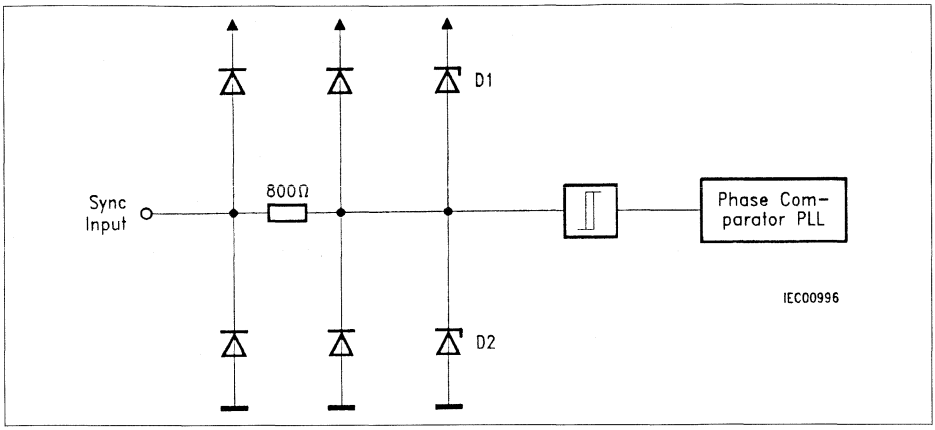


Figure 10
Circuit Principle at the Sync Input

Functional Description

Diodes D1 and D2 exhibit a behaviour similar to that of a Z-diode and become conductive at approx. 3.0 V.

Despite of the line voltage at the triac, it is ensured in combination with R_2 **(figure 4)** that the voltages occuring at the sync input of the SLB 0587 do not exceed essentially the range of the supply voltage.

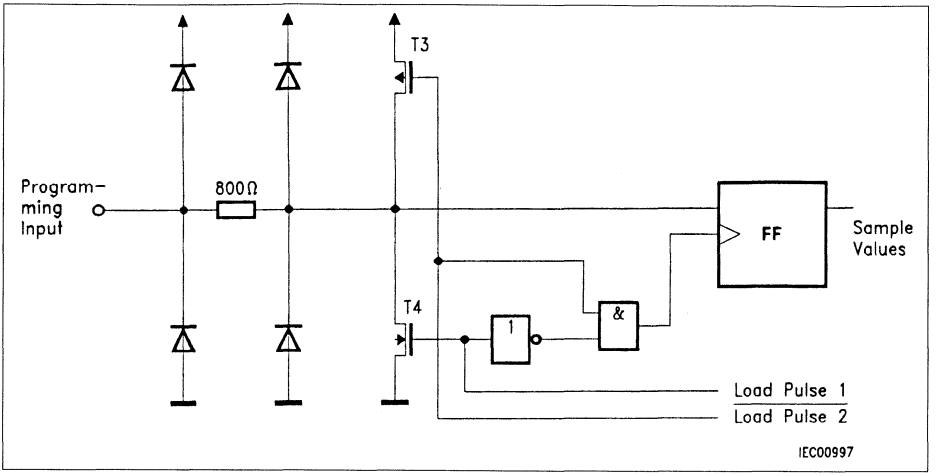


Figure 11
Circuit Principle on Programming Input (Pin 2)

Functional Description of the Programming Input (Pin 2):

The SLB 0587 distinguishes between 3 operating modes if pin 2 is wired accordingly.

The transistors T3 and T4 alternate in being conductive as shown in **figure 11**.
Acceptance of the logic level (which is dependent on the external wiring of the input) at the programming input, is performed during the second edge of the load pulse.

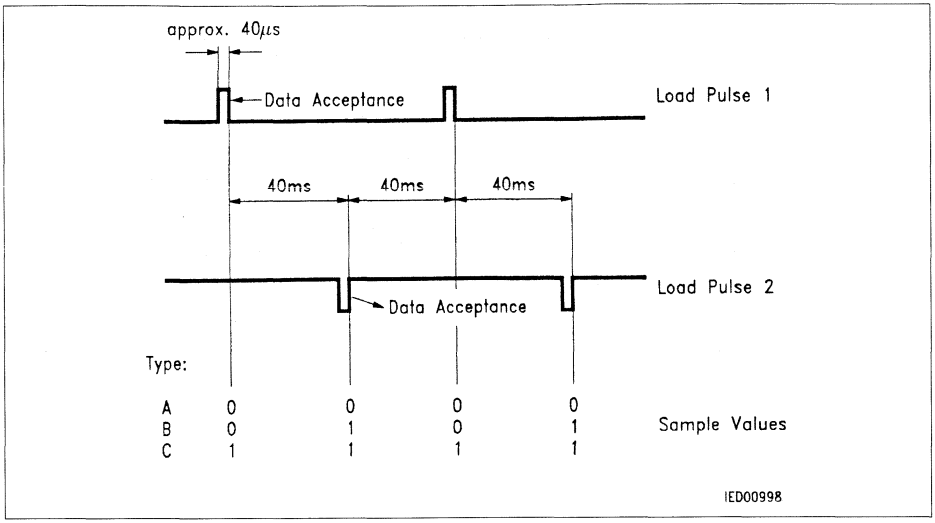


Figure 12
Internal Timing for Distinguishing between the Operating Modes A, B and C

Absolute Maximum Ratings

V_{DD} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{SS}	– 7.5	0.3	V
Input voltage	V_I	V_S – 0.3	0.3	V
Input current: Sync input Extension input	 I_I I_I	 – 0.5 – 1	 0.5 1	 mA mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	– 55	125	°C
Total power dissipation (T_A = 25 °C)	–	–	10	mW
Thermal resistance System-air (P-DIP-8) System-air (P-DSO-8-1)	 $R_{th\,SA}$ $R_{th\,SA}$	 – –	 135 231	 K/W K/W

Operating Range

Supply voltage	V_{SS}	– 5.6	– 4.5	V
Line frequency	f	47.5	63	Hz
Ambient temperature	T_A	0	100	°C

Characteristics

T_A = 25 °C; V_{SS} = –5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current, pin 1	I_{DD}	–	0.5	0.65	mA	Dimmer OFF: f_{sync} = 50 Hz R_L = 120 Ω*)

*) Load resistance between pin 1 and pin 8

Characteristics (cont'd)
T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Sensor Input (pin 5)						
H-input voltage	V_{IH}	1/2 V_{SS} + 1.1	–	–	V	–
L-input voltage	V_{IL}	–	–	1/2 V_{SS} – 1.1	V	–
Input current (extension)	I_{IH}	–	23	–	µA	220 V at sensor (extension)
Input current	I_{IH} I_{IL}	– 1 0	–	0 1	µA µA	V_I = 0 V V_I = V_{SS}
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}	–	line sine wave	–	–	–
Frequency with active signal	f	–	–	–	Hz	Line frequency
Extension (pin 6)						
H-input voltage	V_{IH}	V_{SS} + 3.0	–	–	V	–
L-input voltage	V_{IL}	–	–	V_{SS} + 0.8	V	–
Input current	I_{IL}	0	–	1	µA	V_I = V_{SS}
Sync Input (pin 4)						
H-input voltage	V_{IH}	1/2 V_{SS} + 1.8	–	–	V	–
L-input voltage	V_{IL}	–	–	1/2 V_{SS} + 1.8	V	–
Input current	I_{IH}	–	207	–	µA	**Application Circuit**
HL transition time (trigger transition) LH transition time	t_{THL} t_{TLH}	–	supply sine wave	–	–	–
Frequency	f	–	50/60	–	Hz	Line frequency

Characteristics (cont'd)

T_A = 25 °C; V_{SS} = – 5 V (V_{DD} = 0 V)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Programming Input (pin 2)						
Load capacitance	C_L	0	–	500	pF	–
Load resistance Mode B Mode A; C	 R_L R_L	 200 0	 – –	 ∞ 1	 kΩ kΩ	–
Integrator (pin 3)						
Application circuit	C_5 R_{10}	68 22	100 330	330 680	nF kΩ	see **figure 4**
Output (pin 8)						
L-output current	I_{OL}	25	–	65	mA	V_{QL} = – 3 V R_L = 120 Ω
L-pulse width	t_{QL}	–	117.2 97.7	–	µs µs	50 Hz supply 60 Hz supply
HL transition time	t_{HLQ}	–	–	200	ns	–
LH transition time	t_{HLQ}	–	–	1	µs	R_L = 120 Ω C_L = 1 nF

Selector Guide

Type	Package	Resolution Bit	Conversion time[3]	Strobe frequency max MHz	Supply voltage V	Analog Multiplex	TUE[4] LSB max.	Page
Ultra-Fast ADC								
SDA 5200 N; S	C-DIP-16	6	10 ns	100	+ 5, – 5.2		± 1/2[5]	341
Microprocessor-Compatible ADC								
SDA 0808 B	P-DIP-28	8	13 µs	1.5[1]	5	8 ×	± 1/2	348
SDA 0808 N	PL-CC-28	8	13 µs	1.5[1]	5	8 ×	± 1/2	348
SDA 0810 B	P-DIP-28	10	15 µs	1.5[1]	5	8 ×	± 1/2	379
SDA 0810 N	PL-CC-28	10	15 µs	1[1]	5	8 ×	± 1/2	379
SDA 0812 A	P-DIP-28	12	8.5 µs	2[1]	5	4 ×	± 1/2	413
SDA 0812 AN	PL-CC-28	12	8.5 µs	2[1]	5	4 ×	± 1/2	413
SDA 1808 A	P-DIP-28	8	7.5 µs	2[1]/125 kHz[2]	5	8 ×	± 1/2	362
SDA 1808 N	P-LCC-28	8	15 µs	2.5[1]	5	8 ×	± 1	348
SDA 1808 AN	P-LCC-28	8	7.5 µs	2[1]/125 kHz[2]	5	8 ×	± 1/2	362
SDA 1810 A	P-DIP-28	10	8.5 µs	2[1]/110 kHz[2]	5	8 ×	± 1/2	395
SDA 1810 AN	P-LCC-28	10	8.5 µs	2[1]/110 kHz[2]	5	8 ×	± 1/2	395
SDA 1810 N	PL-CC-28	10	15 µs	2[1]	5	8 ×	± 1	379
SDA 1810 D	P-DIP-28	10	15 µs	2[1]/66 kHz[2]	5	8 ×	± 1.25	379
SDA 1810 DN	P-LCC-28	10	15 µs	2[1]/66 kHz[2]	5	8 ×	± 1.25	379
SDA 1812 D	P-DIP-28	12	8.5 µs	2[1]/110 kHz[2]	5	4 ×	± 0.75	413
SDA 1812 DN	P-LCC-28	12	8.5 µs	2[1]/110 kHz[2]	5	4 ×	± 0.75	413
SDA 2812 A	P-DIP-16	12	9.5 µs	2[1]/100 kHz[2]	5	4 ×	± 1.5	444
SDA 2812 AG	P-DSO16	12	9.5 µs	2[1]/100 kHz[2]	5	4 ×	± 1.5	444
SDA 3812 A	P-DIP-28	12	9.5 µs	2[1]/100 kHz[2]	5	4 ×	± 1.5	444
SDA 3812 AN	P-LCC-28	12	9.5 µs	2[1]/100 kHz[2]	5	4 ×	± 1.5	444

[1] Clock frequency
[2] Sampling rate
[3] Including sample time
[4] Total Unadjusted Error
[5] Linearity Error

SMD = (Surface Mounted Device)

6-Bit A/D Converter, 100 MHz

SDA 5200

Bipolar IC

Features

- Strobe frequency 100 MHz
- 6-bit resolution (1.6 %)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs (SDA 5200 N), thus simple cascading for 7-bit or 8-bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to Nyquist limit
- ± ½ LSB max. linearity error
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage + 5 V; – 5.2 V

C-DIP-16

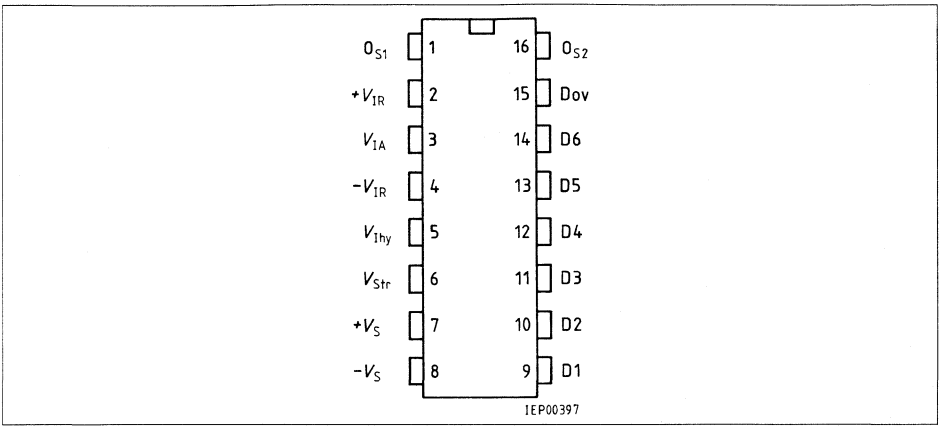
	Type	Ordering Code	Package
■ S	SDA 5200 N	Q67000-A2242	C-DIP-16
■ S	SDA 5200 S	Q67000-A4243	C-DIP-16

■ Not for new design

The SDA 5200 is an ultrafast A/D converter with 6-bit resolution and overflow output. After cascading, it enables straightforward implementing of 7 or 8 bit A/D converters, respectively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and excellent linearity, the SDA 5200 is outstanding for a broad analog bandwidth which – from the analog side – permits application up to the limit of the Nyquist theorem.

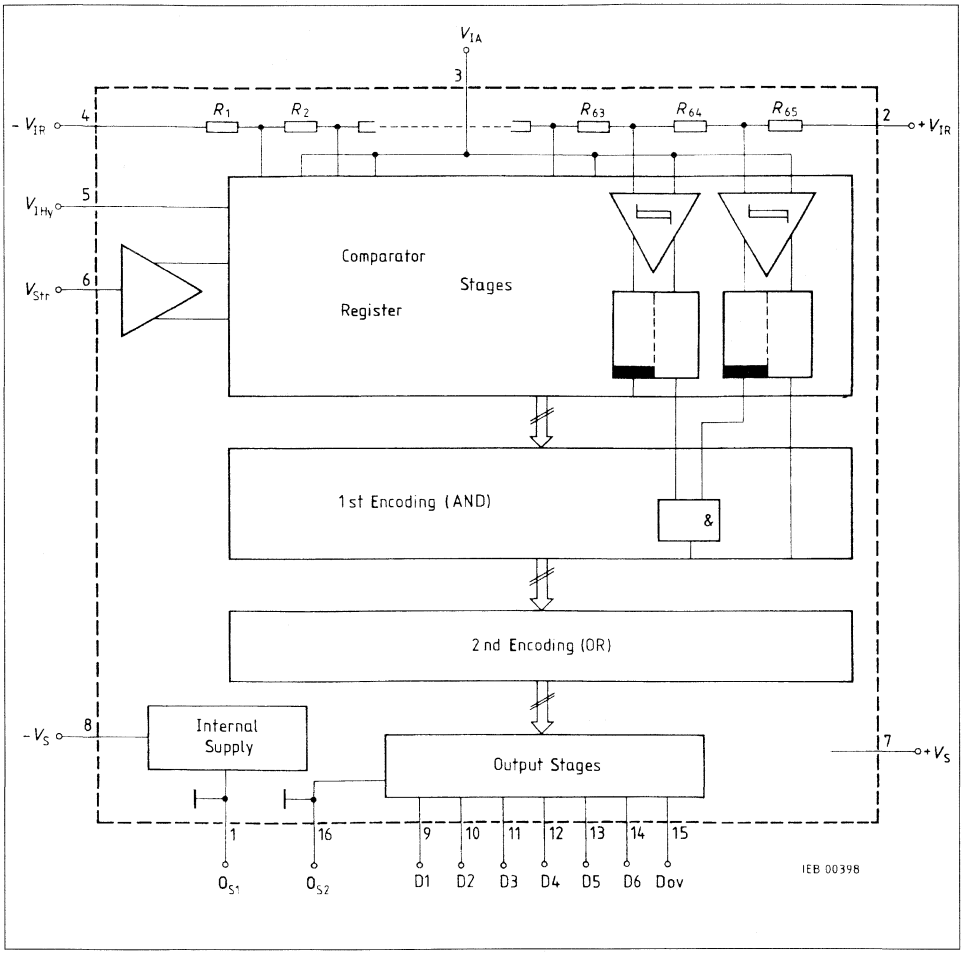
The SDA 5200 is pin-compatible with the SDA 6020.



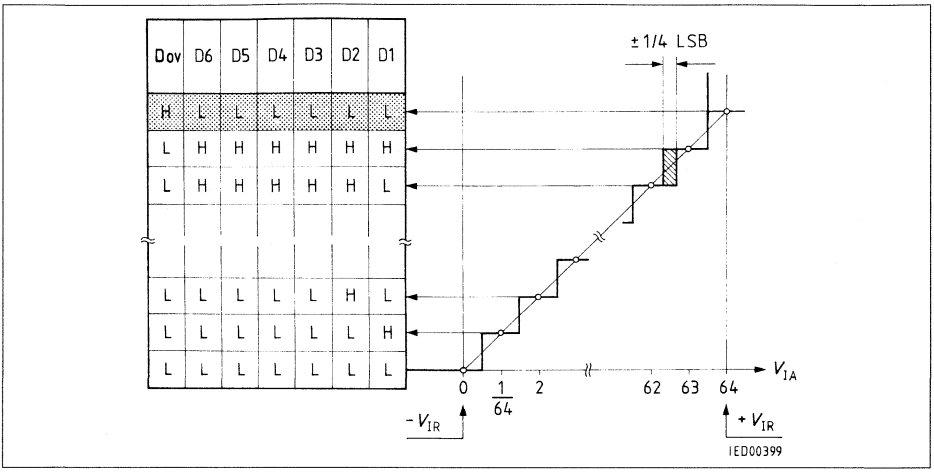
Pin Configuration
(top view)

Pin Definitions and Functions

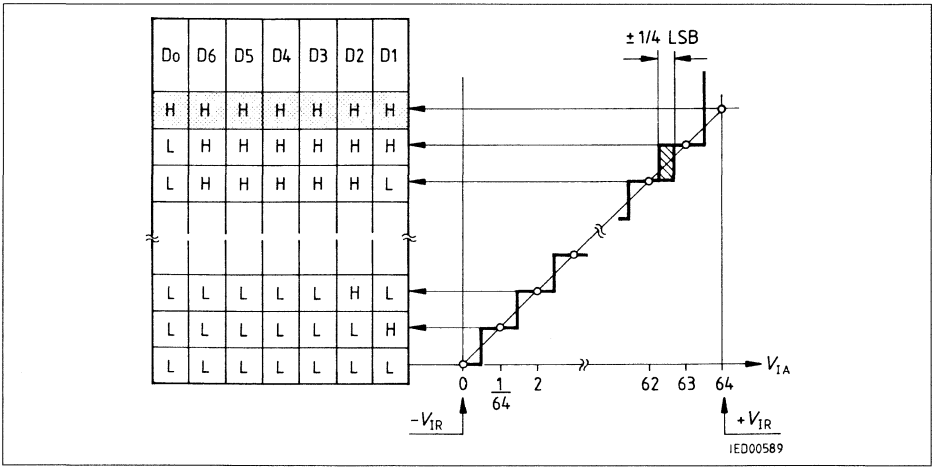
Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (+ 2 V)
3	V_{IA}	Analog signal input (max. + 2 V; – 3 V)
4	$-V_{IR}$	Negative reference voltage (– 3 V)
5	V_{Ihy}	Hysteresis control (0 V to + 2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+ 5 V)
8	$-V_S$	Negative supply voltage (– 5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Dov	Overflow output
16	0_{S2}	Digital ground 2



Block Diagram



Transfer Characteristic and Truth Table (SDA 5200 N)



Transfer Characteristic and Truth Table (SDA 5200 S)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$+ V_S$	– 0.3	6.0	V
Supply voltage	$- V_S$	– 6.0	0.3	V
Input voltages	$V_{IA} + V_{IR} - V_{IR}$	– 3.5	2.5	V
Strobe	V_{strobe}	$- V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	– 0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	– 55	125	°C
Thermal resistance				
system – air	$R_{th\,SA}$		70	K/W
junction	$R_{th\,J}$		16	K/W

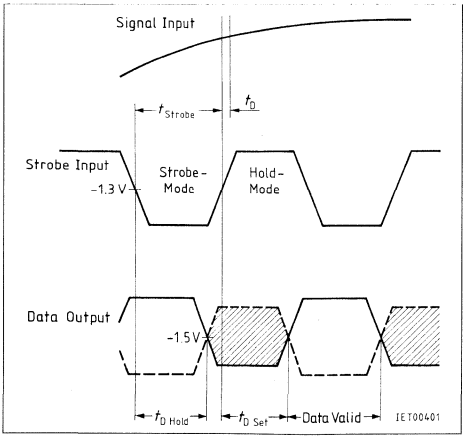
7

Characteristics

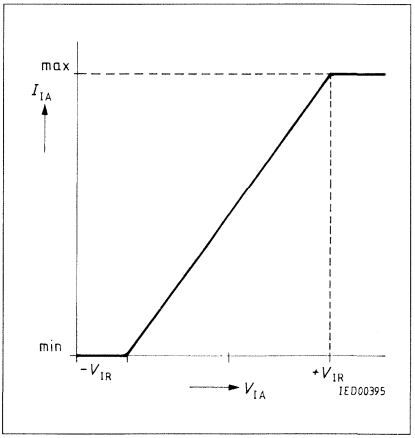
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Power Supply					
Positive supply voltage	$+ V_S$	4.5	5.0	5.5	V
Negative supply voltage	$- V_S$	– 5.7	– 5.2	– 4.7	V
Current consumption					
at $+ V_S = + 5.0$ V; $V_{IA} \leq - V_{IR}$	I_{S+}		50	80	mA
at $- V_S = - 5.2$ V; $V_{IA} \leq - V_{IR}$	I_{S-}		55	80	mA
Analog Section					
Signal Input					
Maximum input voltage	$V_{IA\,max}$	$- V_{IR\,min}$		$+ V_{IR\,max}$	V
$V_{IA\,max} = \mid (+ V_{IR\,max}) - (- V_{IR\,min}) \mid$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = + V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < - V_{IR}$	I_{IA}	– 500		500	nA
Input capacitance					
at $V_{IA} < - V_{IR}$	C_{IA}		25		pF
Reference Input					
Pos. reference voltage	$+ V_{IR}$	– 2.5		2	V
Negative reference voltage	$- V_{IR}$	– 3.0		1.5	V
Reference resistance	R_{REF}	96	128	195	Ω

Characteristics (cont'd)

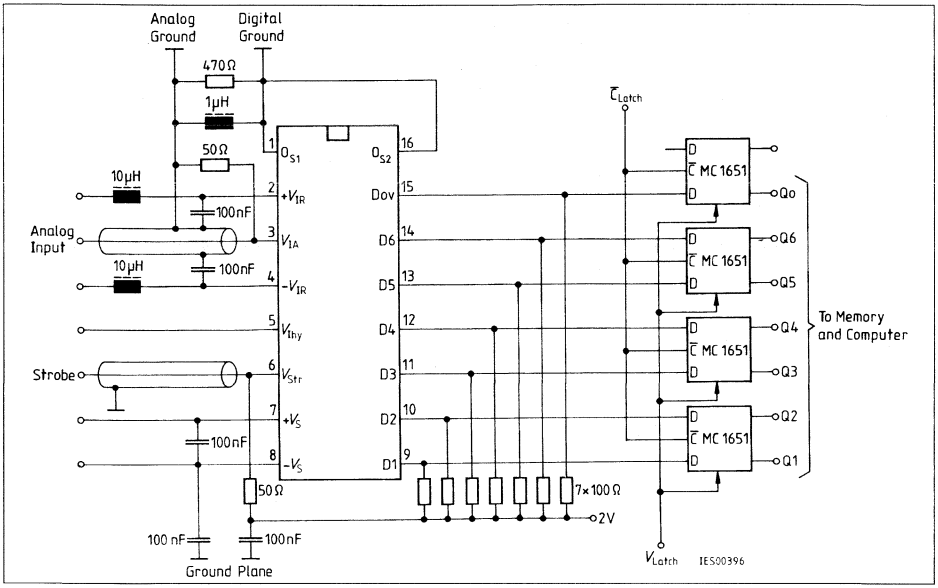
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Digital Section					
Strobe Input					
H-input voltage	V_{IH}	– 1.1	– 0.9	– 0.6	V
L-input voltage	V_{IL}	– 2.0	– 1.7	– 1.6	V
H-input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA
Data Outputs 100 Ω to – 2 V					
H-output voltage	V_{QH}	– 1.1	– 0.9	– 0.7	V
L-output voltage	V_{QL}	– 2.0	– 1.7	– 1.5	V
Dynamic Parameters					
Aperture time	t_D		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time SDA 5200 N; S	$t_{D\,Hold}$		12	17	ns
Signal transition time SDA 5200 N; S	$t_{D\,Set}$		12	17	ns
Max. strobe frequency SDA 5200 N; S	f_{strobe}	100			MHz
Max. slew rate	SR		0.5		V/ns
Bandwidth (– 3 dB)	B		140		MHz



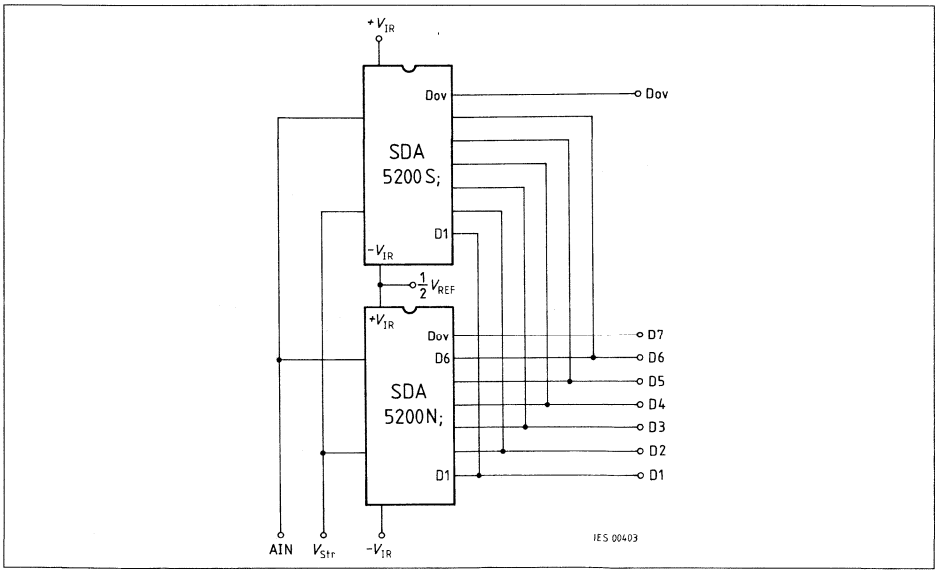
Pulse Diagram of Strobe Input and Data Outputs



Input Current versus Input Voltage



Test Circuit



Application Circuit
7-bit A/D converter with SDA 5200 S, N

SIEMENS

Microprocessor-Compatible 8-Bit A/D Converters with 8-Channel Multiplexer

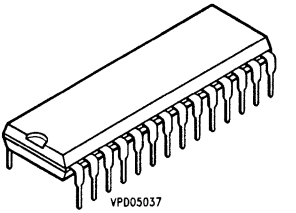
SDA 0808
SDA 1808

Preliminary Data

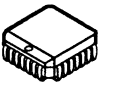
ACMOS IC

Features

- **A**dvanced **CMOS** (ACMOS) technology
- 8-bit resolution
- Total unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (13 µs) (SDA 0808)
- Fast conversion time (15 µs) (SDA 1808)
- Single 5 V DC supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustment required
- Latched tristate outputs
- TTL-compatible output voltage
- Low power consumption (15 mW)



P-DIP-28



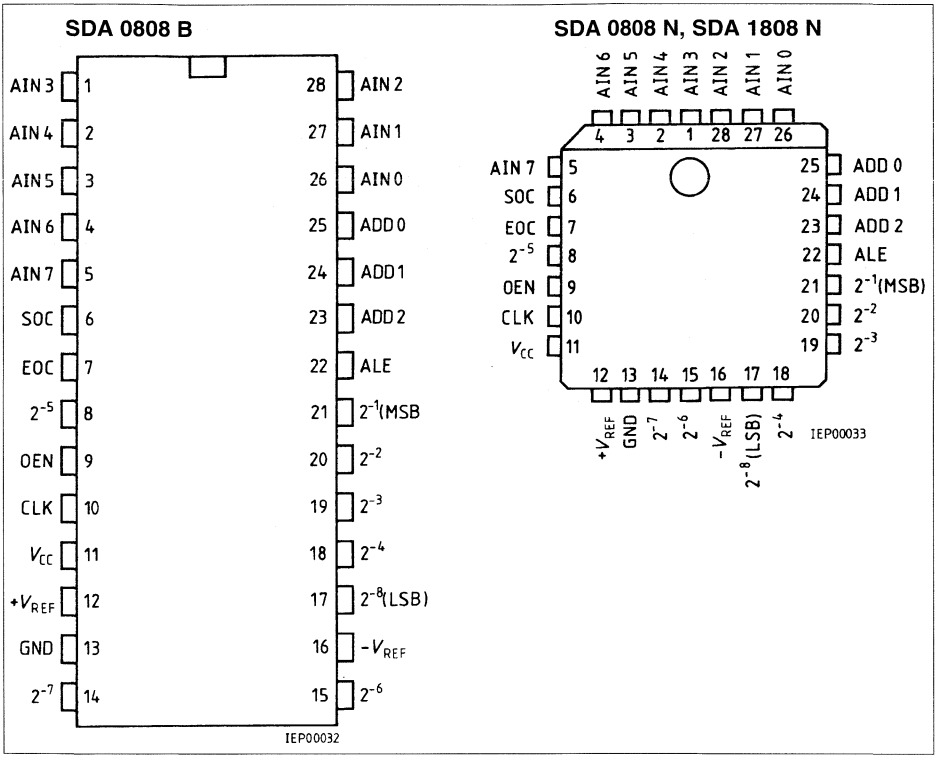
P-LCC-28-2

Type	Ordering Code	Package
S SDA 0808 B	Q67100-A8129	P-DIP-28
SDA 0808 N	Q67100-A8206	P-LCC-28-2 (SMD)
SDA 1808 N	Q67100-A8254	P-LCC-28-2 (SMD)

SDA 0808 and SDA 1808 are monolithic 8-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V DC supply. The IC contains a microprocessor-compatible control logic and an 8-bit data bus. They are pin-compatible with the data-acquisition component ADC 0808/0809.

SDA 0808 and SDA 1808 use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

The temperature range of the SDA 0808 N, SDA 1808 N is – 40 °C to 85 °C and that of the SDA 0808 B – 40 °C to 125 °C. The SDA 0808 operates at a clock frequency of 1.5 MHz, the SDA 1808 at 2.5 MHz max.



Pin Configuration
(top view)

7

Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^{-5}	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11 12	V_{CC} + V_{REF}	Positive supply voltage Positive reference voltage
13	GND	Ground
14, 15	2^{-7}, 2^{-6}	Digital output signals
16	– V_{REF}	Negative reference voltage
17 to 21	2^{-8} (LSB) to 2^{-1} (MSB)	} Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 50 pF) as a sample and hold circuit, a successive-approximation register and a comparator.

The A/D converter's successive-approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output (end of conversion) passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is automatically set to zero, has a high resolution and a low drift. Thus the A/D converter is extremely insensitive to temperature errors.

A/D Converter Timing

The values stated apply to the SDA 0808, those in parentheses to the SDA 1808.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 10 (20) external clock cycles which will be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 10 (20) clock cycles.

Conversion of the sampled analog voltage takes place between the 11th (22nd) and 19th (38th) clock cycle after sampling has been completed. In the 19th (38th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 20th (40th) clock cycle.

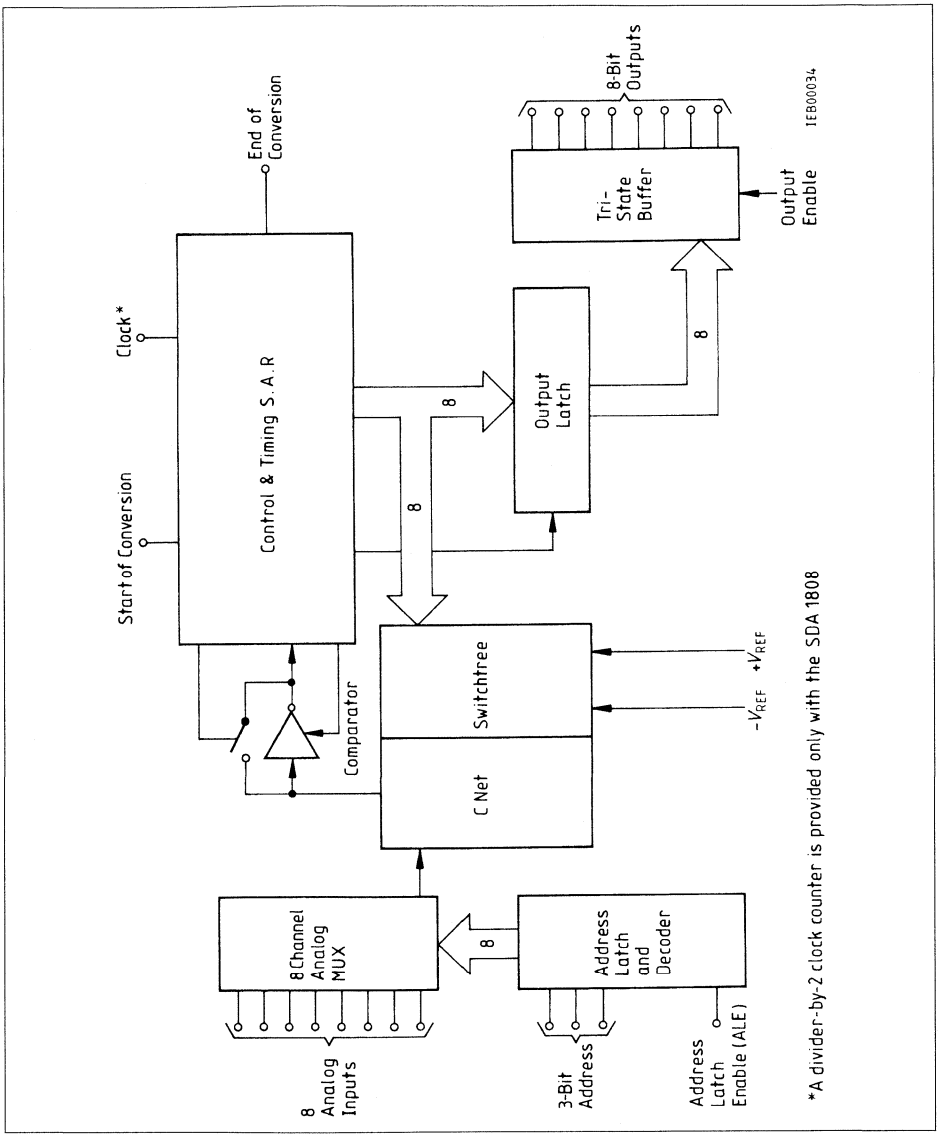
Multiplexer

The converters provide eight multiplexed analog input channels. The input channels are selected by three address lines (AD2, AD1, AD0).

Table 1 shows the input states for the address lines that select a channel. The address is latched on the rising slope of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7



Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage [1]	V_{CC}		6.5	V
Input voltage range, any input	V_I	− 0.3	V_{CC} + 0.3	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	− 65	125	°C
Thermal resistance system – ambient P-DIP-28	$R_{th\,SA}$		50	K/W
P-LCC-28	$R_{th\,SA}$		70	K/W

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage [2]	+ V_{REF}		V_{CC}	V_{CC}+0.1	V
Negative reference voltage	− V_{REF}	− 0.1	0		V
Differential reference voltage [10]	ΔV_{REF} = + V_{REF} − (− V_{REF})		5		V
Analog input range	V_{AIN}	− V_{REF}		+ V_{REF}	V
Slew rate [11] at f_{CLK} = 1 MHz/2 MHz	*SR*			60	mV/µs
Start pulse duration	$t_{W\,(S)}$	200			ns
Address load control pulse width	$t_{W\,(ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0808	f_{CLK}	10	640	1500	kHz
SDA 1808	f_{CLK}	20	1280	2500	kHz
Ambient temperature SDA 0808 N; SDA 1808 N	T_A	− 40		85	°C
SDA 0808 B	T_A	− 40		125	°C

For note refer to 3 pages hereafter.

Characteristics

V_{CC} = 4.75 to 5.25 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} –1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} –0.4			V	I_Q = – 360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state output current (high impedance-state)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			– 3	µA	V_Q = 0
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			– 1	µA	V_I = 0
Supply current	I_{CC}		0.3	3	mA	f_{CLK} = f_{CLK} (typ.)
Input capacitance, control input	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance between pins 12 and 16	R	1		1000	kΩ	T_A = 25 °C

Analog Multiplexer

V_{CC} = 5 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel ON-state current[3]	I_{ON}			2	µA	V_I = 5 V, f_{CLK} = f_{CLK} (typ.)
				– 2	µA	V_I = 0 V, f_{CLK} = f_{CLK} (typ.)
Channel OFF-state current[3]	I_{OFF}		10	200	nA	V_{CC} = 5 V T_A = 25 °C, V_I = 5 V
			– 10	–200	nA	V_{CC} = 5 V T_A = 25 °C, V_I = 0 V
				1	µA	V_{CC} = 5 V, V_I = 5 V
				– 1	µA	V_{CC} = 5 V, V_I = 0 V

For note refer to 2 pages hereafter.

Characteristics

T_A = 25 °C, V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V, f_{CLK} = f_{CLK} (typ), unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage sensitivity	k_{SVS}		± 0.05		%/V	V_{CC} = V_{REF} + = 4.75 V to 5.25 V, T_A = – 40 °C to 85 °C [4]
Linearity error [5]				± 0.5	LSB	
Zero error [6]				± 0.5	LSB	
Total unadjusted error [7]			± 0.25		LSB	T_A = 25 °C
SDA 0808 N				± 0.5	LSB	T_A = – 40 °C to 85 °C
SDA 0808 B				± 0.5	LSB	T_A = – 40 °C to 125 °C
SDA 1808 N			± 0.5	± 1	LSB	T_A = – 40 °C to 85 °C, f_{CLK} = 2.5 MHz
Output enable time **(figure 1)**	t_{en}		80	150	ns	C_L = 50 pF, R_L = 10 kΩ
Output disable time **(figure 1)**	t_{dis}		40	95	ns	C_L = 10 pF, R_L = 10 kΩ
Output turn-OFF time **(figure 1)**	t_{OFF}		20	60	ns	C_L = 10 pF, R_L = 10 kΩ
Conversion time [12]	t_{Conv}	13	31	2000	µs	f_{CLK} =1.5 MHz/640 kHz/ 10 kHz [8]
SDA 1808 N	t_{Conv}	15	31	2000	µs	f_{CLK} = 2.5 MHz/1280 kHz/ 20 kHz [8]
Delay time, EOC output	$t_{D\,(EOC)}$	0		200	ns	[9]

For notes refer to next page.

7

Notes

1) All voltage values refer to the network's ground terminal.

2) Care must be taken that this rating is observed, even during power-up.

3) The channel on-state current is primarily generated by the current of the Schmitt trigger and varies directly with the clock frequency.

4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and + V_{REF} are changing together and the change in accuracy is measured with respect to full-scale deflection.

5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.

6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

7) The total unadjusted error is the total-of-linearity error, zero and full-scale error.

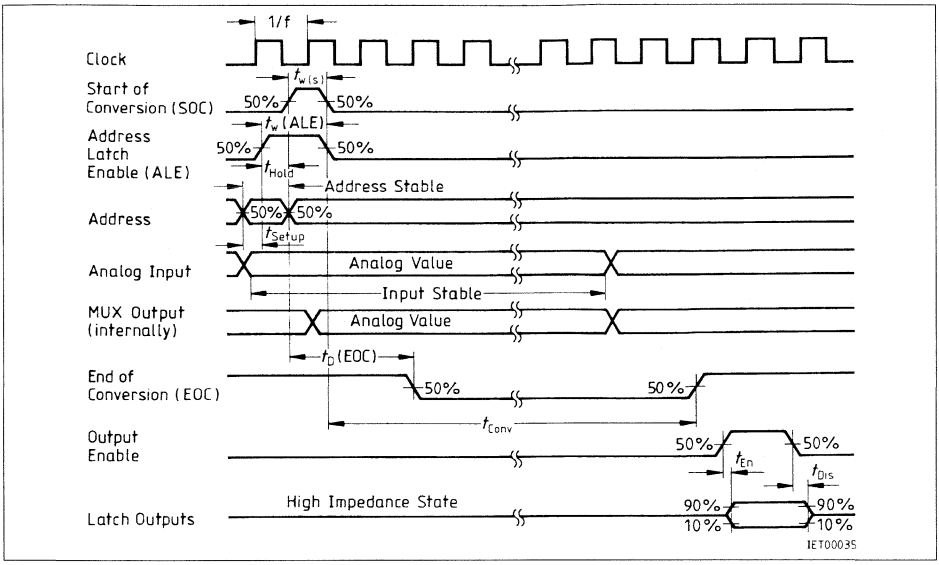
8) SDA 0808: $t_{Conv\ max} = 20 \times 1/f_{CLK}$ $t_{Conv\ min} = 19 \times 1/f_{CLK}$;
SDA 1808: $t_{Conv\ max} = 40 \times 1/f_{CLK}$ $t_{Conv\ min} = 38 \times 1/f_{CLK}$;

9) Refer to the operating pulse diagram.

10) For typical error versus reference voltage span refer to the respective diagram.

11) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full-scale errors. Filtering by a low pass (R = 500 Ω, C = 100 nF) or use of an external sample-and-hold is then required.

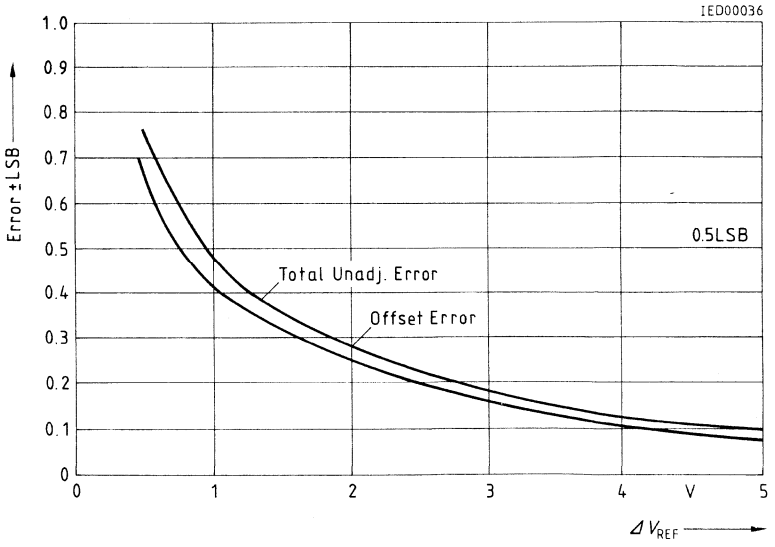
12) Including sample time.



Operating Pulse Diagram

Typical Error versus Reference Voltage Span

V_{CC} = 5.0 V; $f_{CLK} = f_{CLK}$ typ.; $\Delta V_{REF} = +V_{REF} - (-V_{REF})$



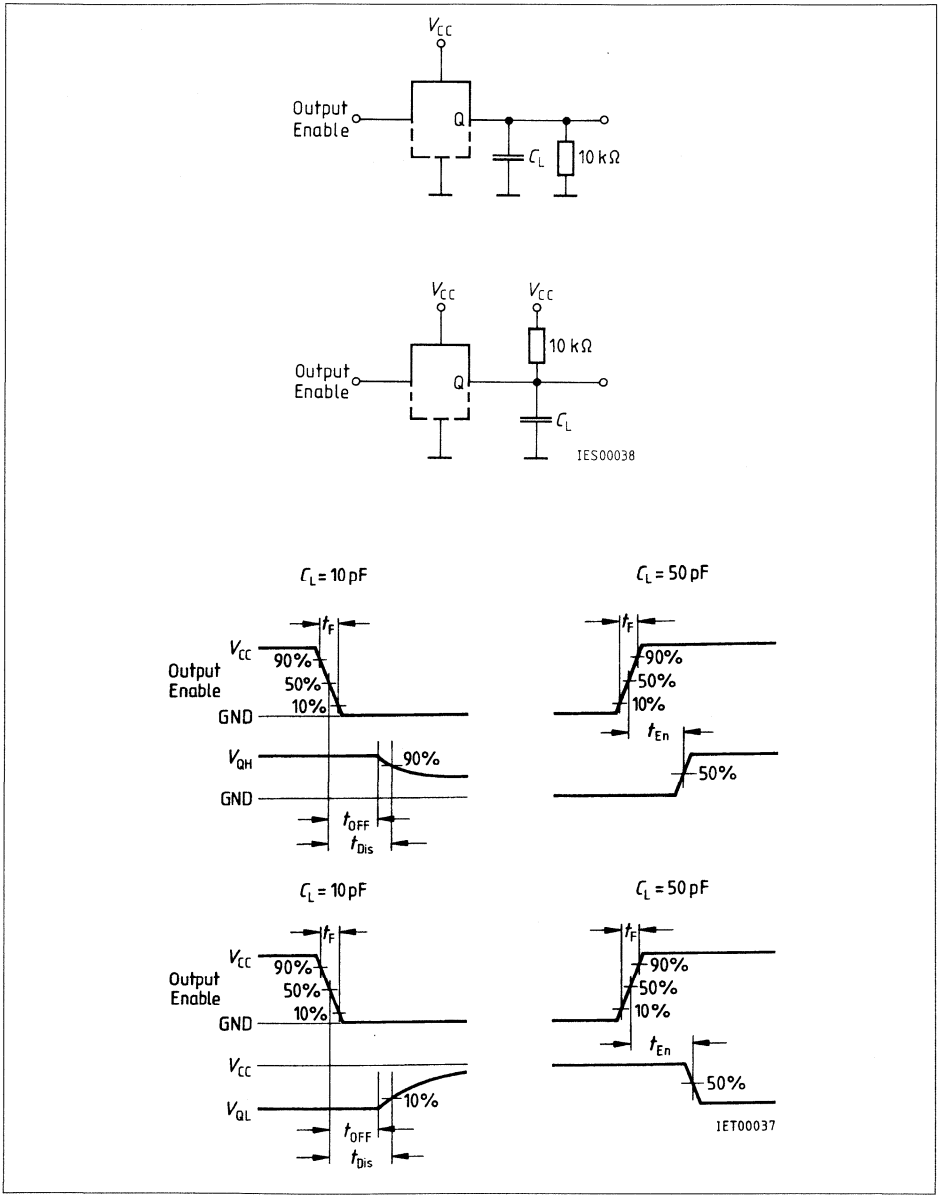


Figure 1
Tristate Measurement Circuits and Pulse Diagrams

Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates.

INTEL Microprocessors

A typical interface is shown in **figure 2**.

Start of Conversion

A write instruction selects one of the analog input channels and starts the conversion.

Write address: $\overline{\text{ADC\_CS}}$

The end of conversion signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the Conversion Result

With a read instruction the conversion result is read from the $\overline{\text{ADC\_CS}}$ address.

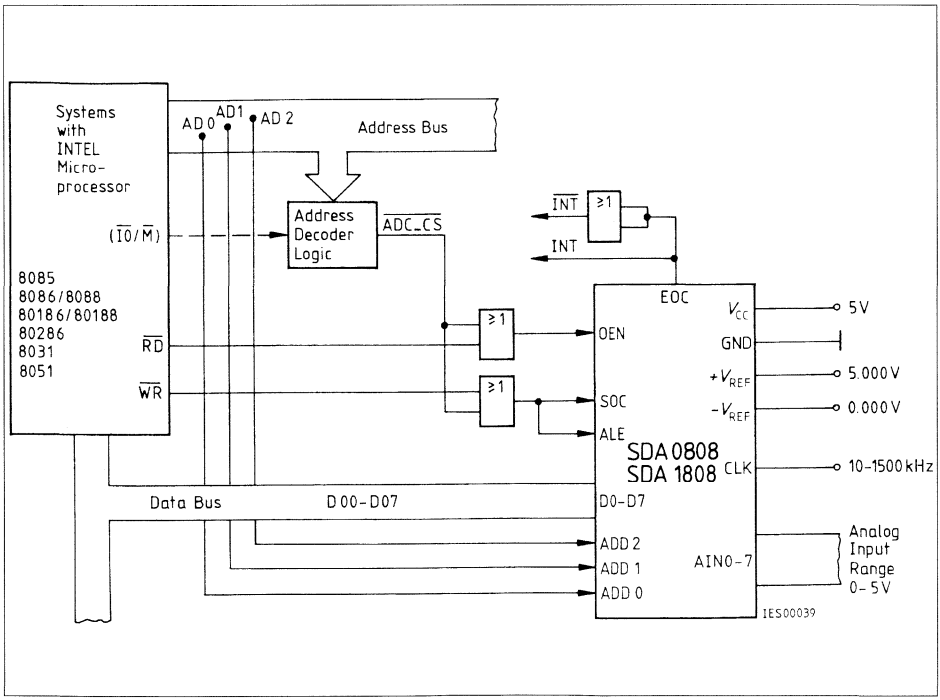


Figure 2

Motorola Microprocessors

A typical interface is shown in **figure 3**.

Start of Conversion

A write instruction to an address that has been decoded by the address decoder logic will start a conversion. The lower 3 bits of the address bus select the input channel.

Reading of the Conversion Result

A read instruction from the ADC-address puts the conversion result to the data bus: MOVE.B ADC-ADDRESS, D0 places the conversion data in the D0 register of the microprocessor.

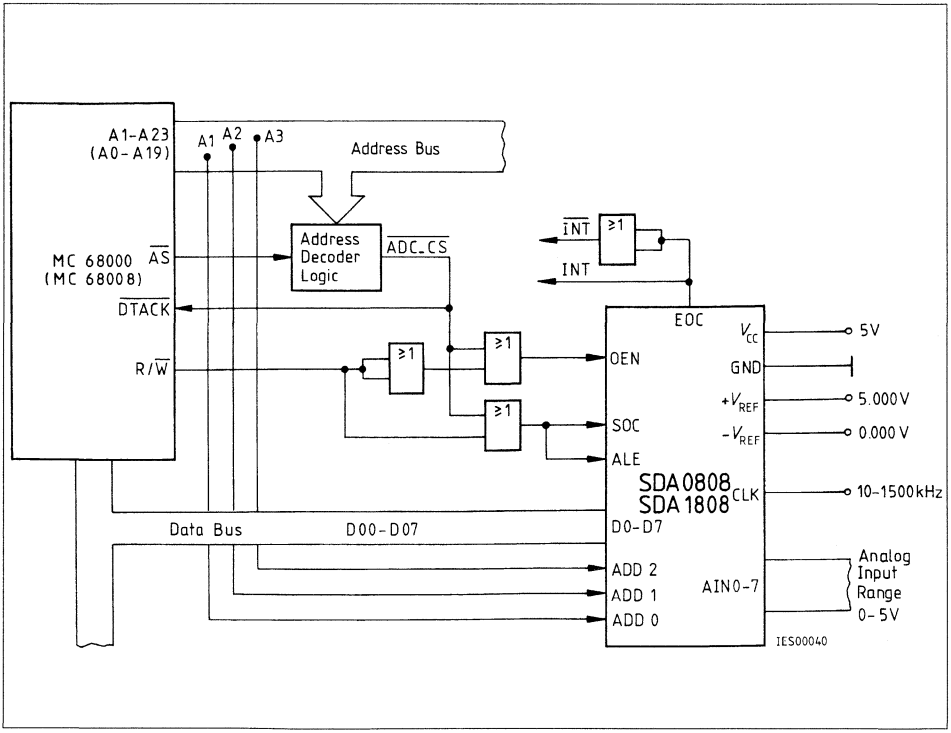


Figure 3

Application Hints

Power Supply Decoupling

The power supply should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 0.1 µF ceramic capacitor should be placed between pins – V_{REF} and GND.

Analog Input

The high input impedance of the analog channels AIN0 to AIN7 allows simple analog interfacing. Signal sources (– $V_{REF} \leq$ AIN $\leq$ + V_{REF}) can directly be connected to the analog input channels, that is, without additional buffering if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 10 (20 for SDA 1808) clock cycles.

7

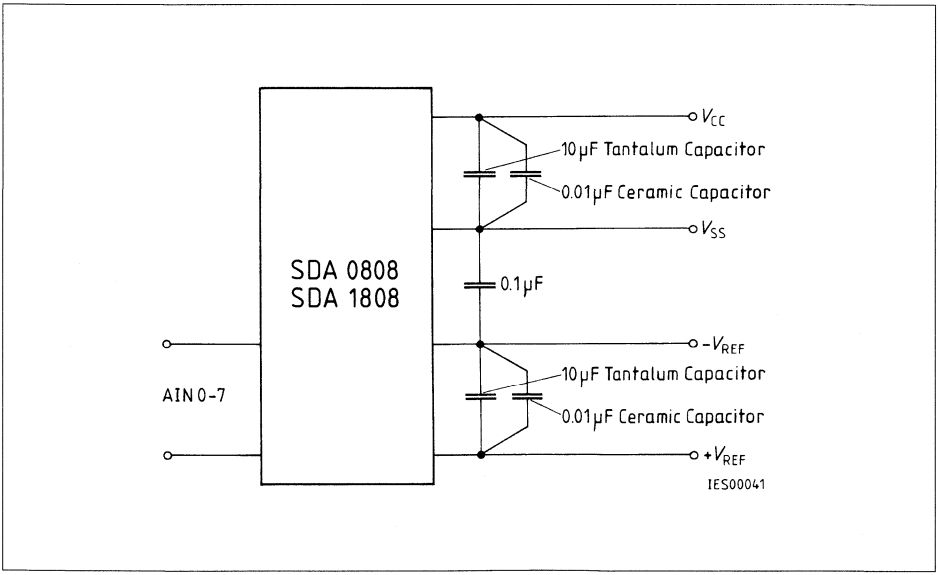


Figure 4
Capacitors

SIEMENS

Microprocessor-Compatible 8-Bit Sampling A/D Converter with 8-Channel Multiplexer

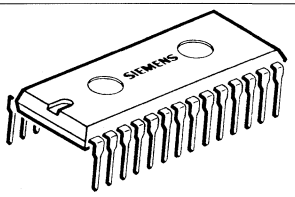
SDA 1808 A

Advance Information

CMOS IC

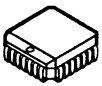
Features

- 8-bit resolution
- 125-kHz sampling rate
- Total unadjusted error ± 1/2 LSB
- Fast conversion time (5 µs)
- Sampling time 2.5 µs
- No missing codes
- Single 5 V DC supply
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustment required
- TTL-compatible output voltages
- Latched tristate outputs
- Low power consumption (10 mW during conversion, 50 µW idle)
- Offset calibration circuit



VPD 05037

P-DIP-28



VPL05039

P-LCC-28-2

	Type	Ordering Code	Package
▼	SDA 1808 A	Q67100-A8350	P-DIP-28
▼	SDA 1808 AN	Q67100-A8351	P-LCC-28-2 (SMD)

▼ = New type

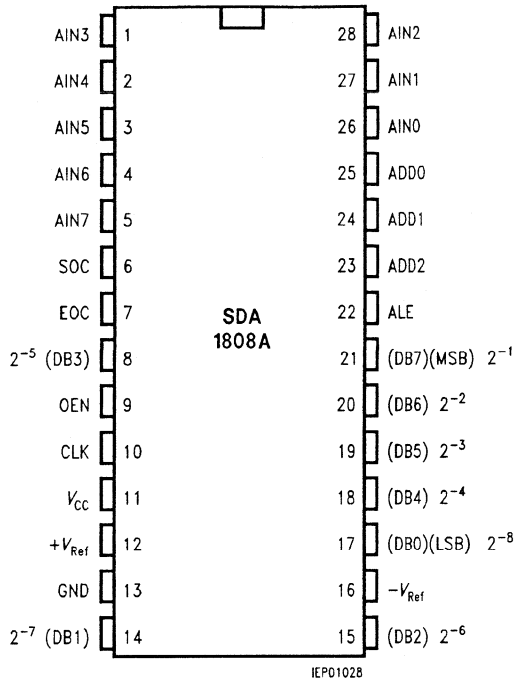
General Description

SDA 1808 A is a monolithic CMOS 8-bit A/D converter with a single supply voltage of 5V DC. It contains a microprocessor-compatible control logic and an 8-bit data bus. It is pin-compatible with the industry standards 0808 and 0809. The 8-bit data stream is supplied in a parallel format for interfacing with 8-bit microprocessors. The SDA 1808 A operates at a clock frequency of 2 MHz and offers enhanced dynamic performance for sampling rates up to 125 kHz.

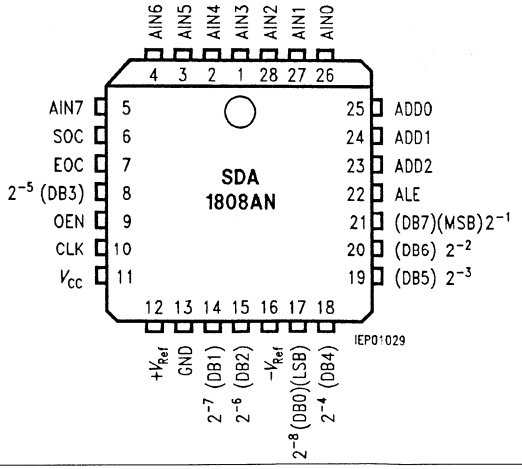
The converter uses the method of successive approximation by means of a capacitor network. The converter features a temperature-stabilized differential comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converter does not need any external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

The temperature range of the SDA 1808 A is -40 °C to 85 °C.

SDA 1808 A



SDA 1808 AN



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog Inputs, channel 3 to channel 7
6	SOC	Start of conversion, T/$\overline{H}$
7	EOC	End of conversion
8	DB3	Digital output signal
9	OEN	Output enable
10	CLK	External clock input
11	V_{CC}	Positive supply voltage
12	+ V_{REF}	Upper reference voltage
13	GND	Ground
14, 15	(DB1, DB2) 2^{-7}, 2^{-6}	Digital output signals
16	- V_{REF}	Lower reference voltage
17 to 21	(DB0 to DB7) 2^{-8} to 2^{-1}	Digital output signals
22	ALE	Address latch enable
23 to 25	ADD2 to ADD0	Address inputs
26 to 28	AIN0 to AIN2	Analog inputs

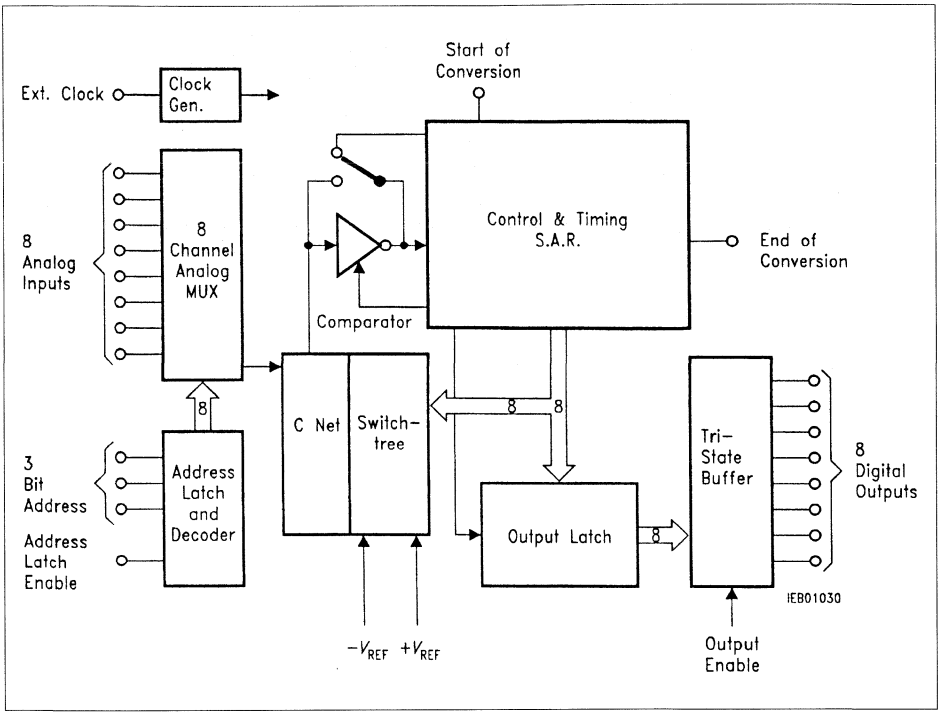


Figure 1
Block Diagram

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 30 pF) as a sample and hold circuit, a successive approximation register and a comparator.

The A/D converter's successive approximation register (SAR) is reset at the positive edge of the start of conversion (SOC) pulse. The conversion starts with sampling the analog signal. A conversion in process will be interrupted by a SOC pulse.

Following the rising edge of the SOC pulse, the end of conversion output (EOC) passes to low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator for high power supply rejection.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 5 external clock cycles and will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitor of approximately 30 pF within those 5 clock cycles.

Conversion of the sampled analog voltage takes place between the 6th and 16th clock cycle after sampling has been completed. In the 16th clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 16th clock cycle.

Multiplexer

The converter provides 8 multiplexed analog input channels. A particular input channel is selected by programming 3 address lines (ADD2, ADD1, ADD0). The table shows the input states for the address lines to select a channel. The address is latched on the rising edge of the ALE signal.

Address Lines			Select. Analog Channel
ADD2	ADD1	ADD0	AIN
L	L	L	AIN0
L	L	H	AIN1
L	H	L	AIN2
L	H	H	AIN3

Address Lines			Select. Analog Channel
ADD2	ADD1	ADD0	AIN
H	L	L	AIN4
H	L	H	AIN5
H	H	L	AIN6
H	H	H	AIN7

Reading the Conversion Results

The data is read as an 8-bit byte. The converter's digital outputs are positive true. The OEN signal enables the 8 bits parallel to the output buffers.

Autocalibration

An autocalibration circuit is included. It corrects offset errors only. Offset errors are adjusted in each conversion cycle, an initial offset calibration is done by power up.

Power-Up

An autocalibration cycle is started by power up. The autocalibration cycle takes 256 clock cycles. A start of conversion signal interrupts this autocalibration cycle and gives a normal conversion result (with increased offset errors) the autocalibration cycle will be finished after the conversion automatically.

Power Consumption

The current consumption is typical 2 mA during a conversion and during autocalibration (power-on). If no conversion (calibration) is running, the power consumption will be typically 10 µA.

T / $\overline{H}$ Mode

Normal conversion is started by a SOC high pulse. The min. start pulse duration is 100 ns. In this case the sample point is defined by the rising slope of CLK (**see figure 2a**).
If the SOC signal exceeds 5 CLK pulses the sample point will be defined by the falling slope of SOC (**see figure 2b**).

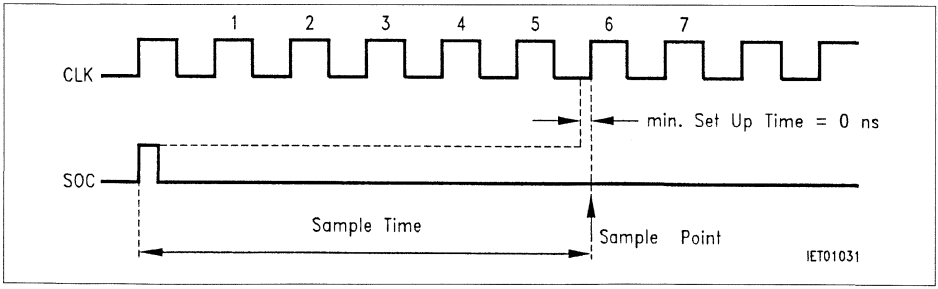


Figure 2 a)

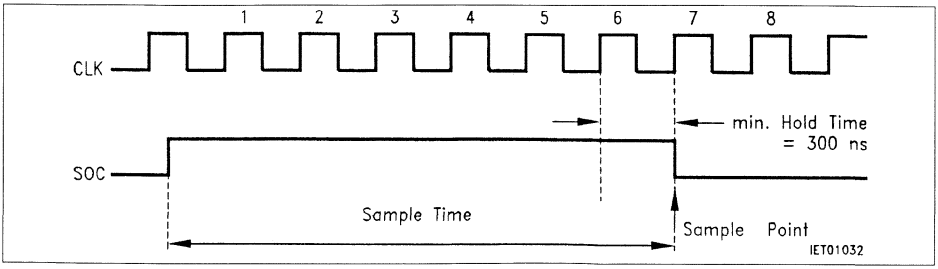


Figure 2 b)

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 3**.

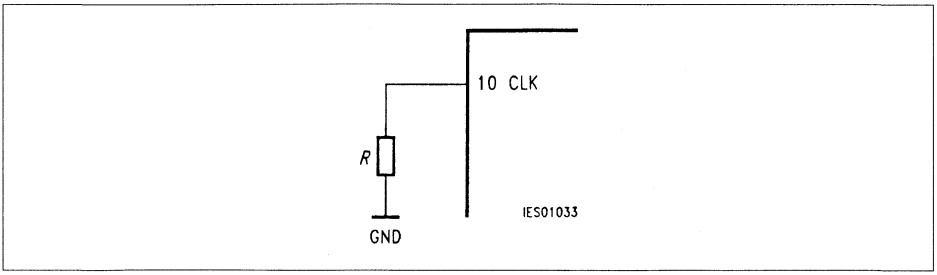


Figure 3
The Internal Clock Frequency only Depends on the *R* Value

The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.1 to 2.0 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device. Therefore, for precisely defined conversion times use of an external clock generator is recommended.

External Clock Operation

The required circuitry for external clock operation is shown in **figure 4**.

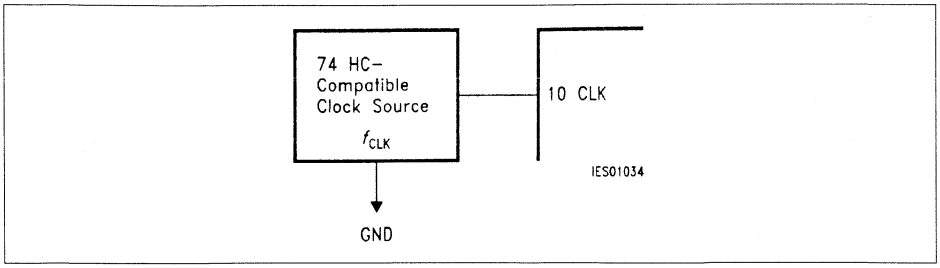


Figure 4
Circuitry for External Clock Operation

7

The external clock source has to provide 0.8 V max. for low voltage level and 3.5 V min. for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. T/$\overline{H}$ signal (see SOC). Synchronizing should be provided for optimum performance (see A/D converter timing). Note that the specification is referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.1 to 2.2 MHz.

Absolute Maximum Ratings

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Supply voltages [1]		V_{CC}		6.5	V
Input voltage range (all inputs)		V_I	– 0.3	V_{CC} + 0.3	V
Thermal resistance (system - air)	P-DIP-28	$R_{th\ SA}$		50	K/W
	P-LCC-28-2	$R_{th\ SA}$		70	K/W
Junction temperature		T_j		125	°C
Storage temperature		T_{stg}	– 65	125	°C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Operating Range					
Supply voltage	V_{CC}	4.5	5	6	V
Upper ref. voltage [2]	$+V_{REF}$		V_{CC}	$V_{CC+0.1}$	V
Lower ref. voltage	$-V_{REF}$	-0.1	0		V
Differential ref. voltage	ΔV_{REF}		5		V
Analog input range	V_{AIN}	$-V_{REF}$		$+V_{REF}$	V
Start pulse duration	$t_{w\ (S)}$	100			ns
Address load control pulse width	$t_{w\ (ALE)}$	100			ns
Address setup time	t_{Setup}	20			ns
Address hold time	t_{Hold}	20			ns
Clock frequency	f_{CLK}	100		2200	kHz
Ambient temperature	T_A	-40		85	°C

[1] All voltages are referred to ground.

[2] Care must be taken that this rating is observed even during power up.

Note: $\Delta V_{REF} = + V_{REF} - (- V_{REF})$

Characteristics

V_{CC} = 4.75 V to 5.25 V, unless otherwise specified, f_{CLK} = 2 MHz

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} - 1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} - 0.4			V	I_Q = - 360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state (high-impedance)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			-3	µA	V_Q = 0 V
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			-1	µA	V_I = 0 V
Supply current	I_{CC}		2.0 10	2.5 50	mA µA	during conversion idle
Input capac.,control inputs	C_I		10	15	pF	T_A = 25 °C
Output capacitance,data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance from pin12 to16	R	1	1000		kΩ	

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Characteristics

$V_{CC} = +V_{REF} = 5V$, $-V_{REF} = 0V$, $f_{CLK} = 2$ MHz, $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog Multiplexer V_{CC} = 5V						
Channel ON-state current [3]	I_{ON}			2	µA	V_I = 5 V
				- 2	µA	V_I = 0 V
Channel ON-state resistance	R_{ON}		1		kΩ	
OFF-state current (High impedance state)	I_{OFF}		10	200	nA	V_{CC} = 5 V, T_A = 25 °C, V_I = 5 V
			-10	- 200	nA	V_{CC} = 5 V, T_A = 25 °C, V_I = 0V
				1	µA	V_{CC} = 5 V, V_I = 5 V
				-1	µA	V_{CC} = 5 V, V_I = 0 V
Supply voltage sensitivity [4]	k_{SVS}		±0.05		% / V	$V_{CC} = +V_{REF}$ = 4.75 V to 5.25 V
Total unadjusted error [7]	*TUE*			0.5	LSB	
Zero error [6]	*OFS*		±0.25	0.5	LSB	
Integral nonlinearity [5]	*INL*			0.5	LSB	
Differential nonlinearity [5]	*DNL*		±0.25	0.5	LSB	
Gain error	*GE*		±0.125	0.5	LSB	
Sampling rate	f_S			125	kHz	f_{CLK} = 2 MHz
Effective number of bits	*ENOB*		7.8		bits	f_{AIN} = 50 kHz
Output enable time (**fig. 6**)	t_{en}		25	50	ns	C_L = 50 pF, R_L = 10 kΩ
Output disable time (**fig. 6**)	t_{dis}		40	95	ns	C_L = 10 pF, R_L = 10 kΩ
Output switch-OFF time (**fig. 6**)	t_{OFF}		10	20	ns	C_L = 10 pF, R_L = 10 kΩ
Sample time [8]	t_{sample}	2.5	6	60	µs	f_{CLK} = 2 MHz / 1 MHz / 100 kHz
Conversion time [8]	t_{conv}	5	10	100	µs	
Delay time, output EOC [9]	$t_{d\,EOC}$	0	20	50	ns	

[3] Channel on state current is primarily generated by the bias current into or out of the threshold detector and it varies directly with the clock frequency.

[4] The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies.

[5] The linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.

[6] The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

[7] Total unadjusted error is the max. sum of linearity error, zero error, integral and differential nonlinearity.

[8] $t_{conv\,max} = 10.1/f_{CLK}$, $t_{sample\,min} = 5.1/f_{CLK}$

[9] Refer to operating pulse diagram.

Characteristics

V_{CC} = $+V_{REF}$ = 5V, $-V_{REF}$ = 0V, f_{CLK} = 2 MHz, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Performance [10) 11)]						
Signal-to-noise ratio	*SNR*	47	48		dB	Full scale input sine-wave 1 kHz, *f* sampling is 100 kHz
		45	46		dB	Full scale input sine-wave 1 kHz, *f* sampling is 100 kHz
Total harmonic distortion	*THD*		70		dB	Full scale input sinewave 50 kHz, *f* sampling is 100 kHz
Full power bandwidth (-3 dB)	*BW*		4		MHz	
Aperture delay time			5		ns	SOC pin, T/$\overline{H}$ condition

10) *SNR* includes harmonic distortion.

11) Sample tested at 25 °C .

7

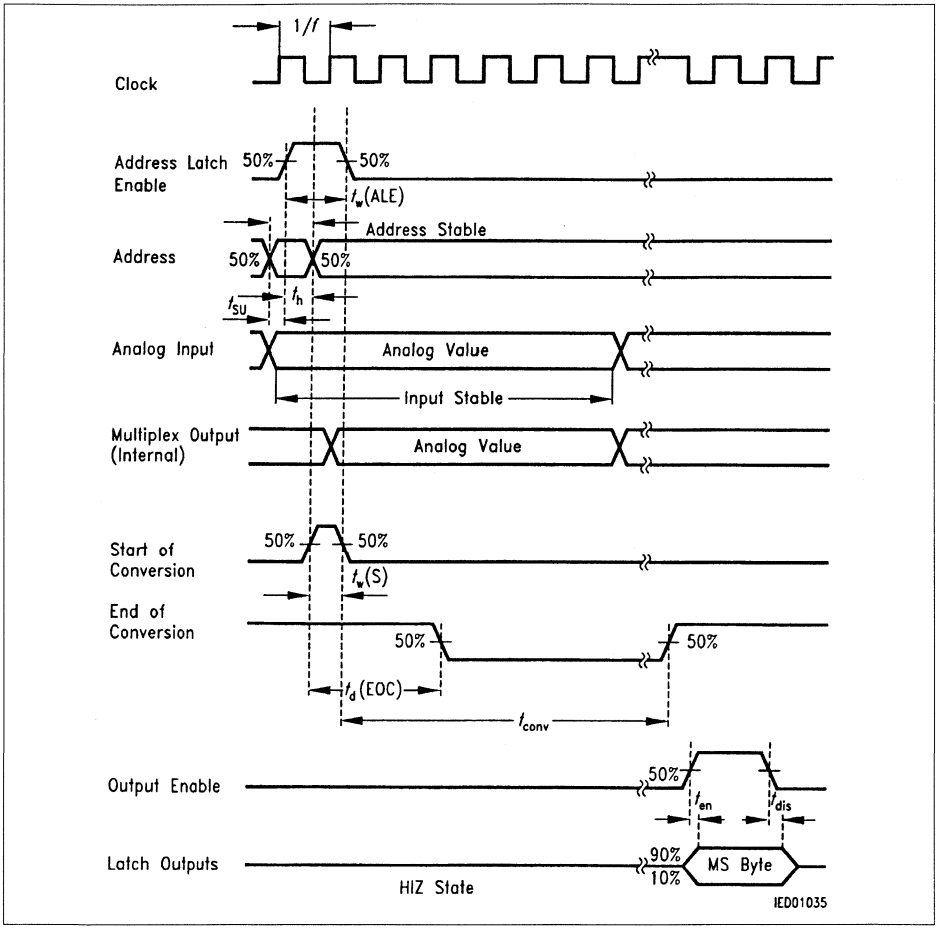


Figure 5
Operational Pulse Diagram

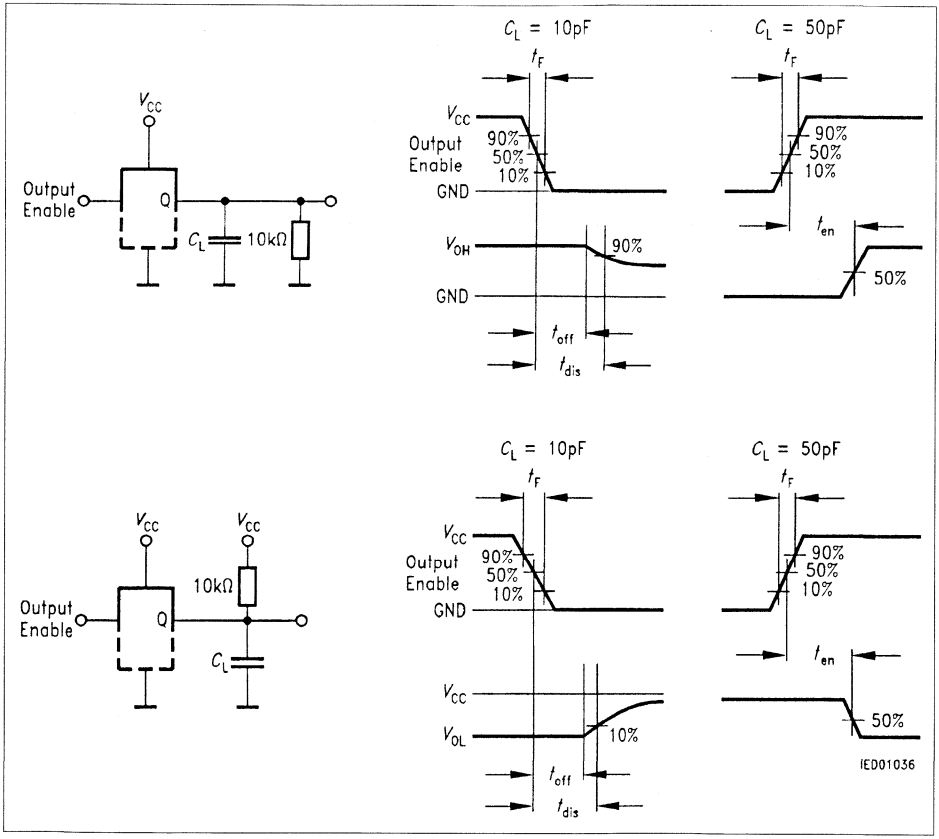


Figure 6
Tristate Test Circuits and Pulse Diagrams

Microprocessor Interface

Microprocessor interfacing is straight forward and requires only a few external gates.

Intel / Siemens Microprocessors

A typical interface is shown in **figure 7**.

- Start of conversion

  A write instruction selects one of the analog input channnels and starts the conversion Write address: ADC_CS.

  The end of conversion signal (EOC) can be used for producing an interrupt to the microprocessor (INT or $\overline{INT}$).

- Reading the conversion result

  With a read instruction the result is read from the ADC_CS address.

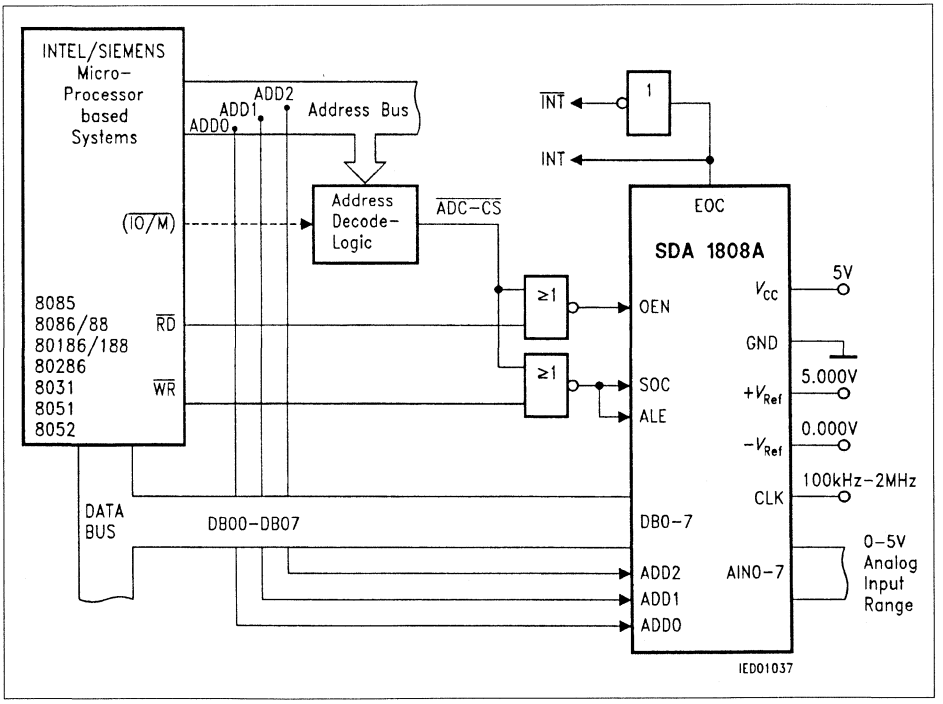


Figure 7
Microprocessor Interfacing

Motorola Microprocessors

A typical interface is shown in **figure 8**.

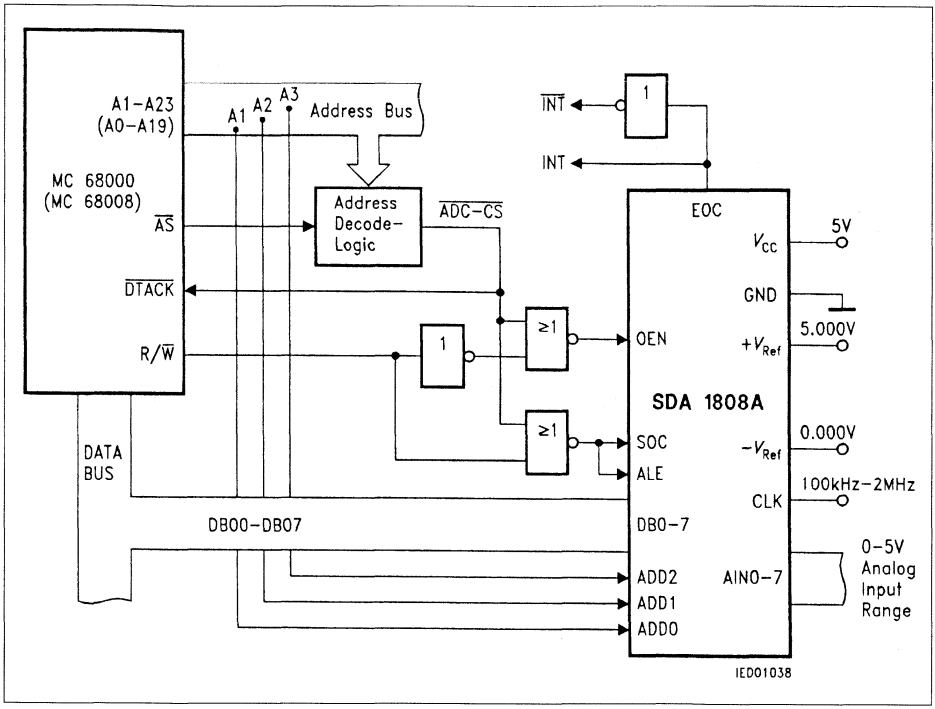


Figure 12
Microprocessor Interfacing

Application

Power Supply Decoupling

The power supply of the SDA 1808 A should be connected with a 10 µF tantalum or an electrolytic capacitor. To insure good high frequency performance, this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog Input

The high input impedance of the analog channels AIN0-AIN7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq$ AIN $\leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 30 pF, within 5 clock cycles.

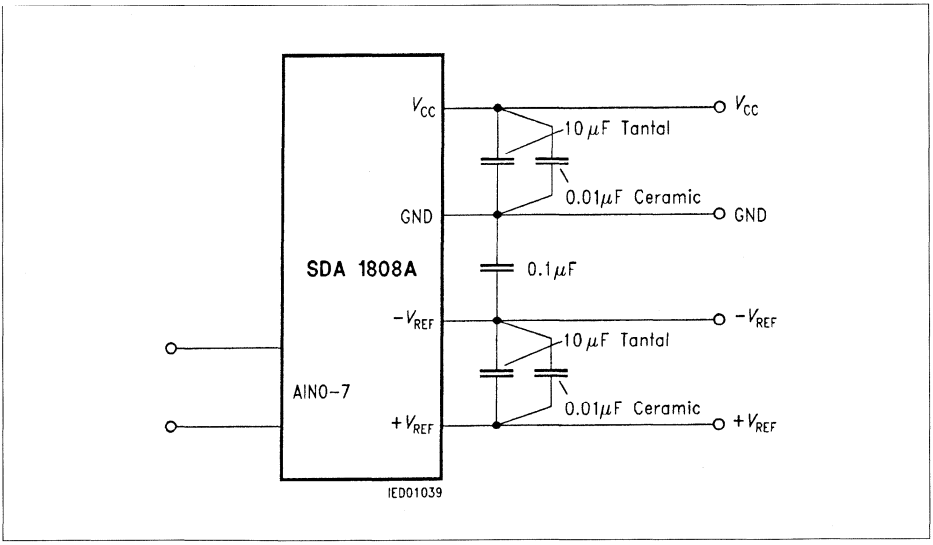


Figure 9
Capacitors

SIEMENS

Microprocessor-Compatible 10-Bit A/D Converters with 8-Channel Multiplexer

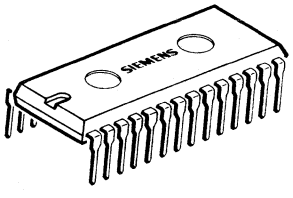
SDA 0810
SDA 1810

Preliminary Data

ACMOS IC

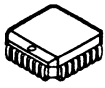
Features

- **A**dvanced **CMOS** (ACMOS) technology
- 10-bit resolution
- Total unadjusted error ± 1/2 LSB
- No missing codes
- Fast conversion time (15 µs)
- SDA 1810 D with 66-kHz sampling frequency
- Single 5 V DC supply voltage
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustments required
- Latched tristate outputs
- TTL-compatible output voltages
- Low power consumption (15 mW)



VPD 05037

P-DIP-28



VPL05039

P-LCC-28-2

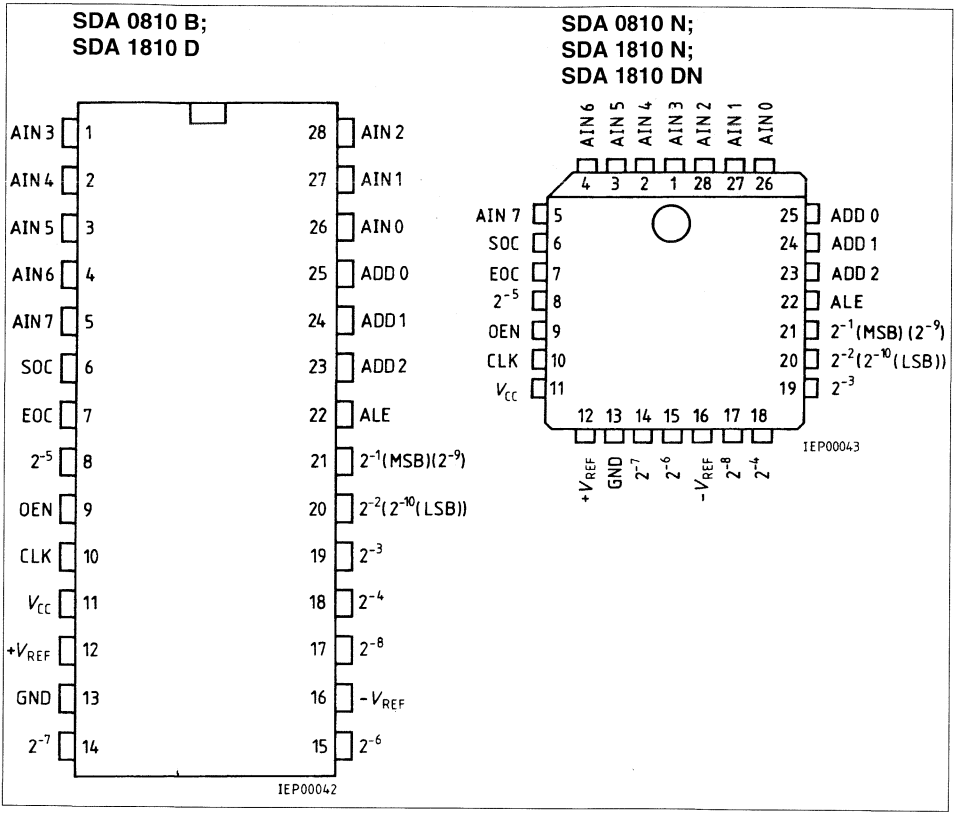
7

Type	Ordering Code	Package
S SDA 0810 B	Q67100-A8144	P-DIP-28
SDA 0810 N	Q67100-A8207	P-LCC-28-2 (SMD)
SDA 1810 D	Q67100-H8730	P-DIP-28
SDA 1810 N	Q67100-A8230	P-LCC-28-2 (SMD)
SDA 1810 DN	Q67100-H8735	P-LCC-28-2 (SMD)

SDA 0810 and SDA 1810 are monolithic 10-bit CMOS A/D converters with an 8-channel analog multiplexer and a single 5 V DC supply. They contain a microprocessor-compatible control logic and an 8-bit data bus and are pin-compatible with the industrial standard ADC 0808 and 0809. The 10-bit data stream is supplied in a 2-byte format for interfacing with 8-bit microprocessors. While the SDA 0810 can be operated at a clock frequency of 1 MHz, the SDA 1810 operates at a clock frequency of 2 MHz. SDA 1810 D offers enhanced dynamic performance for analog input frequencies up to 33 kHz.

The converters use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converters need no external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

The temperature range of the SDA 0810 N and SDA 1810 N/D is – 40 °C to 85 °C, and that of the SDA 0810 B – 40 °C to 125 °C.

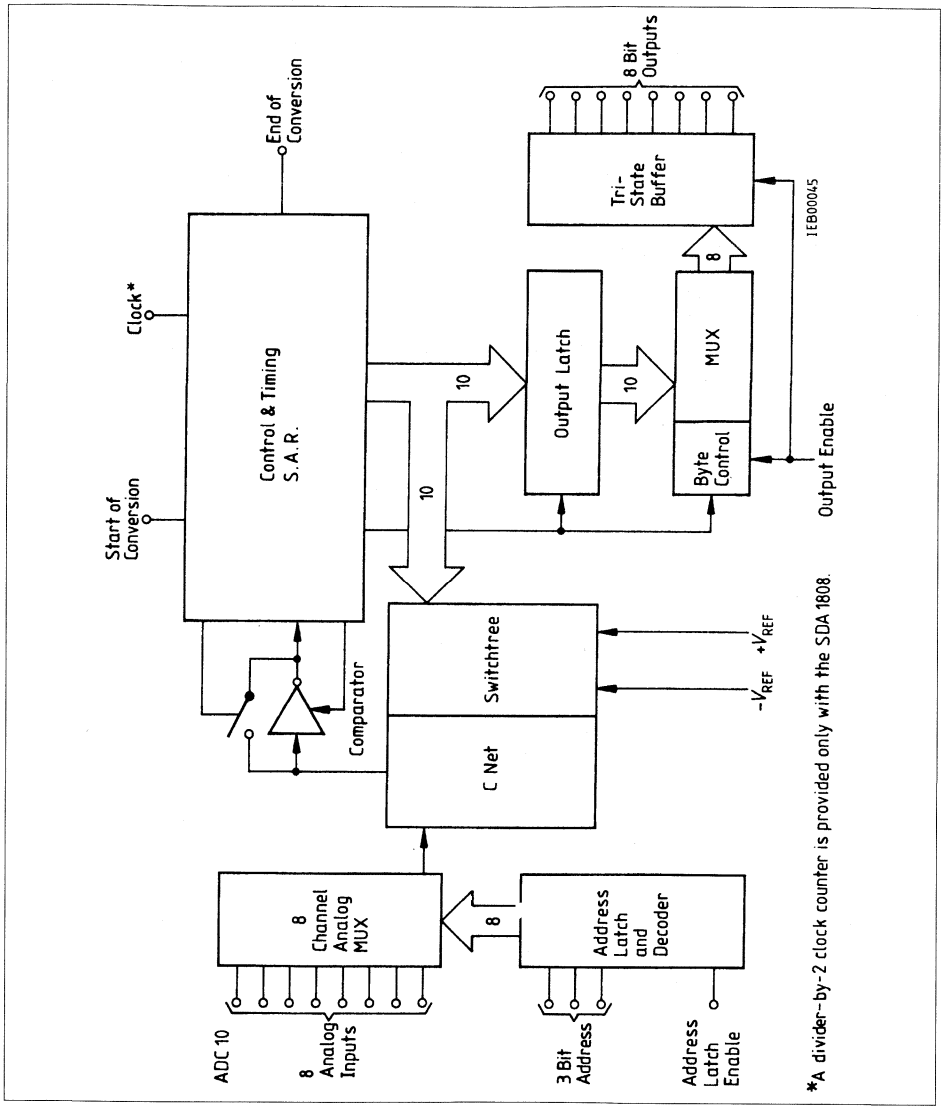


Pin Configurations
(top view)

7

Pin Definitions and Functions

Pin	Symbol	Function
1 to 5	AIN 3 to AIN 7	Analog inputs
6 7	SOC EOC	Start of conversion End of conversion
8	2^{-5}	Digital output signal
9	OEN	Output enable signal
10	CLK	External clock input
11	V_{CC}	Positive supply voltage
12	$+ V_{REF}$	Positive reference voltage
13	GND	Ground
14 to 15	2^{-7}, 2^{-6}	Digital output signals
16	$- V_{REF}$	Negative reference voltage
17 to 21	2^{-8} to 2^{-1}	Digital output signals
22	ALE	Address latch enable
23 to 25 26 to 28	ADD 2 to ADD 0 AIN 0 to AIN 2	Address inputs Analog inputs



Block Diagram

7

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 50 pF) as a sample and hold circuit, a successive-approximation register and a comparator.

The A/D converter's successive-approximation register (SAR) is reset with the positive edge of the start of conversion (SOC) pulse. The conversion starts with the next rising edge of the external clock signal after the falling edge of the SOC pulse. A conversion in process will be interrupted by an SOC pulse.

Following the rising edge of the SOC pulse, the EOC output passes to the low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator which is automatically set to zero; it has a high supply rejection factor.

A/D Converter Timing

The values stated apply to the SDA 0810, those in parentheses to the SDA 1810.

After a conversion has been started, the analog voltage at the selected input channel is sampled for 4 (8) external clock cycles which will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitance of approx. 50 pF within those 4 (8) clock cycles.

Conversion of the sampled analog voltage takes place between the 5th and 15th (10th and 30th) clock cycle after sampling has been completed. In the 15th (30th) clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 16th (32nd) clock cycle.

Multiplexer

The converter provides eight multiplexed analog input channels. The input channels are selected by programming three address lines (AD2, AD1, AD0).

Table 1 shows the input states for the address lines that select a channel. The address is latched on the rising slope of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Reading the Conversion Results

The data is read as two 8-bit bytes. The digital outputs of the converters are positive true. Data is presented left-justified and high byte first. The first OEN high after completion of a conversion enables high byte (2^{-1} to 2^{-8}) to the output buffers, the second OEN pulse enables the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are grounded. The byte control logic determines which byte is to be read. With each reading operation a flipflop is toggled so that in successive reading operations the bytes are output alternately. This flipflop is always reset to the high byte at the end of a conversion.

Data Bit Location

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
High byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low byte	2^{-9}	2^{-10}	0	0	0	0	0	0

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage [1]	V_{CC}		6.5	V
Input voltage range, any input	V_I	− 0.3	V_{CC} + 0.3	V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	− 65	125	°C
Thermal resistance system ambient				
P-DIP-28	$R_{th\,SA}$		50	K/W
P-LCC-28-2	$R_{th\,SA}$		70	K/W

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{CC}	4.5	5	6	V
Positive reference voltage [2]	+ V_{REF}		V_{CC}	V_{CC} +0.1	V
Negative reference voltage	− V_{REF}	− 0.1	0		V
Differential reference voltage [10]	V_{REF} = + V_{REF} − (− V_{REF})		5		V
Analog input range	V_{AIN}	V_{REF}		+ V_{REF}	V
Slew rate [11] (f_{CLK} = 1 MHz/2 MHz)					
SDA 0810 B/N; SDA 1810 N	*SR*			78	mV/µs
Start pulse duration	$t_{W\,(S)}$	200			ns
Address load control pulse width	$t_{W\,(ALE)}$	200			ns
Address setup time	t_{Setup}	50			ns
Address hold time	t_{Hold}	50			ns
Clock frequency SDA 0810	f_{CLK}	50	640	1000	kHz
SDA 1810	f_{CLK}	100	1280	2000	kHz
Ambient temperature					
SDA 0810 N; SDA 1810 N/D	T_A	− 40		85	°C
SDA 0810 B	T_A	− 40		125	°C

For notes refer to 3 pages hereafter.

Characteristics in the Operating Temperature Range
V_{CC} = 4.75 to 5.25 V, unless otherwise specified

Total Component

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} – 1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} – 0.4			V	I_Q = – 360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state output current (high impedance-state)	I_{QZ}			3	µA	V_Q = 5 V
Output current	I_{QZ}			– 3	µA	V_Q = 0
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			– 1	µA	V_I = 0
Supply current	I_{CC}		0.3	3	mA	f_{CLK} = f_{CLK} (typ)
Input capacitance, control inputs	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance between pins 12 and 16	R	1	1000		kΩ	

Characteristics
Analog Multiplexer V_{CC} = 5 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Channel ON-state current[3]	I_{ON}			2	µA	V_I = 5 V, f_{CLK} = f_{CLK} (typ)
				– 2	µA	V_I = 0 V, f_{CLK} = f_{CLK} (typ)
Channel OFF-state current	I_{OFF}		10	200	µA	V_{CC} = 5 V, T_A = 25 °C, V_I = 5 V
			– 10	– 200	nA	V_{CC} = 5 V, T_A = 25 °C, V_I = 0
				1	µA	V_{CC} = 5 V, V_I = 5 V
				– 1	µA	V_{CC} = 5 V, V_I = 0

For notes refer to 2 pages hereafter.

Characteristics

T_A = 25 °C, V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V, f_{CLK} = f_{CLK} (typ), unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage sensitivity[4]	k_{SVS}		± 0.05		%/V	V_{CC} = + V_{REF} = 4.75 V to 5.25 V T_A = – 40 °C to 85 °C
Linearity error[5]				± 0.5	LSB	
Zero error[6] (except SDA 1810 D)				± 0.5	LSB	
Total unadjusted error[7] SDA 0810 N SDA 0810 B SDA 1810 N				± 0.5 ± 0.5 ± 1	LSB LSB LSB	T_A = – 40 °C to 85 °C T_A = – 40 °C to 125 °C T_A = – 40 °C to 85 °C f_{CLK} = 1 MHz
Output enable time **(figure 1)**	t_{en}		80	150	ns	C_L = 50 pF, R_L = 10 kΩ
Output disable time **(figure 1)**	t_{dis}		40	95	ns	C_L = 10 pF, R_L = 10 Ω
Output turn-OFF time **(figure 1)**	t_{OFF}		20	60	ns	C_L = 10 pF, R_L = 10 kΩ
Conversion time[8] SDA 0810	t_{Conv}	15	25	320	µs	f_{CLK} = 1 MHz/ 640 kHz/50 kHz
Conversion time[8] SDA 1810/1810 D	t_{Conv}	15	25	320	µs	f_{CLK} = 2 MHz/ 1280 kHz/100 kHz
Delay time, output EOC[9]	$t_{D\,(EOC)}$	0		200	ns	

Characteristics SDA 1810 D only

T_A = 25 °C, V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V, f_{CLK} = 1.28 MHz unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Total Unadjusted Error	*TUE*		± 0.5	± 1.25	LSB	T_A = – 40 °C to 85 °C
Integral nonlinearity	*INL*			± 0.5	LSB	T_A = – 40 °C to 85 °C
Differential nonlinearity	*DNL*		± 0.25	± 0.5	LSB	T_A = – 40 °C to 85 °C
Gain error	*GE*		± 0.125	± 0.5	LSB	T_A = – 40 °C to 85 °C
Zero error	*OFS*		± 0.25	± 1	LSB	T_A = – 40 °C to 85 °C
Sampling rate	f_S			66	kHz	f_{CLK} = 2 MHz
Effective resolution			8.8		bits	f_{AIN} = 30 kHz

For notes refer to next page.

Notes

1) All voltage values refer to the network's ground terminal.

2) Care must be taken that this rating is observed, even during power-up.

3) The channel on-state current is primarily generated by the current of the Schmitt trigger and varies directly with the clock frequency.

4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies. Supply voltage and + V_{REF} are changing together and the change of accuracy is measured with respect to full-scale deflection.

5) The linearity error is the maximum deviation from a straight line to the end points of the A/D transfer characteristic.

6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

7) The total unadjusted error is the total-of-linearity error, zero error, and full-scale error.

8) SDA 0810: $t_{Conv\ max} = 16 \times 1/f_{CLK}$, $t_{Conv\ min} = 15 \times 1/f_{CLK}$; including sampling time
SDA 1810: $t_{Conv\ max} = 32 \times 1/f_{CLK}$, $t_{Conv\ min} = 30 \times 1/f_{CLK}$; including sampling time

9) Refer to the operating pulse diagram.

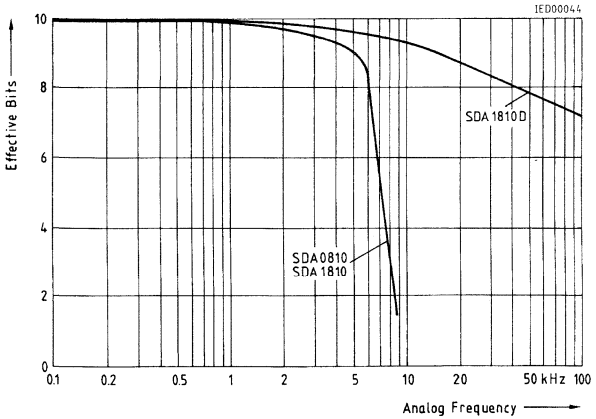
10) For typical error versus reference voltage span refer to diagram next page.

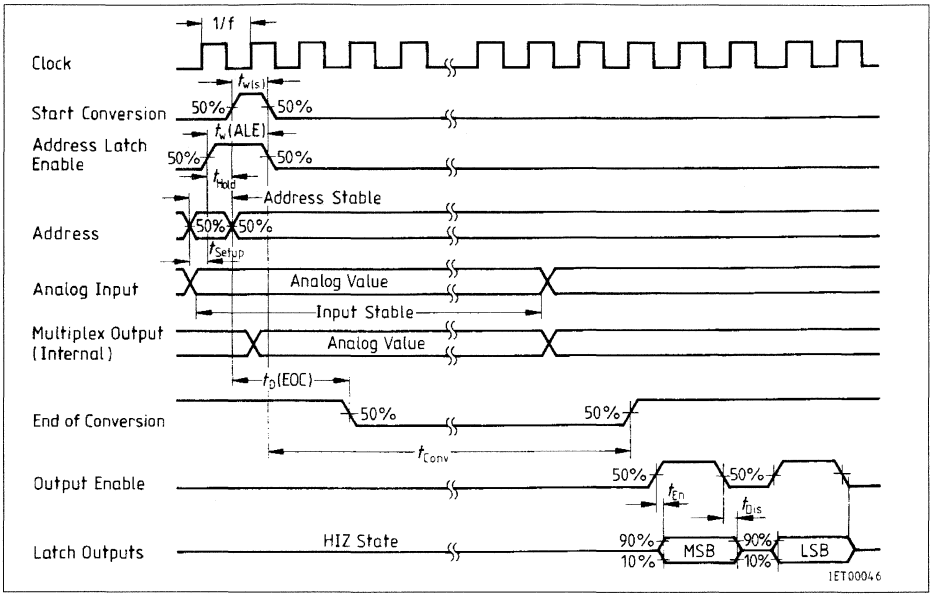
11) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full-scale errors (not SDA 1810 D!) Filtering by a low pass ($R = 2\ k\Omega$, $C = 100$ nF) or use of an external sample-and-hold is then required.

7

Effective Resolution versus Input Frequency

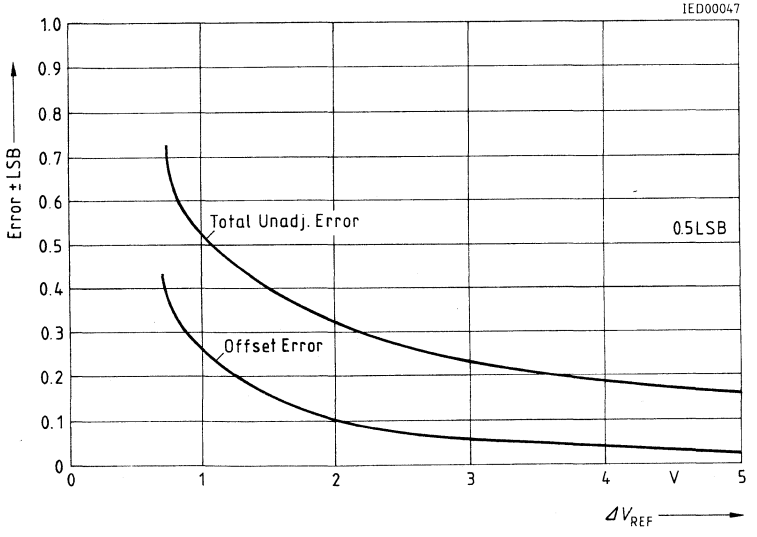
$V_{CC} = 5.0$ V, $+ V_{REF} = 5$ V, $- V_{REF} = 0$ V, $f_{CLK} = f_{CLK\ (typ)}$





Operating Pulse Diagram

Typical Error versus Reference Voltage Span (SDA 0810 A/B/N, SDA 1810 N)
(Total unadjusted error including offset errors, full-scale errors, linearity errors and multiplexer errors). V_{CC} = 5.0 V; $f_{CLK} = f_{CLK\,(typ)}$; $\Delta V_{REF} = +V_{REF} - (-V_{REF})$



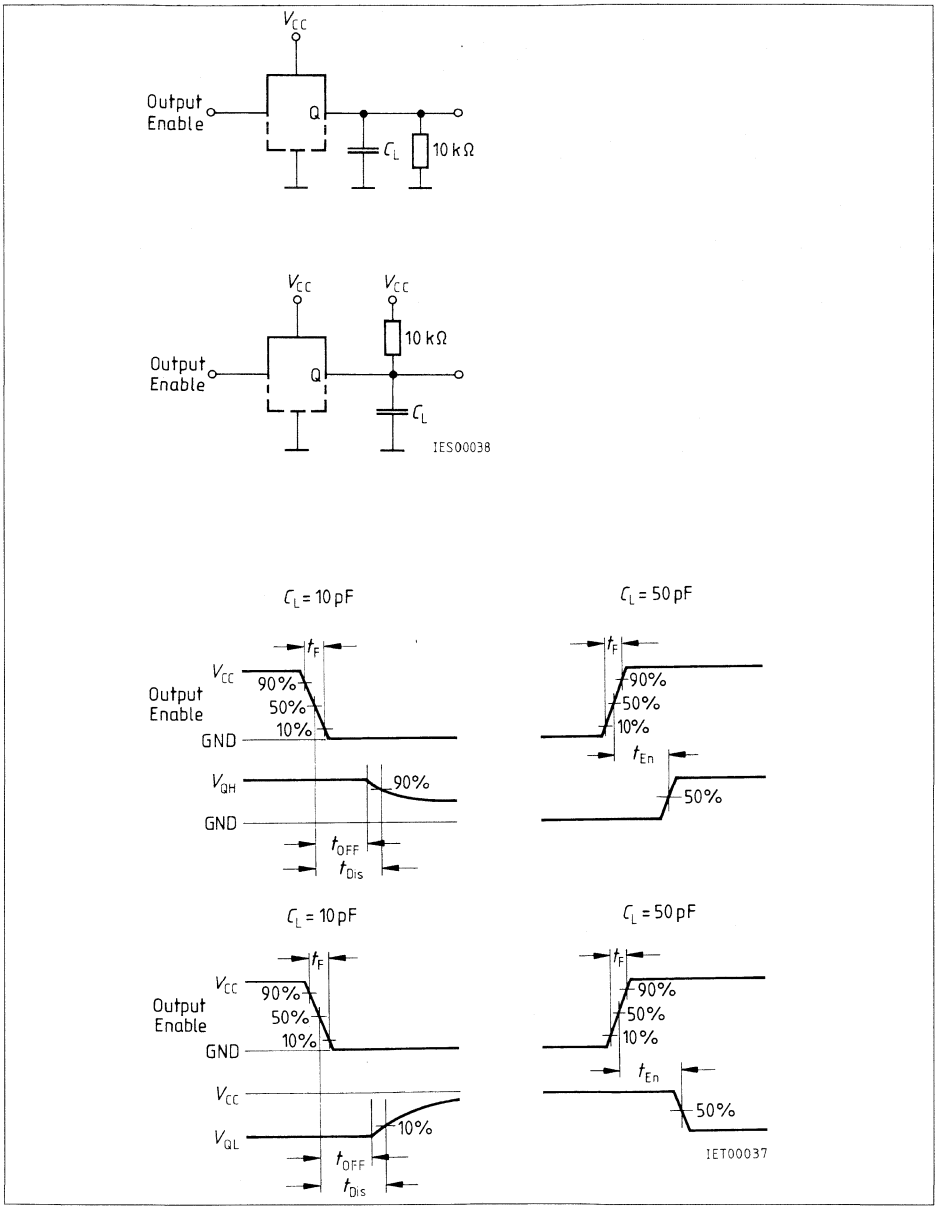


Figure 1
Tristate Measurement Circuits and Pulse Diagrams

Microprocessor Interface

Microprocessor interfacing is straightforward and requires only a few external gates.

INTEL Microprocessors

A typical interface is shown in **figure 2**.

Start of Conversion

A write instruction selects one of the analog input channels and starts the conversion.

Write address: $\overline{\text{ADC\_CS}}$

The end of conversion-signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).

Reading the Conversion Result

With the first read instruction the high byte is read from the $\overline{\text{ADC\_CS}}$ address, with the second read instruction the low byte is read.

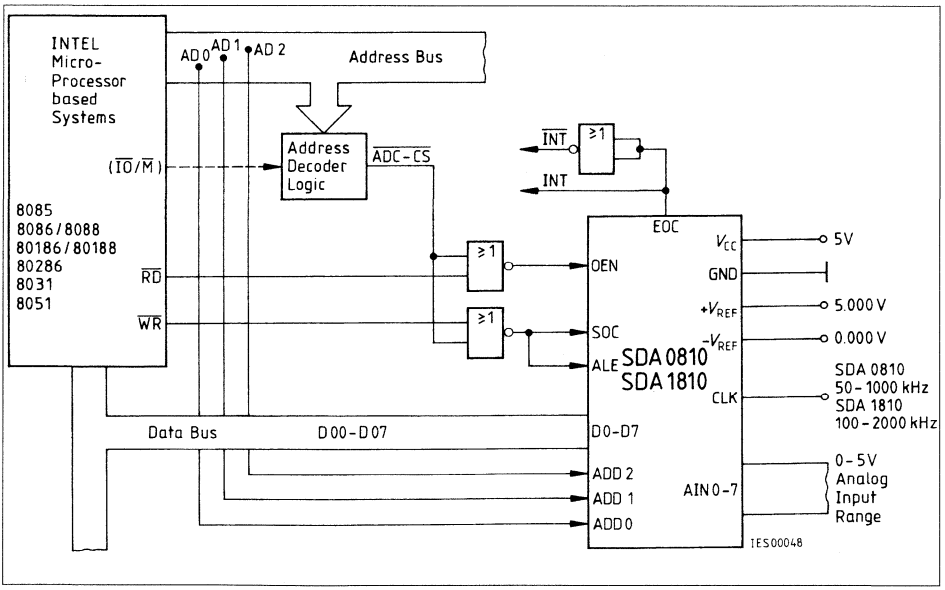


Figure 2

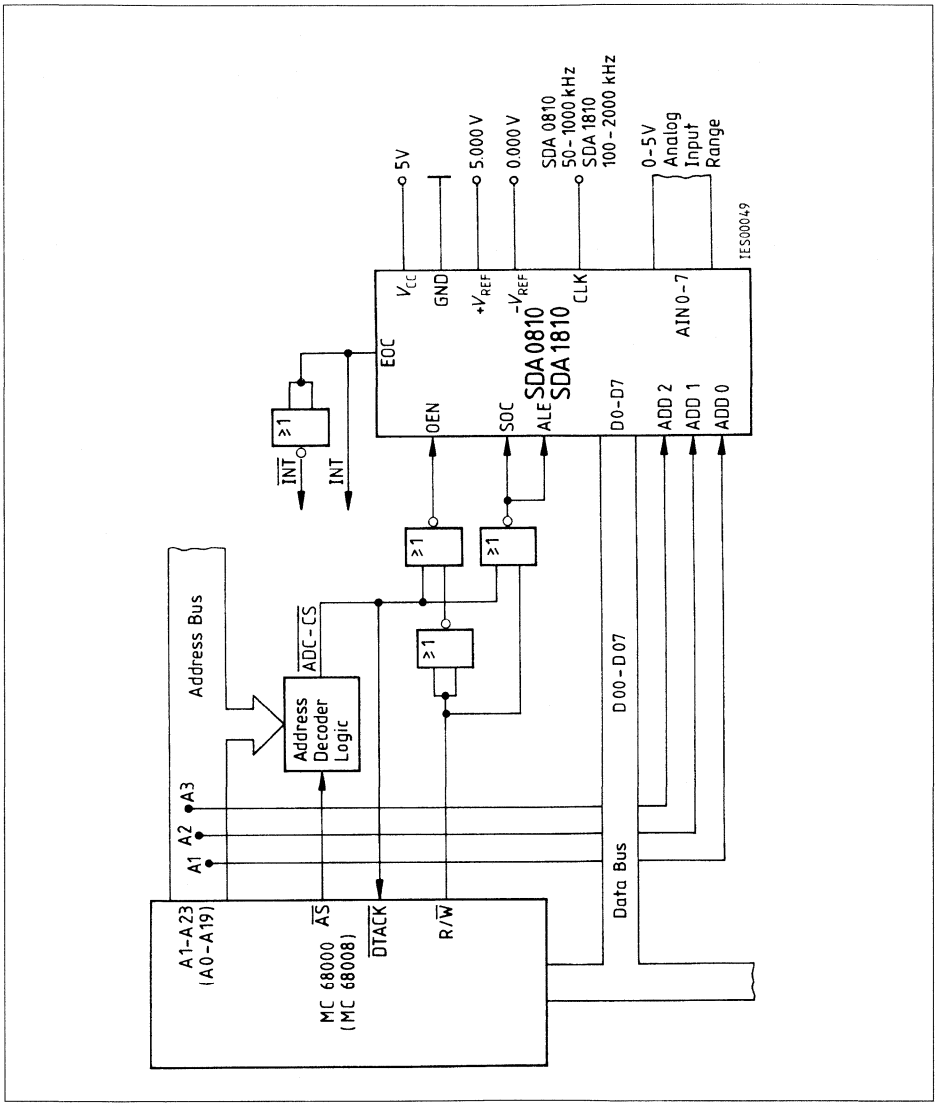


Figure 3
Motorola Microprocessors

A typical interface is shown in **figure 3**.

Application Hints

Power Supply Decoupling

The power supply should be connected with a 10 µF tantalum or an electrolytic capacitor. To ensure good HF performance this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors, a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 0.1 µF ceramic capacitor should be placed between pins – V_{REF} and GND.

Analog Input

The high input impedance of the analog channels AIN 0 to AIN 7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq AIN \leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 4 clock cycles for the SDA 0810 and 8 clock cycles for the SDA 1810.

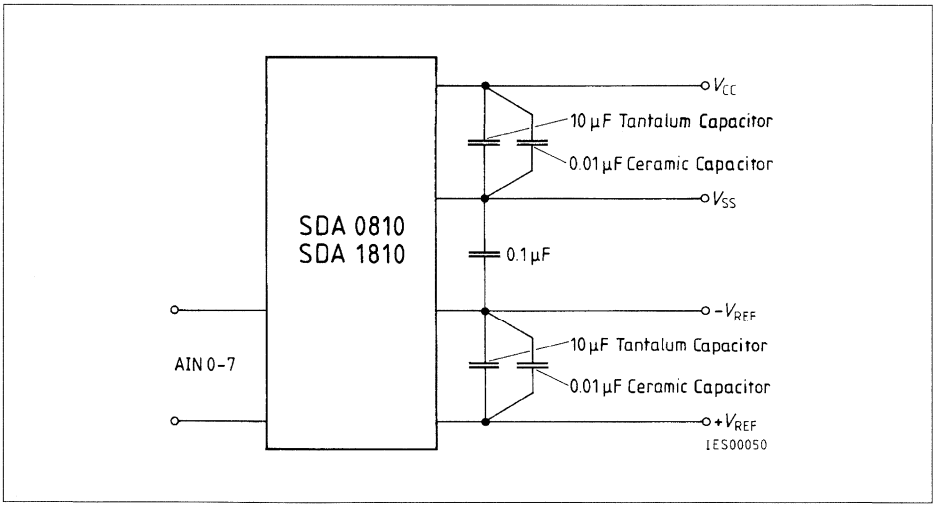


Figure 4
Capacitors

SIEMENS

Microprocessor-Compatible 10-Bit Sampling A/D Converter with 8-Channel Multiplexer

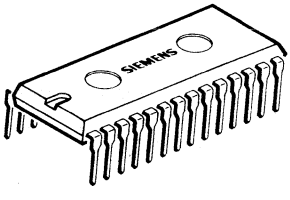
SDA 1810 A

Advance Information

ACMOS IC

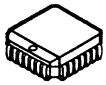
Features

- **A**dvanced **CMOS** (ACMOS) technology
- 10-bit resolution
- 110-kHz sampling rate
- Total unadjusted error ± 1/2 LSB
- Fast conversion time (6 µs)
- Sampling time 2.5 µs
- No missing codes
- Single 5 V DC supply
- 8-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- No offset or gain adjustment required
- TTL-compatible output voltages
- Latched tristate outputs
- Low power consumption (10 mW during conversion, 50 µW idle)
- Offset calibration circuit



VPD 05037

P-DIP-28



VPL05039

P-LCC-28-2

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	Type	Ordering Code	Package
▼	SDA 1810 A	Q67100-A8352	P-DIP-28
▼	SDA 1810 AN	Q67100-A8353	P-LCC-28-2 (SMD)

▼ = New type

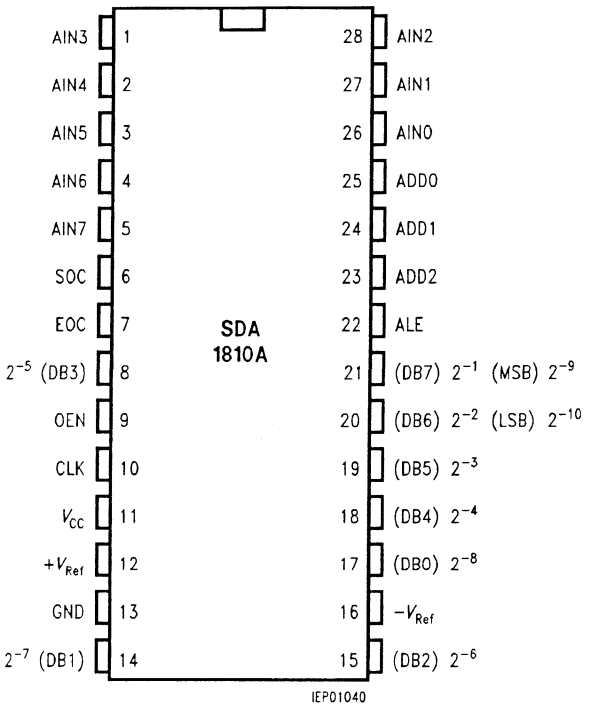
General Description

SDA 1810 A is a monolithic CMOS 10-bit A/D converter with a single supply voltage of 5V DC. It contains a microprocessor-compatible control logic and an 8-bit data bus. It is pin-compatible with the industry standards 0808 and 0809. The 10-bit data stream is supplied in a 2-byte parallel format for interfacing with 8-bit microprocessors. The SDA 1808 A operates at a clock frequency of 2 MHz and offers enhanced dynamic performance for sampling rates up to 110 kHz.

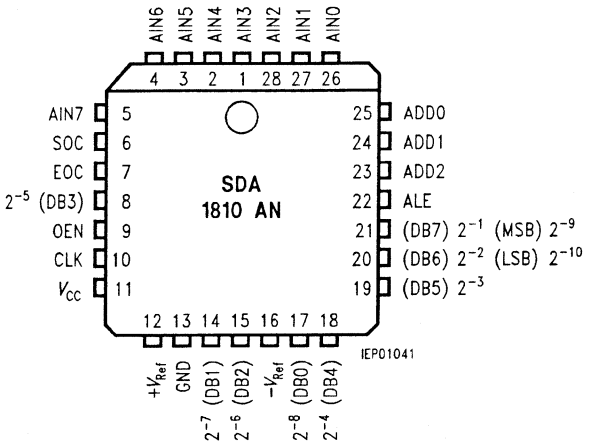
The converter uses the method of successive approximation by means of a capacitor network. The converter features a temperature-stabilized differential comparator, an 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The converter does not need any external offset or gain adjustment. Easy interfacing to microprocessors is provided by 3-bit address latches, output latches and an 8-bit tristate data bus.

The temperature range of the SDA 1810 A is -40 °C to 85 °C.

SDA 1810 A



SDA 1810 AN



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol 1st Byte	Symbol 2nd Byte	Function
1 to 5	AIN 3 to AIN 7		Analog inputs, channel 3 to channel 7
6	SOC, $T/\overline{H}$		Start of conversion
7	EOC		End of conversion
8	(DB3), 2^{-5}	0	Digital output signal
9	OEN		Output enable
10	CLK		External clock input
11	V_{CC}		Positive supply voltage
12	+ V_{REF}		Upper reference voltage
13	GND		Ground
14, 15	(DB1, DB2) 2^{-7}, 2^{-6}	0	Digital output signals
16	- V_{REF}		Lower reference voltage
17 to19	2^{-8}, 2^{-4}, 2^{-3} (DB0, 4, 5)	0	Digital output signals
20	2^{-2}, (DB6)	2^{-10}, (LSB)	Digital output signals
21	2^{-1}, (MSB)	2^{-9}	Digital output signals
22	ALE		Address latch enable
23 to 25	ADD2 to ADD0		Address inputs
26 to 28	AIN0 to AIN2		Analog inputs

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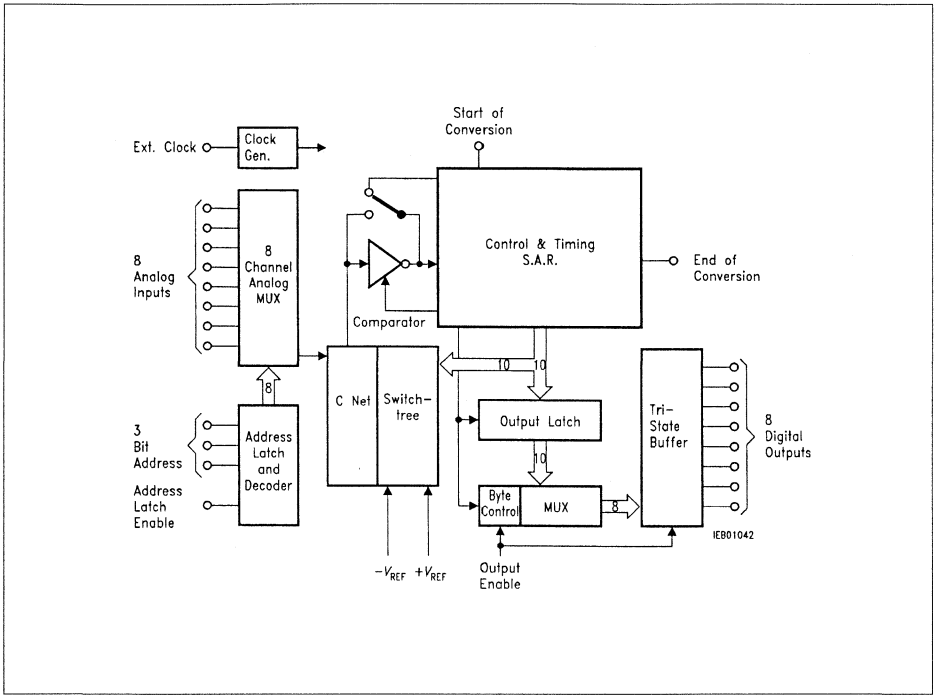

Figure 1
Block Diagram

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 30 pF) as a sample and hold circuit, a successive approximation register and a comparator.

The A/D converter's successive approximation register (SAR) is reset at the positive edge of the start of conversion (SOC) pulse. The conversion starts with sampling the analog signal. A conversion in process will be interrupted by a SOC pulse.

Following the rising edge of the SOC pulse, the end of conversion output (EOC) passes to low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator for high power supply rejection.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 5 external clock cycles and will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitor of approximately 30 pF within those 5 clock cycles.

Conversion of the sampled analog voltage takes place between the 6th and 18th clock cycle after sampling has been completed. In the 18th clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 18th clock cycle.

Multiplexer

The converter provides 8 multiplexed analog input channels. A particular input channel is selected by programming 3 address lines (ADD2, ADD1, ADD0). The table shows the input states for the address lines to select a channel. The address is latched on the rising edge of the ALE signal.

Address Lines			Select. Analog Channel
ADD2	ADD1	ADD0	AIN
L	L	L	AIN0
L	L	H	AIN1
L	H	L	AIN2
L	H	H	AIN3

Address Lines			Select. Analog Channel
ADD2	ADD1	ADD0	AIN
H	L	L	AIN4
H	L	H	AIN5
H	H	L	AIN6
H	H	H	AIN7

Reading the Conversion Results

The data is read as two 8-bit bytes. The converter's digital outputs are positive true. Data is presented left-justified and high byte first. The first OEN high after completing a conversion will enable the high byte (2^{-1} to 2^{-8}) to the output buffers, the second OEN pulse will enable the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are grounded. The BYTE CONTROL logic determines which byte is to be read. With each reading operation a flipflop is toggled so that in successive reading operations the bytes are output alternately. This flipflop is always reset to the high byte at the end of a conversion.

Data Bit Locations

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
High byte	2^{-1} (MSB)	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low byte	2^{-9}	2^{-10} (LSB)	0	0	0	0	0	0

Autocalibration

An autocalibration circuit is included. It corrects offset errors only. Offset errors are adjusted in each conversion cycle, an initial offset calibration is done by power up.

Power-Up

An autocalibration cycle is started by power up. The autocalibration cycle takes 256-clock cycles. A start of conversion signal interrupts this autocalibration cycle and gives a normal conversion result (with increased offset errors) the autocalibration cycle will be finished automatically after the conversion.

Power Consumption

The current consumption is typical 2 mA during a conversion and during autocalibration (power-on). If no conversion (calibration) is running, the power consumption will be typically 10 µA.

T / $\overline{H}$ Mode

Normal conversion is started by a SOC high pulse. The min. start pulse duration is 100 ns. In this case the sample point is defined by the rising slope of CLK (**see figure 2a**).
If the SOC signal exceeds 5 CLK pulses the sample point will be defined by the falling slope of SOC (**see figure 2b**).

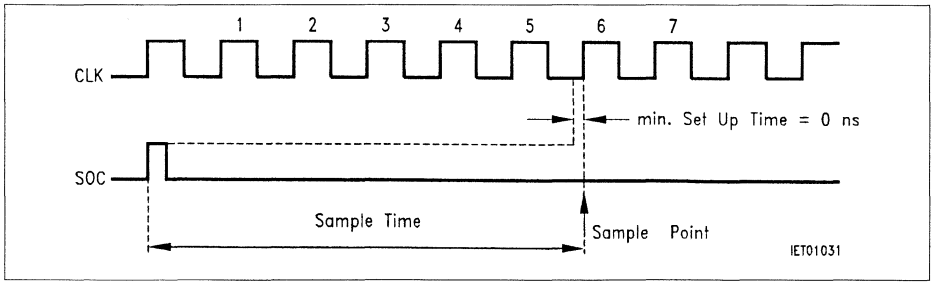

Figure 2 a)

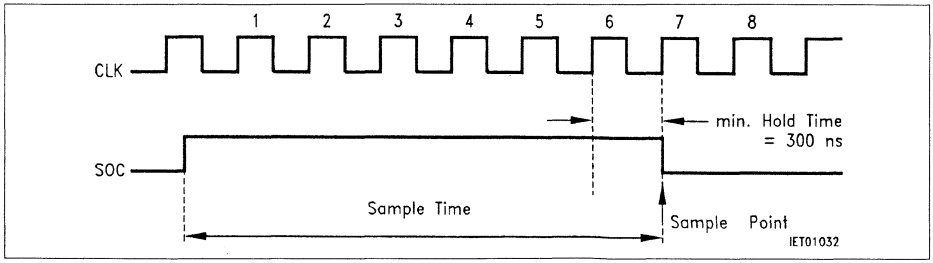

Figure 2 b)

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 3**.

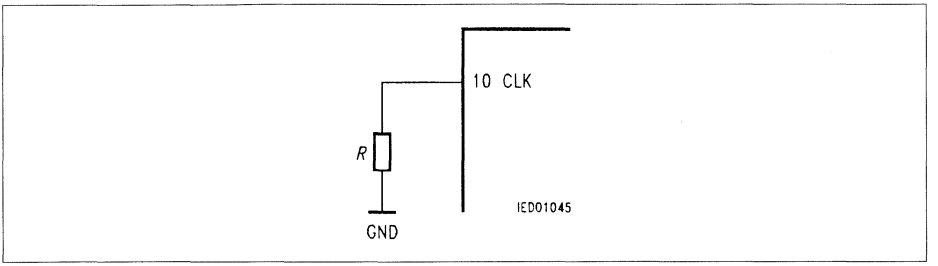

Figure 3
The Internal Clock Frequency only Depends on the *R* Value

The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.1 to 2.2 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device. Therefore, for precisely defined conversion times use of an external clock generator is recommended.

External Clock Operation

The required circuitry for external clock operation is shown in **figure 4**.

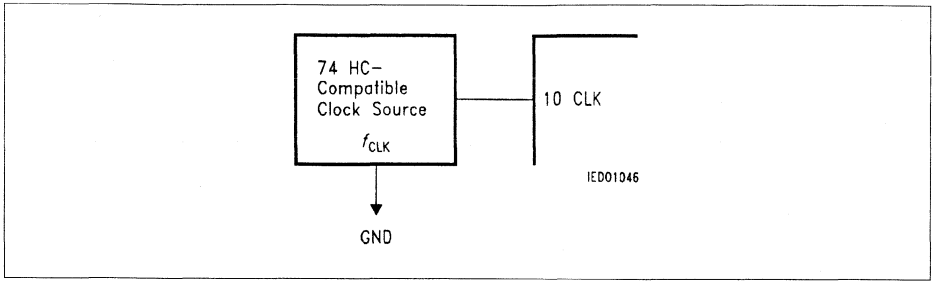

Figure 4
Circuitry for External Clock Operation

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The external clock source has to provide 0.8 V max. for low voltage level and 3.5 V min. for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. T/$\overline{H}$ signal (see SOC). Synchronizing should be provided for optimum performance (see A/D converter timing). Note that the specifications referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.1 to 2.2 MHz.

Absolute Maximum Ratings

Parameter		Symbol	Limit Values		Unit
			min.	max.	
Supply voltage [1]		V_{CC}		6.5	V
Input voltage range (all inputs)		V_I	− 0.3	V_{CC} + 0.3	V
Thermal resistance (system - air)	P-DIP-28	$R_{th\ SA}$		50	K/W
	P-LCC-28-2	$R_{th\ SA}$		70	K/W
Junction temperature		T_j		125	°C
Storage temperature		T_{stg}	− 65	125	°C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Operating Range					
Supply voltage	V_{CC}	4.5	5	6	V
Upper ref. voltage [2]	$+V_{REF}$		V_{CC}	$V_{CC+0.1}$	V
Lower ref. voltage	$-V_{REF}$	-0.1	0		V
Differential ref. voltage	$\Delta\ V_{REF}$		5		V
Analog input range	V_{AIN}	$-V_{REF}$		$+V_{REF}$	V
Start pulse duration	$t_{w\ (S)}$	100			ns
Address load control pulse width	$t_{w\ (ALE)}$	100			ns
Address setup time	t_{Setup}	20			ns
Address hold time	t_{Hold}	20			ns
Clock frequency	f_{CLK}	100		2200	kHz
Ambient temperature	T_A	-40		85	°C

[1] All voltages are referred to ground.

[2] Care must be taken that this rating is observed even during power up.

Characteristics

V_{CC} = 4.75V to 5.25V, f_{CLK} = 2 MHz, unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} - 1.5			V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}			1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} - 0.4			V	I_Q = - 360 µA
Low-level output voltage, data outputs	V_{QL}			0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}			0.45	V	I_Q = 1.2 mA
OFF-state (high-impedance) Output current	I_{QZ}			3	µA	V_Q = 5 V
	I_{QZ}			-3	µA	V_Q = 0 V
Control input current at max. input voltage	I_I			1	µA	V_I = 5 V
Low-level control input current	I_{IL}			-1	µA	V_I = 0 V
Supply current	I_{CC}		2.0	2.5	mA	during conversion
			10	50	µA	idle
Input capac.,control inputs	C_I		10	15	pF	T_A = 25 °C
Output capacitance, data outputs	C_Q		10	15	pF	T_A = 25 °C
Resistance from pin12 to16	R	1	1000		kΩ	

7

Characteristics

$V_{CC} = +V_{REF} = 5V$, $-V_{REF} = 0V$, $f_{CLK} = 2$ MHz, $T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog Multiplexer V_{CC} = 5V						
Channel ON-state current [3]	I_{ON}			2	µA	$V_I = 5$ V
				- 2	µA	$V_I = 0$ V
Channel ON-state resistance	R_{ON}		1		kΩ	
OFF-state current (high impedance state)	I_{OFF}		10	200	nA	$V_{CC} = 5$ V, $T_A = 25$ °C, $V_I = 5$ V
			-10	- 200	nA	$V_{CC} = 5$ V, $T_A = 25$ °C, $V_I = 0$V
				1	µA	$V_{CC} = 5$ V, $V_I = 5$ V
				-1	µA	$V_{CC} = 5$ V, $V_I = 0$ V
Supply voltage sensitivity [4]	k_{SVS}		± 0.05		% / V	$V_{CC} = + V_{REF} = 4.75$ V to 5.25 V
Total unadjusted error [7]	*TUE*			0.5	LSB	
Zero error [6]	*OFS*		± 0.25	0.5	LSB	
Integral nonlinearity [5]	*INL*			0.5	LSB	
Differential nonlinearity [5]	*DNL*		± 0.25	0.5	LSB	
Gain error	*GE*		± 0.125	0.5	LSB	
Sampling rate	f_S			110	kHz	$f_{CLK} = 2$ MHz
Effective number of bits	*ENOB*		9.3		bits	$f_{AIN} = 50$ kHz
Output enable time (**fig. 6**)	t_{en}		25	50	ns	$C_L = 50$ pF, $R_L = 10$ kΩ
Output disable time (**fig. 6**)	t_{dis}		40	95	ns	$C_L = 10$ pF, $R_L = 10$ kΩ
Output switch-OFF time (**fig. 6**)	t_{OFF}		10	20	ns	$C_L = 10$ pF, $R_L = 10$ kΩ
Sample time [8]	t_{sample}	2.5	6	60	µs	$f_{CLK} = 2$ MHz / 1 MHz / 100 kHz
Conversion time [8]	t_{conv}	5	12	120	µs	
Delay time, output EOC [9]	$t_{d\,EOC}$	0	20	50	ns	

3) Channel on state current is primarily generated by the bias current into or out of the threshold detector and it varies directly with the clock frequency.

4) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies.

5 The linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.

6) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

7) Total unadjusted error is the max. sum of linearity error, zero error, integral and differential nonlinearity.

8) $t_{conv\,max} = 12.1/f_{CLK}$, $t_{sample\,min} = 5.1/f_{CLK}$, $t_{sample\,max} = 6.1/f_{CLK}$;

9) Refer to operating pulse diagram.

Characteristics

V_{CC} = $+V_{REF}$ = 5V, $-V_{REF}$ = 0V, f_{CLK} = 2 MHz, T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Performance [10) 11)]						
Signal-to-noise ratio	*SNR*	59	60		dB	Full scale input sine-wave 1 kHz, *f* sampling is 100 kHz
		56	58		dB	Full scale input sine-wave 1 kHz, *f* sampling is 100 kHz
Total harmonic distortion	*THD*		70		dB	Full scale input sinewave 50 kHz, *f* sampling is 100 kHz
Full power bandwidth (-3 dB)	*BW*		4		MHz	
Aperture delay time			5		ns	SOC pin, T / $\overline{H}$ condition

10) *SNR* includes harmonic distortion.

11) Sample tested at 25 °C .

7

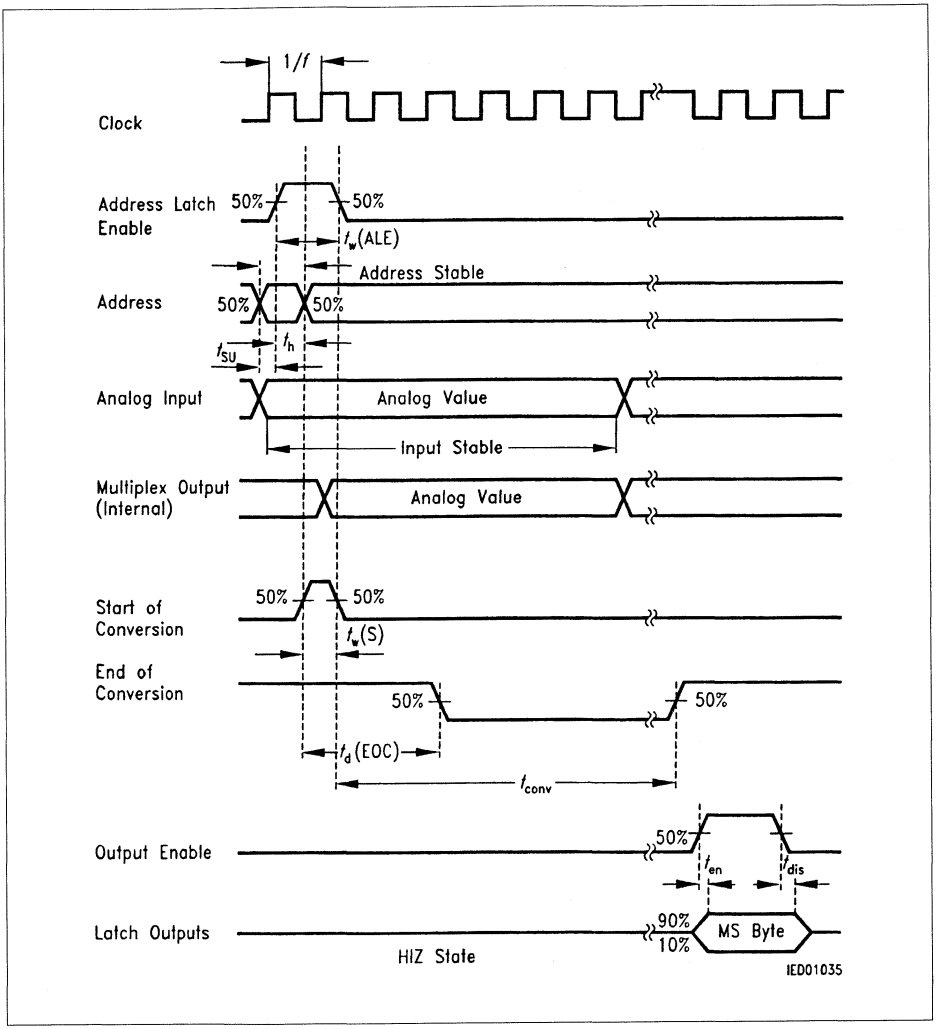


Figure 5
Operational Pulse Diagram

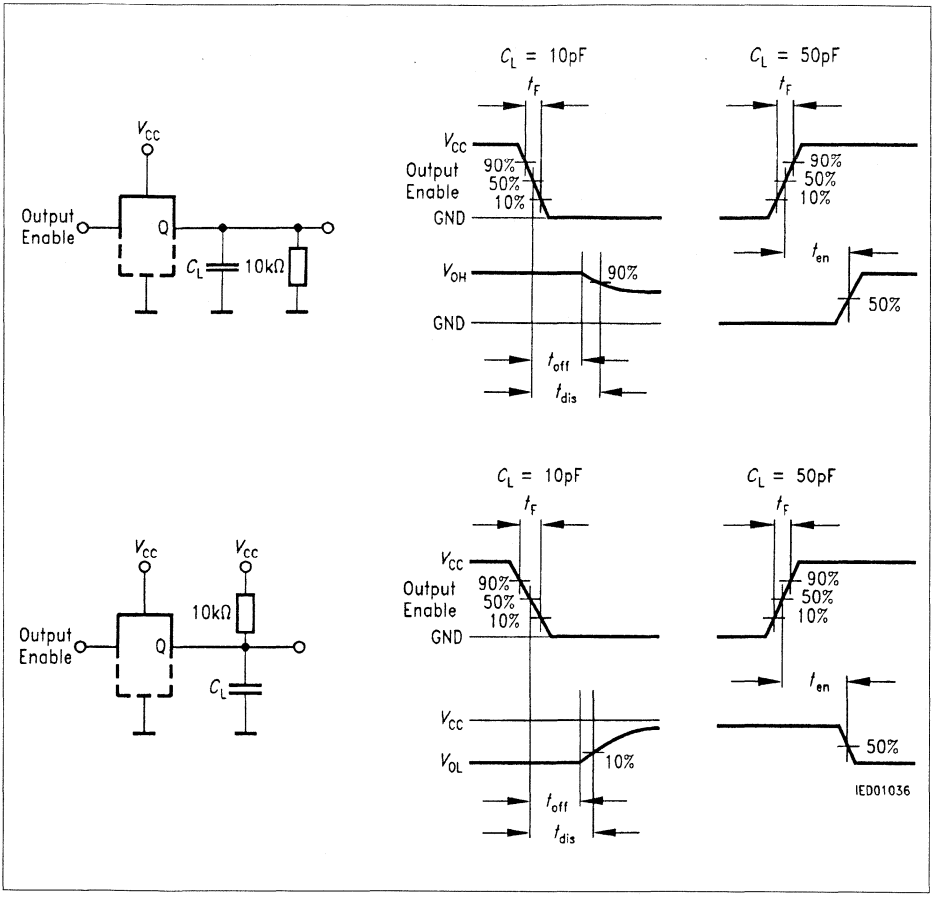


Figure 6
Tristate Test Circuits and Pulse Diagrams

Microprocessor Interface

Microprocessor interfacing is straight forward and requires only a few external gates.

Intel / Siemens Microprocessors

A typical interface is shown in **figure 7**.

- Start of conversion

  A write instruction selects one of the analog input channnels and starts the conversion Write address: ADC_CS.

  The end of conversion signal (EOC) can be used for producing an interrupt to the microprocessor (INT or $\overline{INT}$).

- Reading the conversion result

  With a read instruction the result is read from the ADC_CS address.

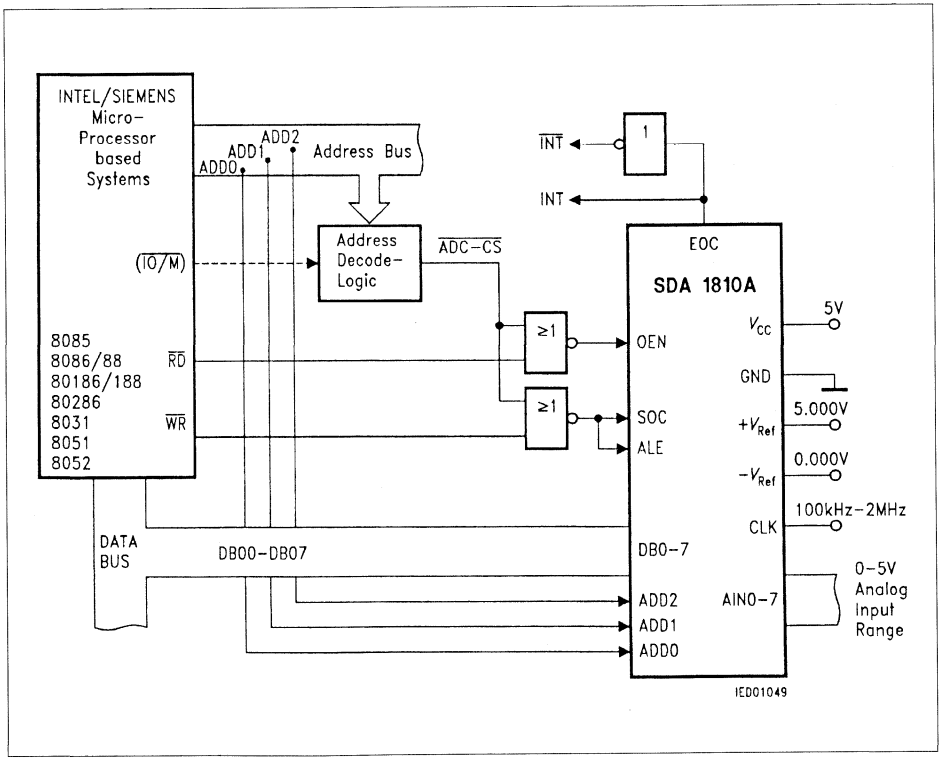


Figure 7
Microprocessor Interfacing

Motorola Microprocessors

A typical interface is shown in **figure 8**.

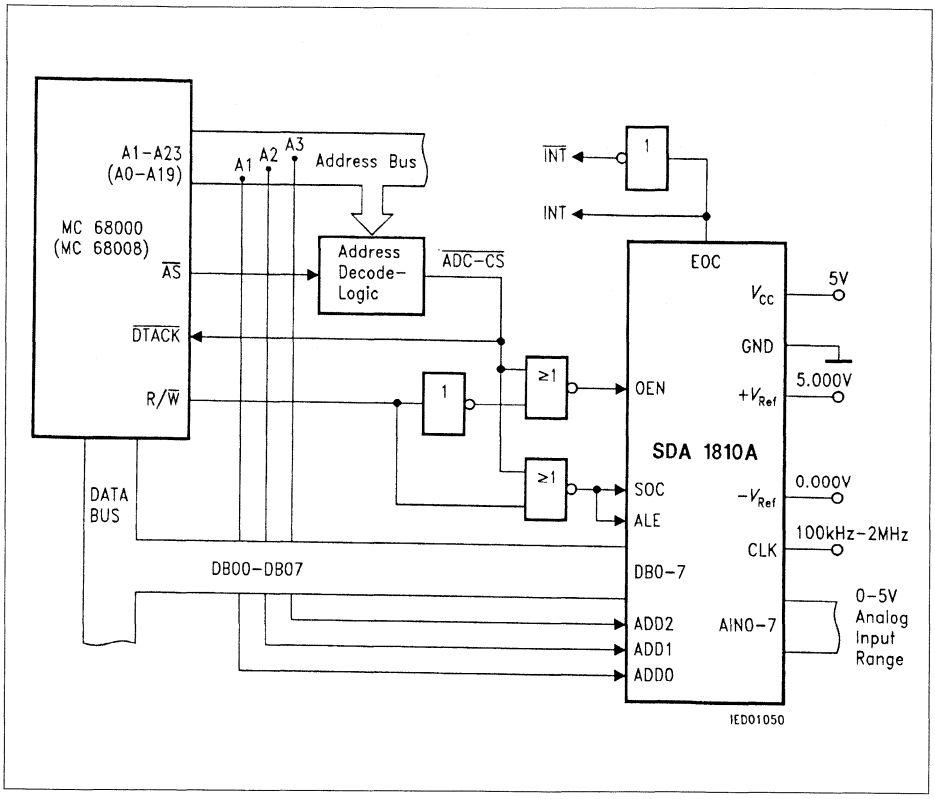


Figure 8
Microprocessor Interfacing

Application

Power Supply Decoupling

The power supply of the SDA 1810 A should be connected with a 10 µF tantalum or an electrolytic capacitor. To insure good high frequency performance, this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins $+V_{REF}$ and $-V_{REF}$. Also an 0.1 µF ceramic capacitor should be placed between pins $-V_{REF}$ and GND.

Analog Input

The high input impedance of the analog channels AIN0-AIN7 allows simple analog interfacing. Signal sources ($-V_{REF} \leq$ AIN $\leq +V_{REF}$) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 30 pF, within 5-clock cycles.

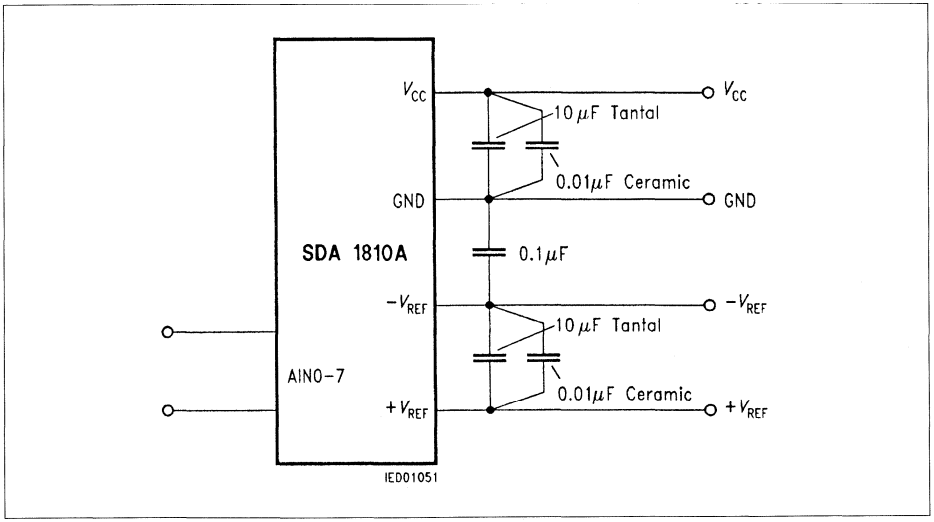


Figure 9
Capacitors

SIEMENS

12-Bit A/D Converter with 4-Channel Multiplexer

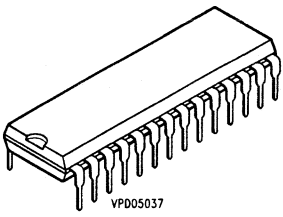
SDA 0812 A
SDA 1812 D

Preliminary Data

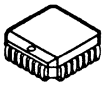
CMOS

Features

- 12-bit resolution
- Autocalibration circuitry
- No offset or gain adjustments required
- Total unadjusted error ± 1/2 LSB max. (SDA 0812 A) respectively ± 3/4 LSB max. (SDA 1812 D)
- Fast conversion time (6 µs)
- SDA 1812 D with over 100 kHz sampling rate
- No missing codes
- *S/N + THD* together 71 dB typ
- Single 5 V supply
- 4-channel multiplexer with latched control logic
- Easy interfacing to 8- and 16-bit microprocessors
- Data output in a 2-byte format
- 0 V to 5 V analog input voltage range
- Digital inputs and outputs are TTL compatible
- Standby mode (50 µW typ)
- CMOS low power consumption (10 mW typ)
- Temperature range – 40 to 85 °C



P-DIP-28



P-LCC-28-2

	Type	Ordering Code	Package
S	SDA 0812 A	Q67100-A8233	P-DIP-28
	SDA 0812 AN	Q67100-H8300	P-LCC-28-2 (SMD)
S	SDA 1812 D	Q67100-H8291	P-DIP-28
	SDA 1812 DN	Q67100-H8301	P-LCC-28-2 (SMD)

General Description

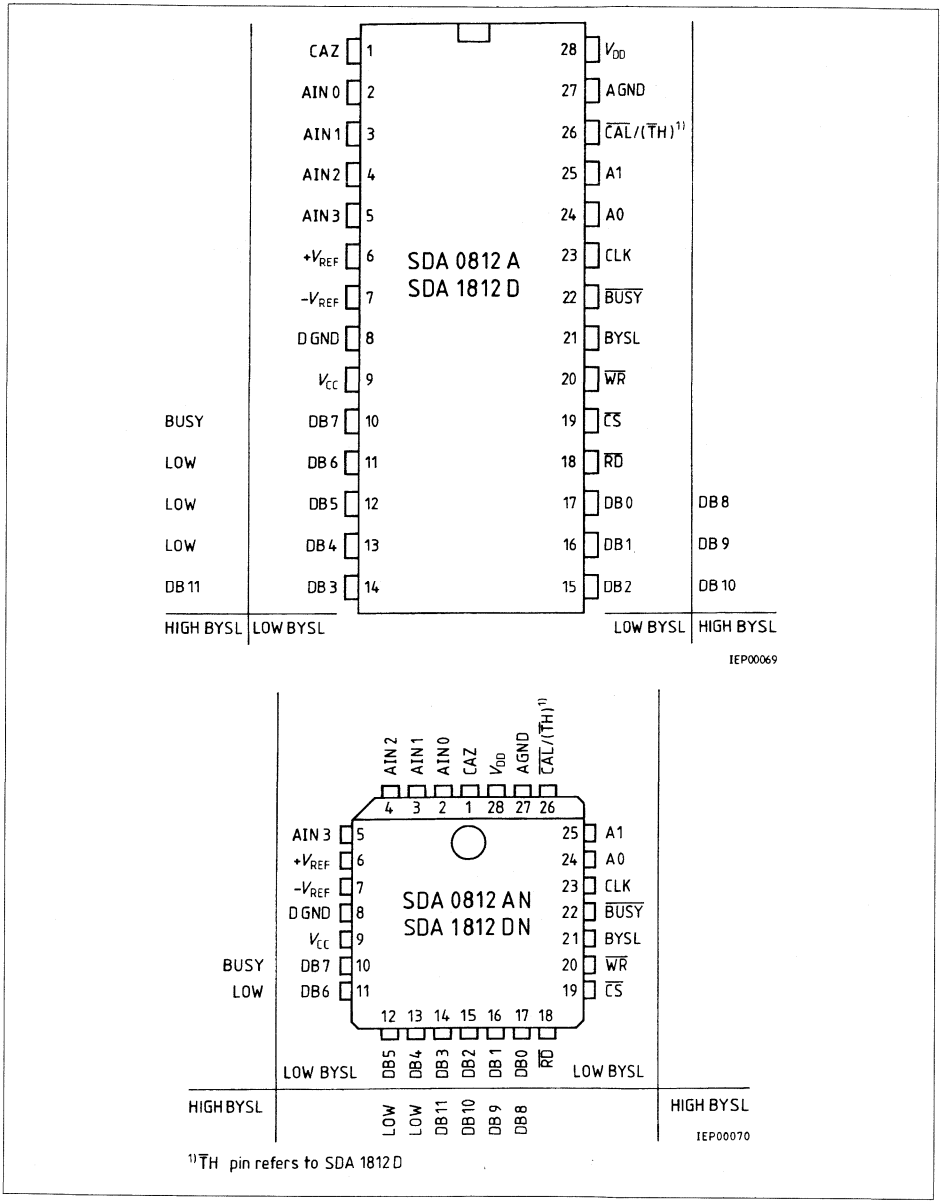
SDA 0812 A and SDA 1812 D are monolithic CMOS 12-bit analog to digital converters with a 4-channel analog multiplexer. They need only a 5 V supply and achieve a conversion time of 6 µs plus 2.5 µs sample time.

They use the method of successive approximation based on a capacitor network. **An autocalibration circuit guarantees a total unadjusted error within ± 1/2 LSB max. (SDA 0812 A) respectively ± 1/2 LSB typ. (SDA 1812 D).** Therefore the device needs no external offset or gain adjustments. The converters feature a temperature stabilized differential comparator, a sample and hold function and a 12-bit data output in a 2-byte format. Designed for easy microprocessor interface using the standard control signals $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ the 4-channel input multiplexer is controlled via address inputs A0 and A1.

Two converter busy flags are available to facilitate polling of the converter's status.

With a sample and hold circuit on chip, the SDA 1812 D is suited for digitizing AC signals as well as DC signals. The maximum sampling rate of the SDA 1812 D is more than 100 kHz according to 2.5 µs sample time plus 6 µs conversion time. The SDA 1812 D is specified with traditional static specifications as well as with dynamic specifications (SNR, THD, effective number of bits).

The temperature range of the SDA 0812 A/1812 D is – 40 °C to 85 °C.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	CAZ	Special function pin (see Reading the Conversion Results, SFR and Internal Clock Operation). Connect to a MP address pin. If not used, CAZ can be connected to AGND or DGND or can be unconnected.
2-5	AIN 0 to AIN 3	**Analog Input,** channel 0 to channel 3
6	+ V_{REF}	Pos. voltage reference input, + V_{REF} = 5 V
7	– V_{REF}	Neg. voltage reference input, – V_{REF} = 0 V
8	DGND	**Digital Ground,** DGND = 0 V
9	V_{CC}	Logic supply voltage, V_{CC} = 5 V must not be applied before V_{DD}!
10-17	DB7-DB0	Three-state data outputs. **Data Bus** output ($\overline{CS}$, $\overline{RD}$ = LOW)
	Symbol (BYSL = HIGH)	Symbol (BYSL = LOW)
10	BUSY	DB7 BUSY is an active high converter status flag. It is high
11	LOW	DB6 during a conversion and during autocalibration.
12	LOW	DB5 LOW Pin 11 to pin 13 are tied to DGND when
13	LOW	DB4 BYSL = HIGH
14	DB11 (MSB)	DB3 DB11 is the MSB.
15	DB10	DB2
16	DB9	DB1
17	DB8	DB0 (LSB) DB0 is the LSB.
18	$\overline{RD}$	Read input, active low, is used to read the data outputs in combination with $\overline{CS}$ and BYSL.
19	$\overline{CS}$	**Chip Select** input, active low.
20	$\overline{WR}$	**Write** input, active low, is used to start a new conversion and to select an analog channel via address inputs A0, A1 in combination with $\overline{CS}$ low. The minimum $\overline{WR}$ pulse width is 100 ns. It is independent of internal/external clock operation.
21	BYSL	**Byte Select** input, is used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.

Pin Definitions and Functions (cont'd)

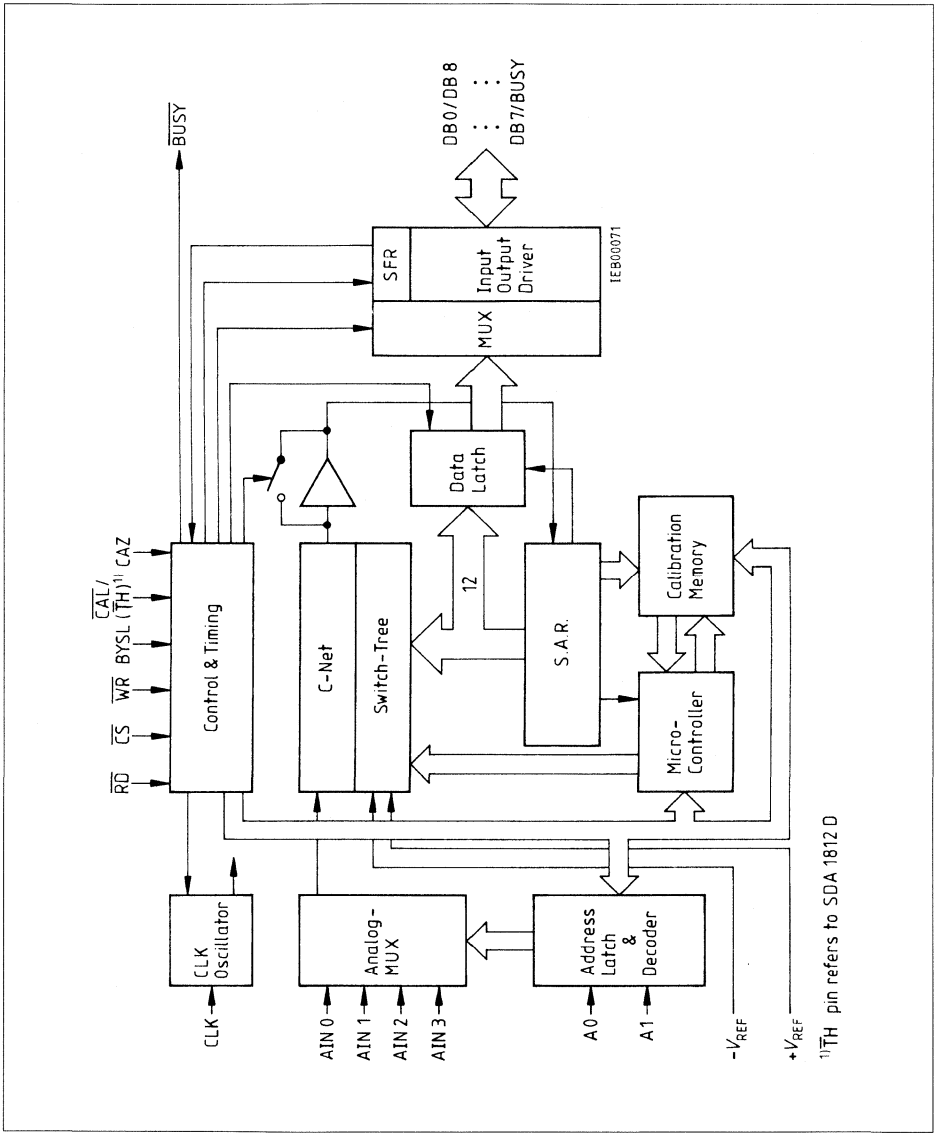
Pin	Symbol	Function
22	$\overline{\text{BUSY}}$	Converter status output. $\overline{\text{BUSY}}$ is low during conversion or autocalibration. $\overline{\text{BUSY}}$ is high after the converter has finished its operation.
23	CLK	**Clock** input for internal/external clock operation. For external clock operation connect pin 23 to a 74HC compatible clock source. For internal clock operation connect pin 23 to a R timing component (see Clock Operation description).
24-25	A0 to A1	**Address** inputs, are used to select one of four analog input channels, in combination with $\overline{\text{CS}}$ and $\overline{\text{WR}}$. The address inputs are latched with the rising edge of $\overline{\text{WR}}$.

A1	A0	Selected Channel
LOW	LOW	AIN0
LOW	HIGH	AIN1
HIGH	LOW	AIN2
HIGH	HIGH	AIN3

26	$\overline{\text{CAL}}$/$\overline{\text{TH}}$[1]	**Calibration** input. An autocalibration cycle is initiated with $\overline{\text{CAL}}$ = LOW. If not used, $\overline{\text{CAL}}$ can be connected to V_{CC} or unconnected. In this case autocalibration is only initiated by power-up/power-fail, or by SFR. The minimum pulse width of CAL is 100 ns. Using the SDA 1812 D, via SFR the function of pin 26 can be defined as an external Track-Hold ($\overline{\text{TH}}$) pin (see SFR description).
27	AGND	**Analog Ground,** AGND = 0 V
28	V_{DD}	Analog supply, V_{DD} = 5 V, must not be applied after V_{CC}!

7

[1] $\overline{\text{TH}}$-pin refers to SDA 1812 D



Block Diagram

Functional Description

SDA 0812 A and 1812 D are 4-channel 12-bit A/D converters. The successive approximation technique provides 6 µs conversion time. The required sampling time of the on-chip sample-and-hold-circuit is 2.5 µs. An autocalibration technique guarantees a total unadjusted error within ± 1/2 LSB max. (SDA 0812 A) and ± 3/4 LSB max. (SDA 1812 D) over the entire temperature range. The major components are shown in the **block diagram.**

The comparator is a fully differential autozeroed one for a high power supply rejection ratio and very low offset voltages. The charge redistribution design using a binary weighted capacitor network inherents the sampling function to convert AC-signals (SDA 1812 D). A Sub-C Network is used to correct linearity-errors in the Main-Capacitor Network. The correction terms are calculated by a microcontroller in an autocalibration cycle, started by power-up or $\overline{CAL}$ signal. The correction terms are stored in a calibration memory. The stability of integrated C-Networks guarantees the correction terms to be valid over time and temperature. In the case of a power up/power fail (V_{CC} less then 3 V typical) new calibration cycles will be initiated automatically. This guarantees the integrity of the correction terms.

Three-state output drivers with multiplexer for 2-byte data format, an analog multiplexer with address latch and a clock oscillator with external or internal clock operation complete the functional components of the device.

7

A/D Converter Timing

SDA 0812 A

After a conversion has been started with the rising edge of $\overline{WR}$ the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time. In parallel an offset compensation mechanism reduces the comparators offset error below 1/4 LSB. During this period the converter is susceptable to spikes and noise at the analog input, which may cause erroneous codes at the digital outputs. Therefore RC-filtering at the analog inputs is recommended.

Conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle. The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin. (See Special Function Register).

SDA 1812 D

After a conversion has been started with the rising edge of $\overline{WR}$ the analog input voltage is sampled for 5 clock cycles. The analog source must be capable to charge the capacitor network of appr. 50 pF to full accuracy in this time.

By starting a conversion with $\overline{WR}$ sampling of the analog signal is defined by the first rising edge of the internal CLK pulse + 4.5 clock cycles + 100 ns (typ) after the rising edge of $\overline{WR}$. For precisely defined sampling point $\overline{WR}$ has to be synchronized with CLK. The conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle.

To avoid synchronizing problems between $\overline{WR}$ and CLK the $\overline{CAL}$ pin is programmable into an external Track-Hold pin ($\overline{TH}$) via SFR. A low to high transition at this pin defines the sampling point of the ADC with a delay time of 5 ns typ. without synchronizing to CLK. The low pulse width of $\overline{TH}$ defines the tracking period of internal sample and hold circuit

and should be 2.5 µs min. Using this $\overline{TH}$ pin an additional offset error of ± 1 LSB may occure. This $\overline{TH}$ pin should be used in combination with on chip clock generator. Using external clock generator in combination with asynchronous $\overline{TH}$ function brings offset errors up to ± 4 LSB via pin coupling effects. By synchronizing the $\overline{TH}$ signal with external CLK this offset error can be reduced again to ± 1 LSB. The best conditions are given by delaying the falling clock slope 20 ns to the rising edge of $\overline{TH}$.

The SDA 1812 D operates with the master clock. The conversion cycle may not begin until up to 1.5 clock cycles after $\overline{TH}$ goes high.

The CAZ pin is not used for normal operation. However CAZ serves as an additional programming pin (see Special Function Register).

Autocalibration

An autocalibration cycle is started

– with the rising edge of a $\overline{CAL}$ low pulse

– by setting the DB1 in the Special Function Register (SFR)

– by power-up/power-fail

and takes 168 clock cycles. Finally a normal conversion (17 clock cycles) is added automatically. During an autocalibration or conversion cycle each power supply voltage and each reference voltage has to be stable. Therefore an internal timer provides a waiting period of 42 240 clock cycles between power up/power fail and autocalibration function. Power up calibration is finished after 42425 (42240 + 168 + 17) clock cycles.

Reading the Conversion Results

Normal Mode (Transparent)

The data is read as two 8-bit bytes. The converters digital outputs are positive true. Data is presented in right justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the BYSL input determines which byte is to be read. Because the conversion results are held in a successive approximation register the high byte may be read out before the conversion is finished.

The 4 most significant bits are valid in the 10^{th} clock cycle after starting a conversion with $\overline{WR}$. Valid 12-bit data are available for reading after the $\overline{BUSY}$ pin has gone high, or internal status flag $\overline{BUSY}$ (available on pin 10) has gone low.

Latched Output Mode

An additional function is reading the data is available via an integrated data latch, which is transparent in normal function mode.

The latched output function may be activated by writing high on DB0 and low on DB7 (see Special Function Register SFR) with $\overline{WR}$, $\overline{CS}$ active in combination with CAZ and BYSL pin high.

The data latch is set transparent by power-up.

When the latch function is active an internal generated latch enable signal shifts the data from the SAR into a 12-bit latch. This occures when $\overline{BUSY}$ gets inactive (high). The conversion result is valid during the next conversion cycle until new data is latched. Therefore it may be read out even after starting a new conversion.

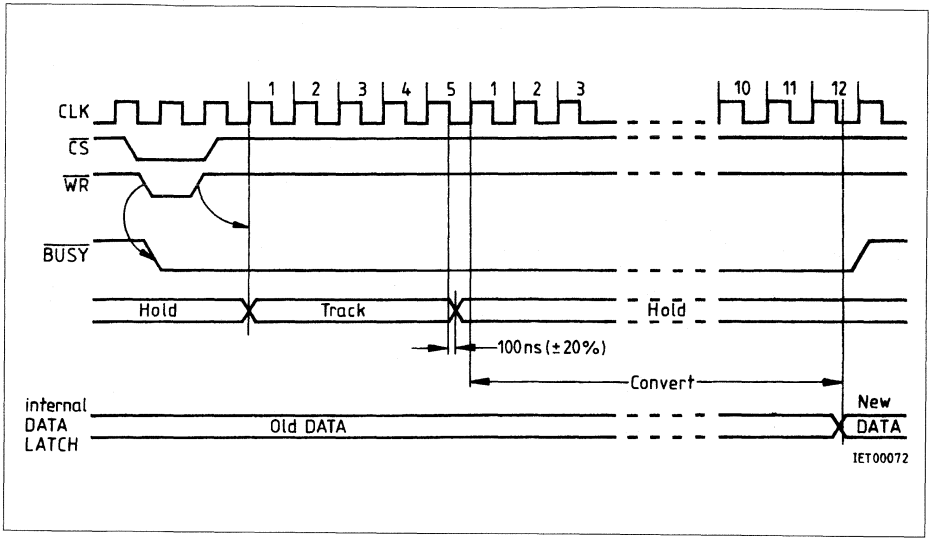


Figure 1
Starting a Conversion with $\overline{WR}$

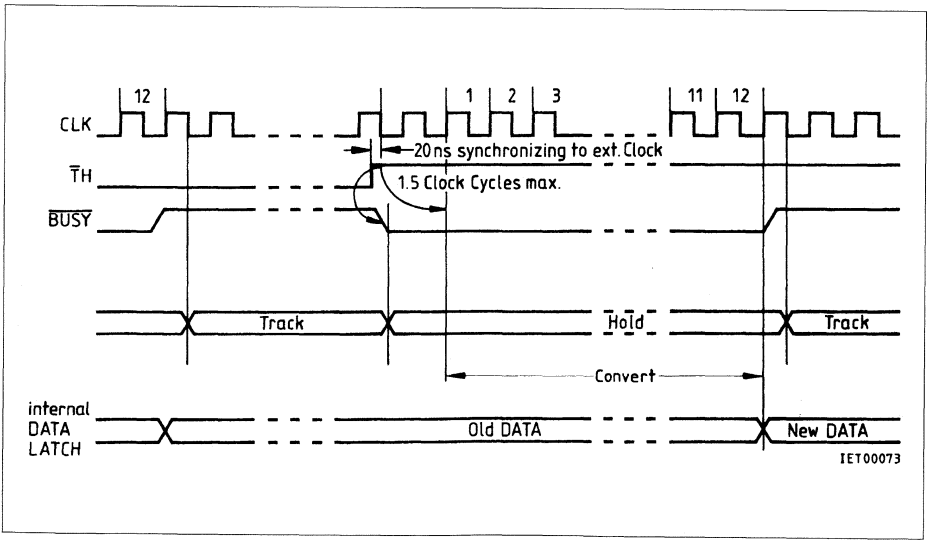


Figure 2
Starting a Conversion with $\overline{TH}$ (SDA 1812 D)
may be synchronous with internal clock generator and should be synchronized with external clock for best performance.

The Special Function Register (SFR)

An internal register for additional functions programmed by the microprocessor is available.

Special Functions

SDA 0812 A

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-$\overline{\text{CAL}}$ starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-$\overline{\text{CAL}}$ function (168 + 17 clock cycles).
- The converter is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduced to 50 µW typ. Wake up the converter by writing low to DB3, ext. $\overline{\text{CAL}}$, INT-$\overline{\text{CAL}}$ (DB1) or power-up function (V_{CC} < 3 V). Applying $\overline{\text{CS}}$ and $\overline{\text{WR}}$ (start of conversion) during standby mode (DB3 high) delivers one correct conversion result, subsequently the converter goes back to standby mode until new conversion start or wake-up signal.
- POWER FAIL FLAG is set if a power fail occured, showing that a new calibration was started ($\overline{\text{BUSY}}$ active) and that the data of SFR (data latch enable) are lost. To reset this flag write low to DB5.
- CAL-ERROR flag is set on DB6 if a calibration overflow occurs (may be in very noisy systems). It is reset by starting a calibration and remains low after a properly finished calibration.
- $\overline{\text{BUSY}}$ flag is high (DB7) if a calibration or a conversion is in process.

SDA 1812 D

- 12-bit data latch is enabled by setting SFR DB0 high.
- INT-$\overline{\text{CAL}}$ starts a calibration by setting SFR DB1 high, the timing of this calibration refers to EXT-$\overline{\text{CAL}}$ function (168 + 17 clock cycles).
- The $\overline{\text{CAL}}$ pin function is modified to an ext. Track-Hold ($\overline{\text{TH}}$) function by setting DB2 high. Reset the function to $\overline{\text{CAL}}$ by writing low into DB2. The ext. Track-Hold pin ($\overline{\text{TH}}$) guarantees sampling points precisely defined by the rising edge of $\overline{\text{TH}}$ signal. The internal sampling point is delayed 5 ns typ. to the external $\overline{\text{TH}}$ slope.
- The SDA 1812 D is set to a standby mode by programming DB3 high. In this mode the analog circuit and the internal CLK-generator are deactivated, total power consumption reduces to 50 µW typ. Wake up the SDA 1812 with writing low to DB3, EXT-$\overline{\text{CAL}}$, INT-$\overline{\text{CAL}}$ (DB1) or power-up function (V_{CC} > 3 V). Applying $\overline{\text{WR}}$ and $\overline{\text{CS}}$ or a rising edge on $\overline{\text{TH}}$ pin (Conversion Start) during standby mode (DB3 high) delivers one correct conversion result, subsequently the SDA 1812 D goes back to standby mode until new SOC or WAKE UP signal.
- POWER FAIL FLAG is set if power fail occured (DB5), showing that a new calibration has been started ($\overline{\text{BUSY}}$ active) and that the data of SFR (data latch enable $\overline{\text{CAL}}$/$\overline{\text{TH}}$ pin programming) are lost. To reset this flag write low to DB5.
- $\overline{\text{CAL}}$-ERROR flag is set on DB6 if a calibration overflow occures (may be in very noisy systems), is reset by starting a calibration and remains low after a properly finished calibration.
- $\overline{\text{BUSY}}$ FLAG is high (DB7) if a calibration or a conversion is in process.

Note that all programmable bits of the SFR are reset to low by power-up.

Writing the SFR (SDA 0812 A/1812 D, see figure 9)

The SFR is activated by pulling CAZ and BYSL pins high and loading a data word with a general low on DB7 by a microprocessor WRITE cycle.

other DB	DB7	DB5	DB3	DB2*)	DB1	DB0	$\overline{CS}$/ $\overline{WR}$	CAZ/ BYSL	Function
reserved	LOW	LOW					active	HIGH	Reset of POWER FAIL FLAG
reserved	LOW	HIGH					active	HIGH	Set POWER FAIL FLAG (not locked)
reserved	LOW		LOW				active	HIGH	Wake-up from STANDBY
reserved	LOW		HIGH				active	HIGH	STANDBY mode active
reserved	LOW			LOW			active	HIGH	$\overline{CAL}$ function on pin 26
reserved	LOW			HIGH			active	HIGH	$\overline{TH}$ function on pin 26
reserved	LOW				LOW		active	HIGH	–
reserved	LOW				HIGH		active	HIGH	INT-$\overline{CAL}$ is initiated
reserved	LOW					LOW	active	HIGH	Output data latch transparent
reserved	LOW					HIGH	active	HIGH	Output data latch enabled

Reading the SFR (SDA 0812 A; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Function
DB0	DATA LATCH State: HIGH enabled, LOW transparent
DB1	CAL FLAG: HIGH during calibration
DB2	RESERVED
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Warning: Reading on CAZ high and BYSL low is prevented for factory use, unpredictable data may appear on the data bus.

*) Refers to SDA 1812 D

Reading the SFR (SDA 1812 D; see figure 10)

The contents of SFR are put to the DATA BUS by a microprocessor READ cycle in combination with BYSL and CAZ high.

Data Bus Pin	Definition
DB0	DATA LATCH State: HIGH enabled, LOW transparent
DB1	$\overline{\text{CAL}}$ FLAG: HIGH during calibration
DB2	$\overline{\text{CAL}}$/$\overline{\text{T}}$H: HIGH for $\overline{\text{T}}$H, LOW for $\overline{\text{CAL}}$ function
DB3	HIGH if STANDBY mode is active
DB4	RESERVED
DB5	POWER FAIL FLAG: HIGH if power fail occured
DB6	CAL ERROR FLAG: HIGH if calibration overflow occured
DB7	BUSY FLAG: HIGH during calibration or conversion

Reading on CAZ high and BYSL low is reserved for factory use only, unpredictable data may appear on the data bus.

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 3**.

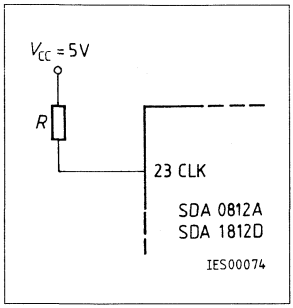
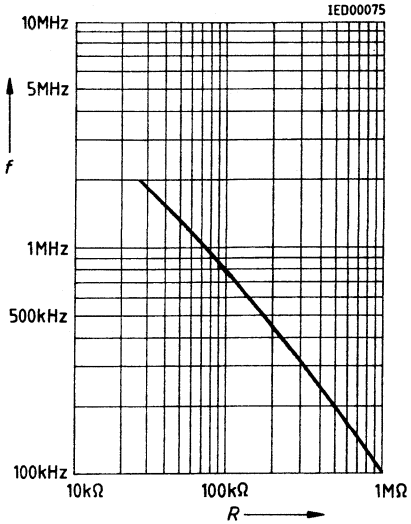


Figure 3
The Internal Clock Frequency only depends on the *R* Value

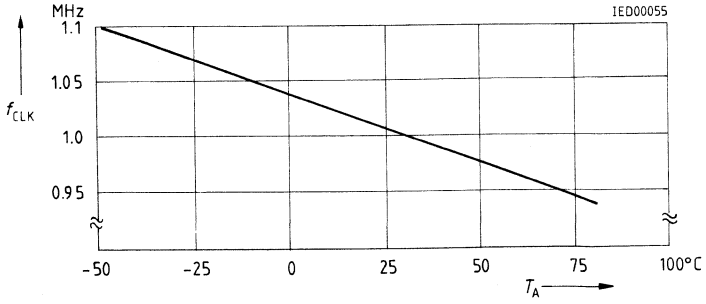
Figure 4
Clock Frequency of Internal Clock Generator versus External Resistor Value



The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.0 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device. Therefore for precisely defined conversion times usage of an external clock generator is recommended.

Figure 5
Typical Internal Clock Frequency versus Temperature



External Clock Operation

The required circuitry for external clock operation is shown in **figure 6**.

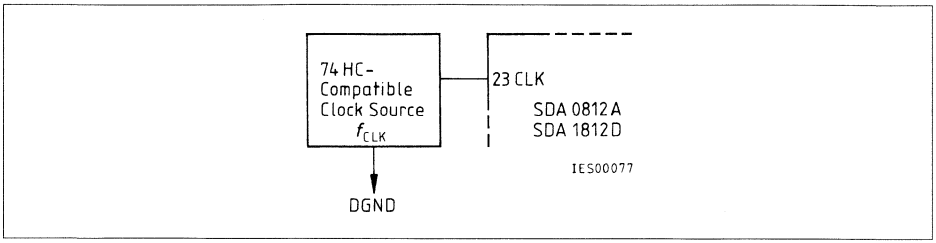


Figure 6

The external clock source has to provide 0.8 Vmax for low voltage level and 3.5 Vmin for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. $\overline{TH}$ signal. Synchronizing should be provided for optimal performance, see A/D converter timing on page 9. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.2 MHz.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Units
		min.	max.	
Supply voltages[1)]	V_{CC}, V_{DD}		6.5	V
Input voltage range (all inputs)	V_I	– 0.3	V_{CC} + 0.3	V
Package dissipation (at or below 25 °C free-air temperature range)			875	mW
Ambient temperature	T_A	– 40	85	°C
Storage temperature	T_{stg}	– 65	125	°C

Note:

1) All voltage values are with respect to network ground terminal

Characteristics (SDA 0812 A)

V_{CC} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Accuracy						
Resolution		12			Bit	No missing codes guaranteed
Total unadjusted error[1]	*TUE*			+/– 1/2	LSB	All channels, AIN0-AIN3
Differential nonlinearity	*DNL*			+/– 1/2	LSB	
Full scale error (gain error)	*GE*			+/– 1/4	LSB	All channels, AIN0-AIN3
Offset error	*OFS*			+/– 1/4	LSB	All channels, AIN0-AIN3
Channel to channel mismatch				+/– 1/4	LSB	
Analog Inputs						
Analog input range	V_{AIN}	$-V_{REF}$		V_{REF}	V	
Slew rate[2]	*SR*			8	mV/µs	
Multiplexer						
Settling time			20		ns	Switch delay after
ON-resistance	R_{ON}		2		kΩ	programming
OFF-resistance	R_{OFF}		10		MΩ	the input channel
On channel input capacitance	C_{AIN}		50		pF	
Input leakage current						
at 25 °C	I_{AIN}			10	nA	AIN0-AIN3
at t_{min} to t_{max}	I_{AIN}			100	nA	
On-state bias current			+/– 5		µA	Depends on analog input voltage
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75	5	V_{DD}	V	For specified
Negative reference voltage	$-V_{REF}$		0		V	performance
Input reference current	I_{REF}		10	100	µA	
Power supply rejection	V_{DD}		± 1/8		LSB	V_{REF} = 4.75 V to 5.25 V
Logic Inputs						
CAZ (pin 1), $\overline{RD}$ (pin 18), $\overline{CS}$ (pin 19), $\overline{WR}$ (pin 20), BYSL (pin 21), A0 (pin 24), A1 (pin 25), $\overline{CAL}$ (pin 26)						
L-input voltage	V_{IL}	2.4		0.8	V	
H-input voltage	V_{IH}				V	

Notes see next page

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Logic Inputs						
Input current						
at 25 °C	I_{IN}	– 1		1	µA	V_{IN} = 0 V to V_{CC}
at – 40 °C ... 85 °C	I_{IN}	– 10		10	µA	
CLK (pin 23)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	3.5			V	
L-input current	I_{IL}	– 10		10	µA	
H-input current	I_{IH}			1.5	mA	100 nA max. during standby
Logic Outputs						
DB0 to DB7 (pins 10 to 17), $\overline{BUSY}$ (pin 22)						
L-output voltage	V_{QL}			0.4	V	I_{SINK} = 1.6 mA
H-output voltage	V_{QH}	4.0			V	I_{SQURCE} = 200 µA
Floating state leakage current (pins 10-17)		– 1		1	µA	V_{OUT} = 0 V to V_{CC}
Floating state output capacitance	C_Q			15	pF	
Conversion Time						
With external clock						
	t			24	µs	f_{CLK} = 500 kHz
	t	6			µs	f_{CLK} = 2 MHz
with internal clock	t	7.5			µs	Using recommended clock
(T_A = 25 °C)	t			38	µs	components as shown in **fig. 4**. See internal clock operation
sampling time	t	2.5			µs	

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity.

2) Input signals with specified slew rates can be converted without external sample-and-hold. Input signals with higher slew rates may cause digital full scale errors. Filtering by a low pass (R = 2 kΩ, C = 100 nF) or use of an external sample-and-hold is required then.

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Functional Range						
Supply voltage	V_{DD}		5		V	± 5 % for specified performance
	V_{CC}		5		V	± 5 % for specified performance
Supply current	I_{DD}			2.5	mA	Typ. 1 mA with V_{DD} = 5 V
	I_{CC}		1.0	2.0	mA	V_{IN} = V_{IL} = or V_{IH}
Power dissipation	P_D		10	25	mW	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = HIGH
Power dissipation (standby mode)	P_{DSB}		50		µW	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = HIGH

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Characteristics (SDA 1812 D)

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, $-V_{REF}$ = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
DC Accuracy						
Resolution		12			Bits	No missing codes guaranteed
Total unadjusted error[1]	*TUE*		± 1/2	± 3/4	LSB	All channels, AIN0-AIN3
Differential nonlinearity	*DNL*		± 1/4	± 1/2	LSB	
Full scale error (gain error)	*GE*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error	*OFS*		± 1/8	± 1/4	LSB	All channels, AIN0-AIN3
Offset error with T/H function			± 1/2	± 1	LSB	with internal clock generator or synchronizing T/H to ext. CLK
Channel to channel mismatch				± 1/4	LSB	
Dynamic Performance[2) 3)]						
Signal to noise ratio	*SNR*	69	71		dB	Full scale input sinwave, 1 kHz f sampling is 100 kHz
		66	69		dB	Full scale input sinwave, 50 kHz f sampling is 100 kHz
Total harmonic distortion	*THD*		75		dB	Full scale input sinwave, 50 kHz f sampling is 100 kHz
Full power bandwidth (– 3 dB)	*BW*		4		MHz	
Aperture delay time			5		ns	T/H pin
Analog Inputs						
Analog input range Multiplexer	*AIN*	$-V_{REF}$		$+V_{REF}$	V	Selected and unselected channels AIN0-AIN3;
Settling time			10		ns	
On channel input Capacitance	C_{AIN}		50		pF	
ON-resistance	R_{ON}		2		kΩ	
OFF-resistance	R_{OFF}		10		MΩ	
Input leakage current						
+ 25 °C	I_{AIN}			10	nA	
t_{min} to t_{max}	I_{AIN}			100	nA	
On-state bias current			± 5		µA	Depends on analog input voltage

Notes see next page

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reference Inputs						
Positive reference voltage	$+V_{REF}$	4.75		V_{DD}	V	(For specified performance)
Negative reference voltage	$-V_{REF}$	0			V	(For specified performance)
Input reference current	I_{REF}			100	µA	$+V_{REF}$ = 5.0 V
Power Supply Rejection						
Supply voltage	V_{DD}		±1/8		LSB	V_{DD} = 4.75 V to 5.25 V
Logic Inputs						
CAZ (pin 1) $\overline{RD}$ (pin 18), $\overline{CS}$ (pin 19), $\overline{WR}$ (pin 20) BYSL (pin 21), A0 (pin 24), A1 (pin 25) $\overline{CAL}$ (pin 26)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	2.4			V	
Input current						
+ 25 °C	I_{IN}	− 1		1	µA	V_{IN} = 0 V to V_{CC}
T_{min} to T_{max}	I_{IN}	− 10		10	µA	
CLK (pin 23)						
L-input voltage	V_{IL}			0.8	V	
H-input voltage	V_{IH}	3.5			V	
L-input current	I_{IL}	− 10		10	µA	
H-input current	I_{IH}			1.5	mA	100 nA max. during standby
Logic Outputs						
DB0-DB7 (pins 10-17), $\overline{BUSY}$ (pin 22)						
L-output voltage	V_{OL}			0.4	V	I_{SINK} = 1.6 mA
H-output voltage	V_{OH}	4.0			V	I_{SOURCE} = 200 µA
Floating state leakage current (Pins 10-17)		− 1		1	µA	
Floating state output Capacitance	C_Q			15	pF	V_{OUT} = 0 V to V_{CC}

Notes

1) Includes full scale error, offset error, integral and differential nonlinearity.
2) *S/N* includes harmonic distortion
3) Sample tested at 25 °C

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Conversion Time						
With external clock	t_{ext}	6			µs	f_{CLK} = 2 MHz symmetrically
				24	µs	f_{CLK} = 500 kHz
With internal clock	t_{int}		6		µs	Using recommended clock components as shown in **figure 4**. See internal clock
Sampling time [1]	t_s	2.5			µs	operation
Power Requirements						
Analog supply voltage	V_{DD}	4.75	5	5.25	V	
Logic supply voltage	V_{CC}	4.75	5	5.25	V	
Analog supply current	I_{DD}		0.75	2.5	mA	V_{DD} = 5 V
Logic supply current	I_{CC}		1.0	2.0	mA	$V_{IN} = V_{IL}$ or V_{IH}
Power dissipation	P_D		10	25	mW	$\overline{WR} = \overline{RD} = \overline{CS} = \overline{BUSY}$ =
Power dissipation (standby)	P_{DS}		50		µW	Logic HIGH

Note:

[1] Ensures the analog input source to load 50pF during sampling time to required accuracy.

Timing Specifications[1]

V_{DD} = 5 V ± 5 %, V_{CC} = 5 V ± 5 %, $V_{REF} \leq V_{DD} \geq V_{CC}$, – V_{REF} = 0 V, DGND = 0 V, AGND = 0 V
f_{CLK} = 2 MHz, all specifications t_{min} to t_{max} unless otherwise specified.

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Min. TH LOW pulse width (SDA 1812 D)	t_{THL}	2.5			µs
AMUX-settling time after programming the input channel	t_{AMUX}		20		ns
$\overline{CS}$ to $\overline{WR}$ setup time	t_1[2]	0			ns
$\overline{WR}$ pulse width	t_2[2]	100			ns
$\overline{CS}$ to $\overline{WR}$ hold time	t_3[2]	0			ns
$\overline{WR}$ to $\overline{BUSY}$ propagation delay	t_4	20	50	150	ns
BYSL, CAZ valid to $\overline{WR}$ setup time	t_5	100			ns
BYSL, CAZ valid to $\overline{WR}$ hold time	t_6	20			ns
$\overline{BUSY}$ to $\overline{CS}$ setup time	t_7	0			ns
CS to $\overline{RD}$ setup time	t_8[2]	0			ns
$\overline{RD}$ pulse width	t_9[2]	100			ns
$\overline{CS}$ to $\overline{RD}$ hold time	t_{10}[2]	0			ns
BYSL, CAZ to $\overline{RD}$ setup time	t_{11}	50			ns
BYSL, CAZ to $\overline{RD}$ hold time	t_{12}	0			ns
$\overline{RD}$ to valid data					
Bus Access Time (100 pF Load)	t_{13}[3]		80	150	ns
Bus Access Time (50 pF Load)	t_{13}[3]		40	75	ns
$\overline{RD}$ to three-state output	t_{14}[4]	20		60	ns
Bus relinquish time	t_{15}[5]		90	180	ns
Data valid to $\overline{WR}$ setup time	t_{16}	100			ns
Data valid to $\overline{WR}$ hold time	t_{17}	20			ns

Notes:

1) All input control signals are specified with $t_r = t_f$ = 20 ns (10 % to 90 % of 5 V) and timed from a voltage level of 1.6 V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}/\overline{RD}$. The internal WR pulse is performed by a NOR wiring of $\overline{CS}/\overline{WR}$.
3) t_{13} is measured with the load circuits of **figure 11** and defined as the time required for an output to cross 0.8 V or 2.4 V.
4) t_{14} is defined as the time required for the data lines to change three-state, **see figure 11.**
5) t_{15} is defined as the time required for the data lines to change 10 %/90 % when loaded with the circuits of **figure 11.**

7

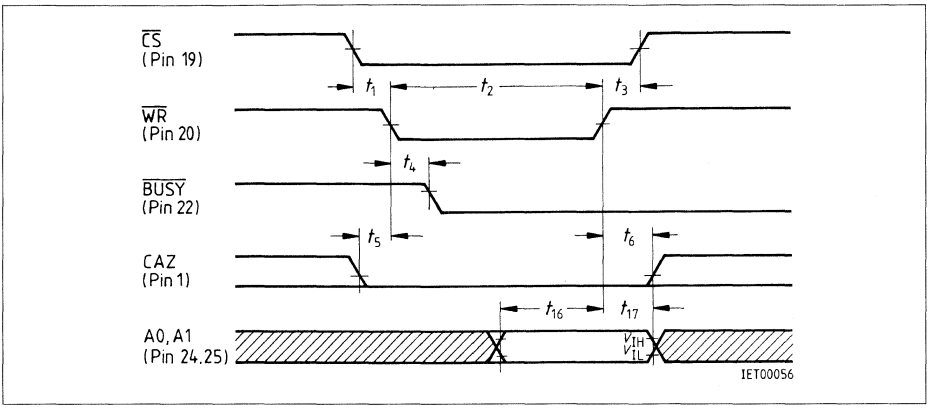


Figure 7
Red Cycle Timing

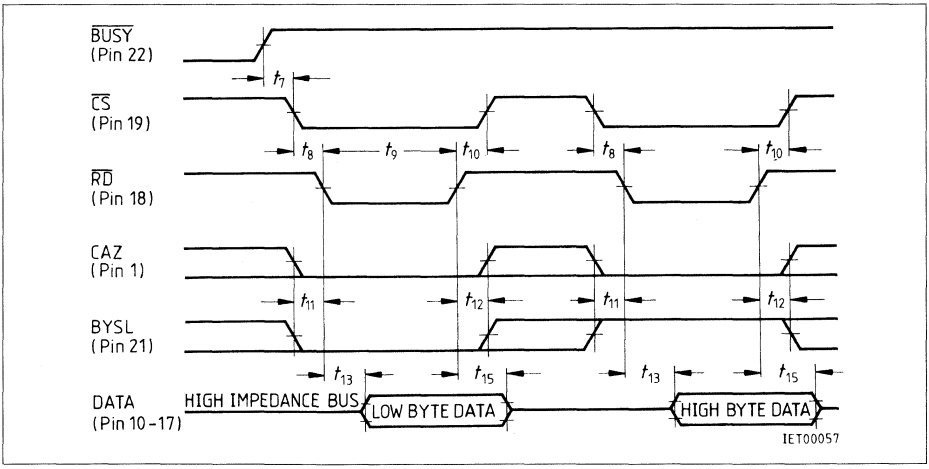


Figure 8
Red Cycle Timing

Notes

The 2-byte conversion result can be read in either order. The figure shows the sequence low byte to high byte. If BYSL changes while $\overline{CS}$ and $\overline{RD}$ are low the data will change to reflect the BYSL input.

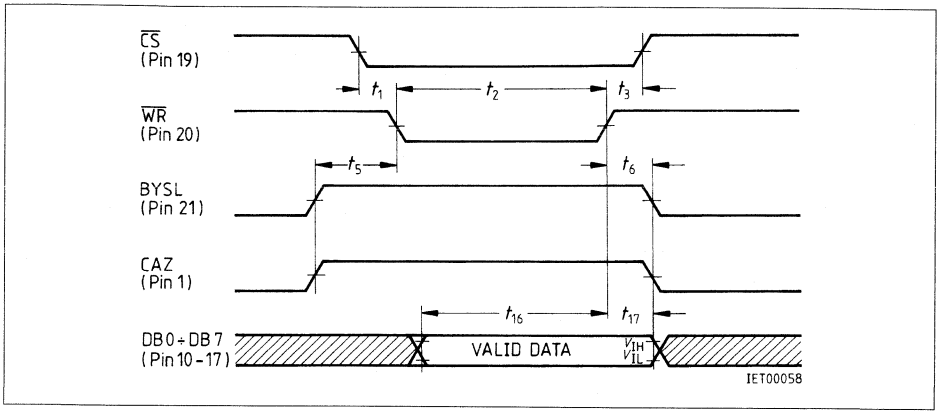


Figure 9
Writing to the SFR

7

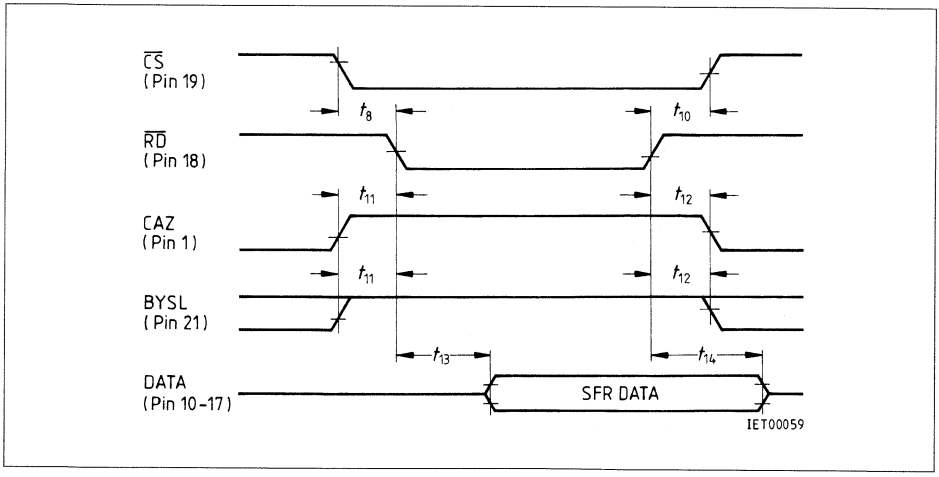


Figure 10
Reading the SFR

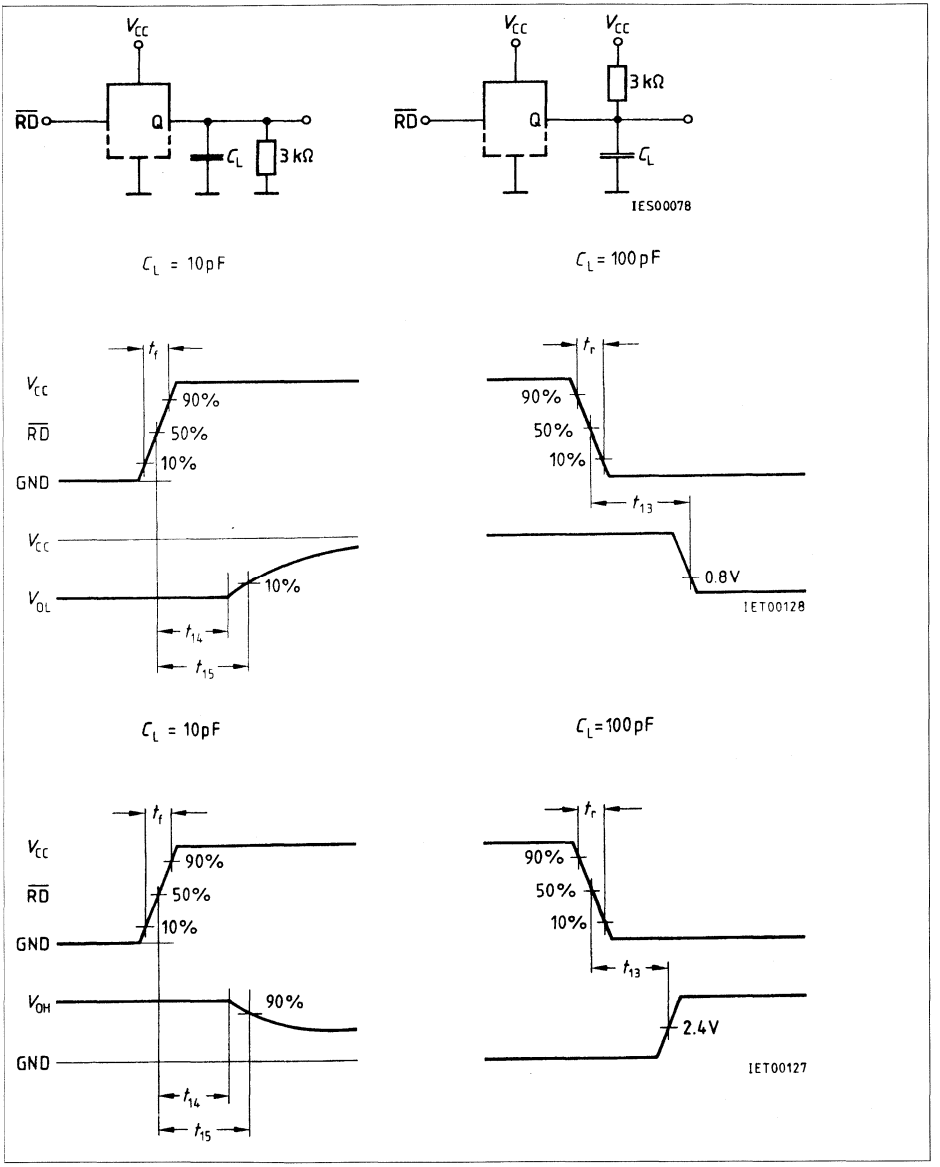


Figure 11
THREE-STATE Test Circuits and Timing Diagrams

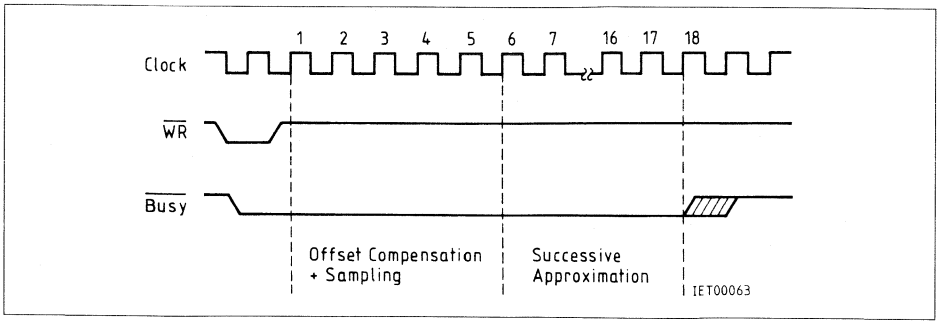
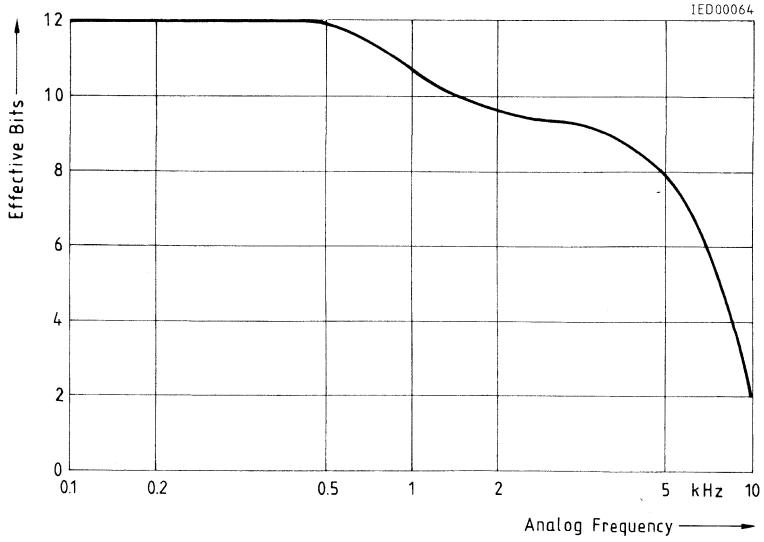


Figure 12
Converter Timing (SDA 0812 A)

7

Figure 13

Effective Number of Bits versus Analog Input Frequency (SDA 0812 A)
$V_{CC} = V_{DD} = +V_{REF} = 5$ V, $-V_{REF} = 0$ V; $f_{CLK} = 1$ MHz



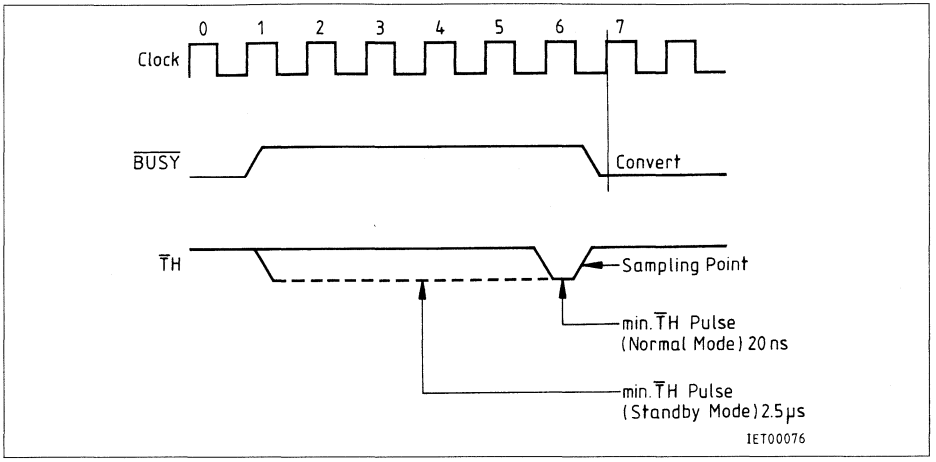


Figure 14
TH-Timing (SDA 1812 D)

Dynamic Performance (SDA 1812 D)

The SDA 1812 D is specified dynamically as well as with standard DC specifications.

Figures 15 and 16 show 2048 point FFT plots of the SDA 1812 D with analog input signals of 1 kHz and 50 kHz. When the SNR is calculated it includes harmonics.

Figure 15

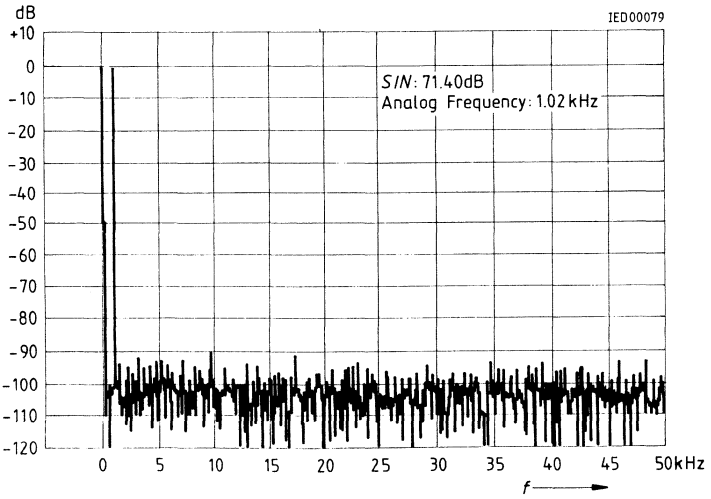
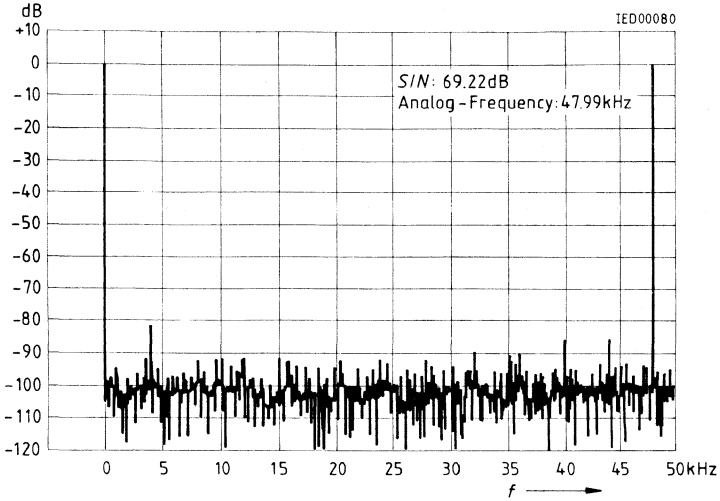


Figure 16

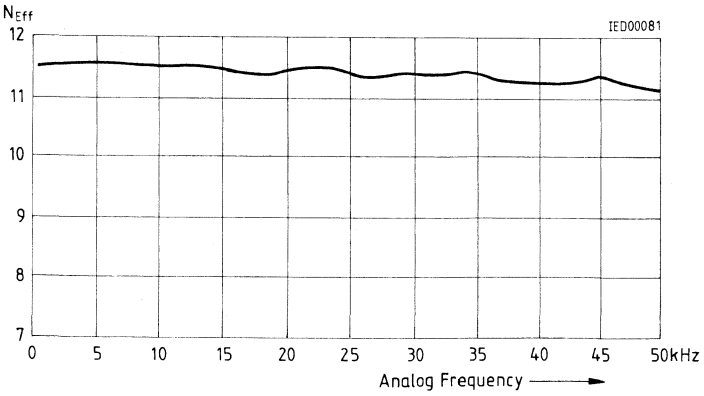


The relationship between Signal-to-Noise Ratio (*SNR* including harmonics) and the resolution of an ideal ADC with no differential or integral linearity errors is expressed in the following equation:

$$N_{eff} = \frac{SNR\,[dB] - 1.76}{6.02}$$

Figure 17

Typ. Effective Number of Bits versus Analog Input Frequency



Micorprocessor Interfacing

Microprocessor interfacing is straight forward and requires only a few external gates.

Siemens/Intel Microprocessors

A typical interface is shown in **figure 15**.

- Start of Conversion
  A write instruction selects one of the analog input channels and starts the conversion. Write Address: $\overline{\text{ADC-CS}}$, DATA pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate an interrupt to the micorprocessor (INT).
- Read the Conversion Result:
  A read instruction from the: $\overline{\text{ADC-CS}}$ -address fetches the low byte, a read instruction from $\overline{\text{ADC-CS}}$ -address + 2 the high byte.

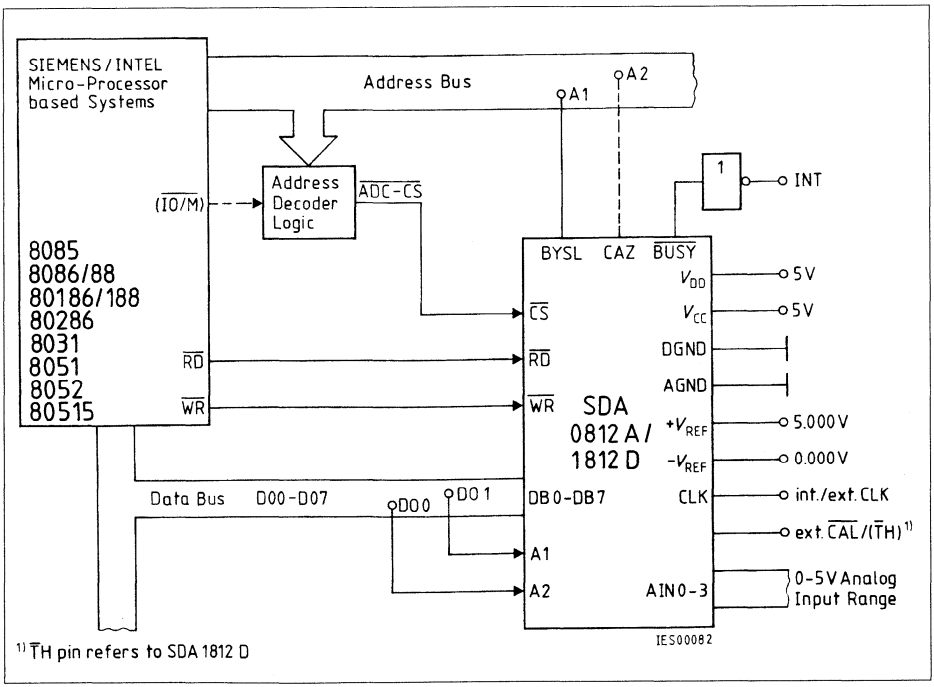


Figure 18

Motorola Microprocessors

A typical interface is shown below

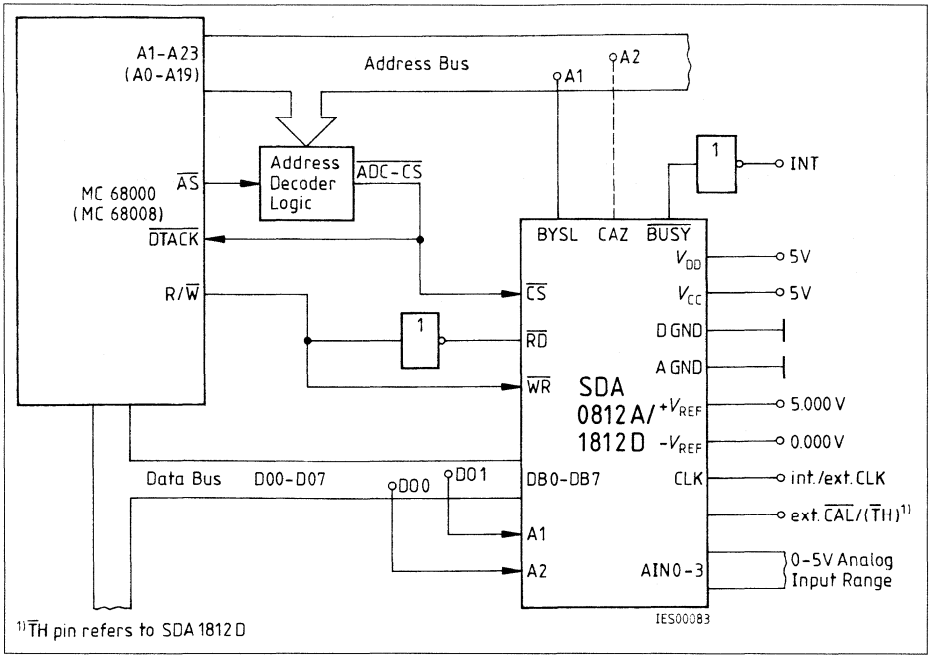


Figure 19

- **Start of Conversion**
  A WRITE instruction to an address decoded by the address decoder logic will start a conversion. The lower 2 bits of the data bus select the input channel. MOVE.W D0, ADC-ADDRESS.

- **Read the Conversion Result**
  A READ instruction to the ADC-ADDRESS puts the conversion result to the data bus: MOVE.PW$000 (ADC-ADDRESS), D0 places the 12-bit result of the conversion in the D0 register. The address decoder has to pull down $\overline{\text{ADC-CS}}$ wire at ADC-ADDRESS and ADC-ADDRESS + 2.
  Figure 20 shows how the result is placed in register D0.

		BUSY	0	0	0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Figure 20

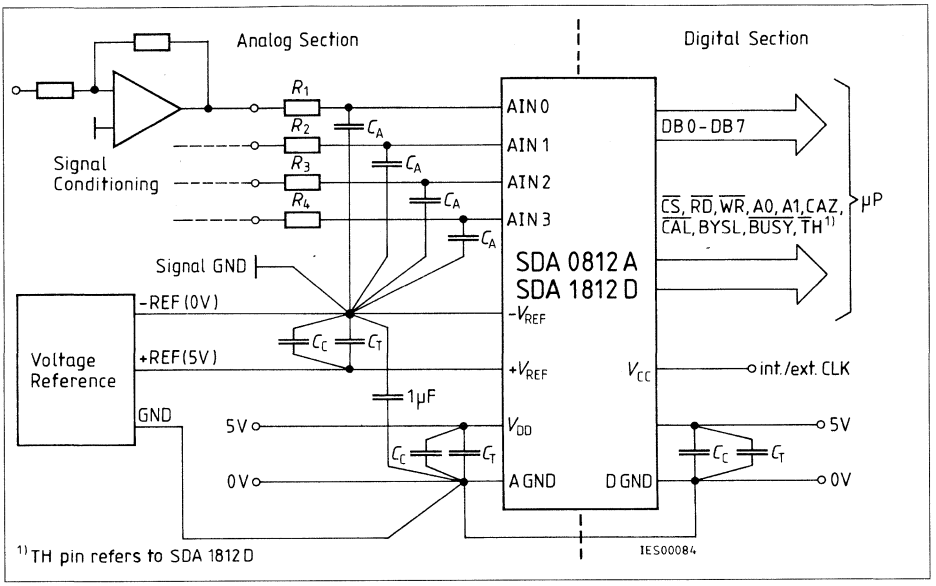


FIgure 21
Application Hints

	SDA 0812 A	SDA 1812 D
C_A	... 5 nF	... 10 nF
C_C	... 10 nF Ceramic	... 10 nF Ceramic
C_T	... 10 µF Tantal	... 10 µF Tantal
R_1 ... R_4	... 50 Ω	... 100 Ω

Power Supply Decoupling

The digital respectively analog 5 V power supply should be connected with a 10 µF tantalum capacitor to DGND respectively AGND. To ensure good HF performance this capacitor should be connected in parallel with a 10 nF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Note, that logic supply voltage V_{CC} must not be applied before V_{DD}!

Reference Voltage

To avoid dynamic errors a 10 µF tantalum capacitor connected in parallel with a 10 nF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 1 µF capacitor should be placed between – V_{REF} and AGND.

Analog Inputs

The high input impedance of the analog channels AIN 0 to AIN 3 allows simple analog interfacing. Signal sources – $V_{REF} \leq$ AIN $\leq$ + V_{REF} can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 50 pF, within 5 clock cycles.

All converter measurements are done with respect to the reference voltages, analog ground only powers the chip. Therefore – V_{REF} has to be used as the signal ground. The simple RC-filter 50 Ω, 5 nF (100 Ω, 10 nF) is recommended in order to protect the analog input against spikes and noise during the offset compensation period.

Application Note

For operation without any interferences, + V_{REF} must not exceed V_{DD} (see characteristics: $V_{DD} \geq V_{CC}$, $V_{DD} \geq$ + V_{REF}), especially not during switching-on. Please start autocalibration using pin CAL after all voltages (V_{DD}, V_{CC}, + V_{REF}, – V_{REF}) are stable.

Note

Values in brackets refer to SDA 1812 D.

SIEMENS

Microprocessor-Compatible 12-Bit Sampling A/D Converter with 4-Channel Multiplexer

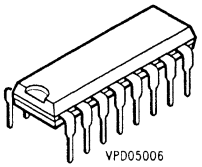
SDA 2812 A
SDA 3812 A

Preliminary Data

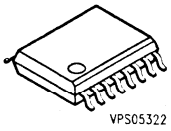
ACMOS

Features

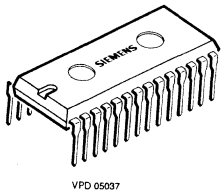
- Advanced CMOS (ACMOS) technology
- 12-bit resolution
- 100-kHz sampling rate
- Total unadjusted error ± 0.75 LSB
- Fast conversion time (7 µs)
- Sampling time 2.5 µs
- No missing codes
- Single 5 V DC supply
- 4-channel multiplexer with latched control logic
- Easy interfacing to all microprocessors, or stand-alone operation
- Serial output with optional MSB or LSB first (SDA 2812 A)
- 12-bit parallel output/serial output (SDA 3812 A)
- No offset or gain adjustment required
- TTL-compatible output voltages
- Latched tristate outputs
- Low power consumption (10 mW during conversion, 50 µW idle)
- Offset calibration circuit



P-DIP-16



P-DSO-16-3

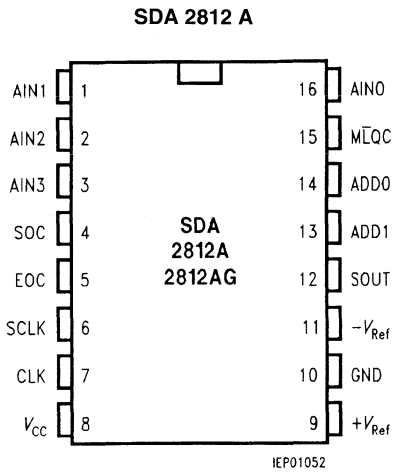


P-DIP-28

P-LCC-28-2

	Type	Ordering Code	Package
▼	SDA 2812 A	Q67100-A8355	P-DIP-16
▼	SDA 2812 AG	Q67100-A8356	P-DSO-16-3 (SMD)
▼	SDA 3812 A	Q67100-A8357	P-DIP-28
▼	SDA 3812 AN	Q67100-A8358	P-LCC-28-2 (SMD)

▼ = New type

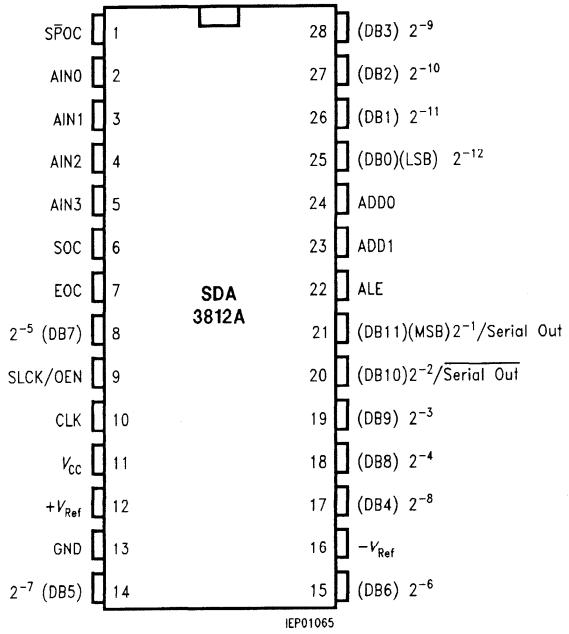


Pin Configurations
(top view)

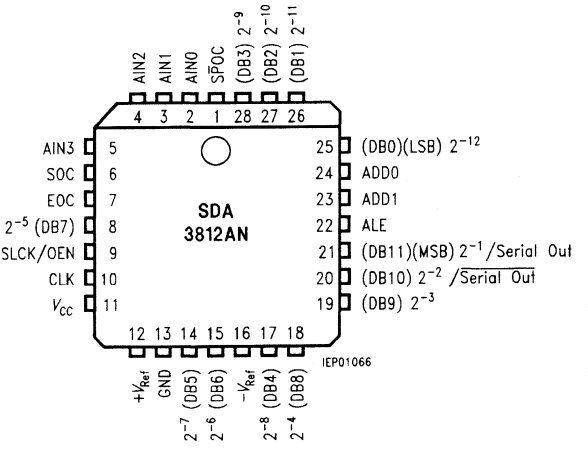
Pin Definitions and Functions (SDA 2812 A)

Pin	Symbol	Function
1 to 3	AIN 1 to AIN 3	Analog inputs
4	SOC	Start of conversion, T/$\overline{H}$
5	EOC	End of conversion
6	SCLK	External or internal clock for serial output
7	CLK	External clock input
8	V_{CC}	Positive supply voltage
9	+ V_{REF}	Upper reference voltage
10	GND	Ground
11	– V_{REF}	Lower reference voltage
12	SOUT	Serial output
13, 14	ADD1, ADD0	Address inputs
15	MLQC	MSB / LSB first control
16	AIN0	Analog input

SDA 3812 A



SDA 3812 AN



Pin Configurations
(top view)

Pin Definitions and Functions (SDA 3812 A)

Pin	Symbol	Function
1	$\overline{SP}OC$	Serial / Parallel output control
2 to 5	AIN0 - AIN3	Analog inputs
6	SOC	Start of conversion
7	EOC	End of conversion
8	DB7	Digital output signal
9	OEN/SCLK	Output enable / internal gate clock for serial output
10	CLK	External clock input
11	V_{CC}	Pos. supply voltage
12	$+ V_{REF}$	Upper reference voltage
13	GND	Ground
14, 15	DB5, 6	Digital outputs signals
16	$- V_{REF}$	Lower reference voltage
17 - 20	DB4, 8, 9, 10 / $\overline{\text{Serial Out}}$	Digital output signals / serial output inverted
21	DB11 (MSB) / Serial Out	Digital output signals / serial output
22	ALE	Address latch enable
23- 24	AD01, ADD0	Address inputs
25 - 28	DB0 (LSB), 1, 2, 3	Digital outputs

7

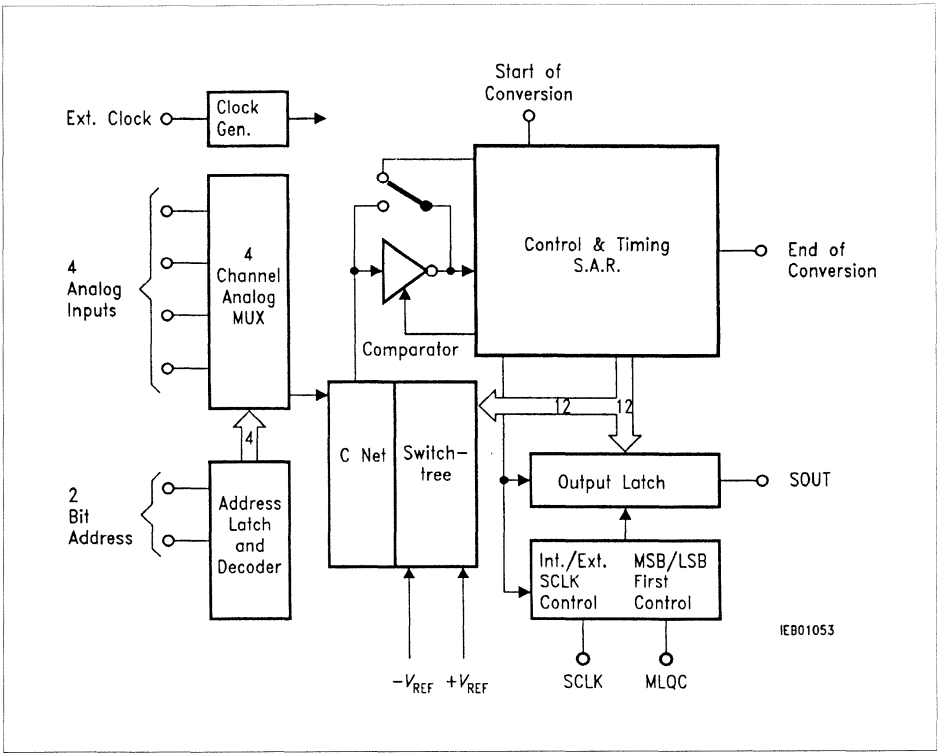


Figure 1 a
Block Diagram (SDA 2812 A)

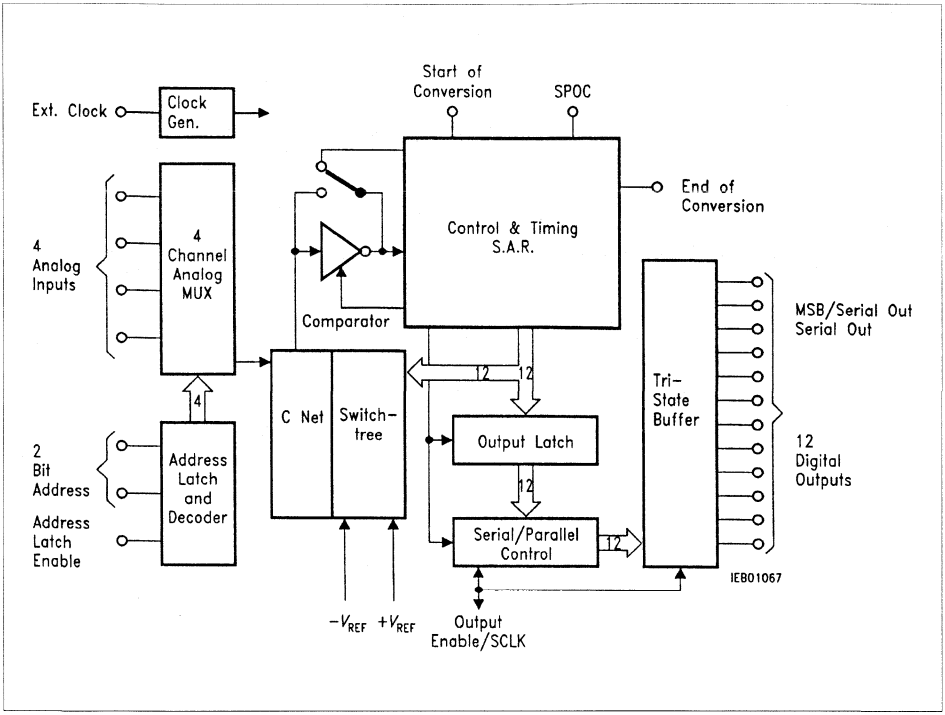


Figure 1 b
Block Diagram (SDA 3812 A)

7

General Description

SDA 2812 A and SDA 3812 A are monolithic CMOS 12-bit A/D converters with a single supply voltage of 5 V DC. They contain a microprocessor-compatible control logic and an optional MSB or LSB first serial output (SDA 2812 A) respectively a 12-bit parallel output (SDA 3812 A). SDA 2812 A/3812 A operate at a clock frequency of 2 MHz and offer enhanced dynamic performance for sampling rates up to 110 kHz.

The converters use the method of successive approximation by means of a capacitor network. The converters feature a temperature-stabilized differential comparator, a 4-channel multiplexer for 4 analog inputs and a sample and hold circuit. The converters do not need any external offset or gain adjustment. Easy interfacing to microprocessors is provided by 2-bit address latches, an output latch and an intelligent serial port. (SDA 2812 A), respectively 12-bit tristate data bus (SDA 3812 A).

The temperature range of the SDA 2812 A is – 40 to 85 °C.

Functional Description

Converter

The converter consists of three major parts: a capacitor network (approx. 30 pF) as a sample and hold circuit, a successive approximation register and a comparator.

The A/D converter's successive approximation register (SAR) is reset at the positive edge of the start of conversion (SOC) pulse. The conversion starts with sampling the analog signal. A conversion in process will be interrupted by a SOC pulse.

Following the rising edge of the SOC pulse, the end of conversion output (EOC) passes to low level. It is set to logic one with the first rising edge of the external clock after the internal latch pulse.

The comparator is a differential comparator for high power supply rejection.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 5 external clock cycles and will then be kept at the sampled level for the remaining conversion time. The external analog source must be capable of supplying the current that is necessary to charge the sample and hold capacitor of approximately 30 pF within those 5 clock cycles.

Conversion of the sampled analog voltage takes place between the 6th and 20th clock cycle after sampling has been completed. In the 20th clock cycle the result of the conversion is written into the output data latch. The EOC signal is set during the rising edge of the 20th clock cycle.

Multiplexer

The converter provides 4 multiplexed analog input channels. A particular input channel is selected by programming 2 address lines (ADD1, ADD0). The table shows the input states for the address lines to select a channel. The address is latched on the rising edge of the SOC signal (SDA 2812 A) (refer to **figure 7a**) respectively of the ALE signal (**figure 7b**, SDA 3812 A).

Address Lines		Select. Analog Channel
ADD1	**ADD0**	
L	L	AIN0
L	H	AIN1
H	L	AIN2
H	H	AIN3

Reading the conversion results (SDA 3812 A):

The data is read as a 12-bit parallel byte. The converter's digital outputs are positive true. The OEN signal enables the 12 bits parallel to the output buffers.

Autocalibration

An autocalibration circuit is included. It corrects offset errors only. Offset errors are adjusted in each conversion cycle, an initial offset calibration is done by power-up.

Power-Up

An autocalibration cycle is started by power up. The autocalibration cycle takes 256 clock cycles. A start of conversion signal interrupts this autocalibration cycle and gives a normal conversion result (with increased offset errors) the autocalibration cycle will be finished automatically after the conversion.

Power Consumption

The current consumption is typical 2 mA during a conversion and during autocalibration (power-on). If no conversion (calibration) is running, the power consumption will be typically 10 µA.

T / $\overline{H}$ Mode

Normal conversion is started by a SOC high pulse. The min. start pulse duration is 100 ns. In this case the sample point is defined by the rising slope of CLK pulse 6 after SOC (**see figure 2a**). If the SOC signal exceeds 5 CLK pulses the sample point will be defined by the falling slope of SOC (**see figure 2b**).

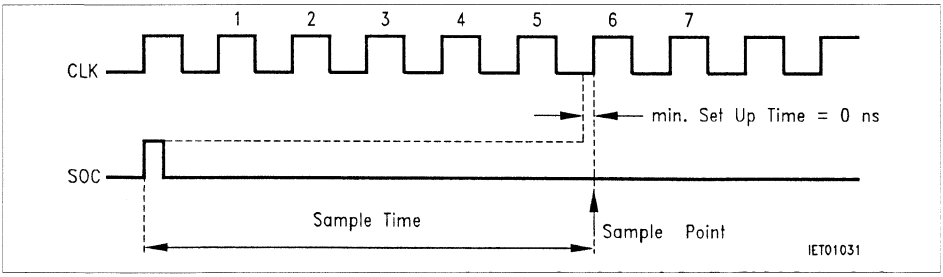


Figure 2a

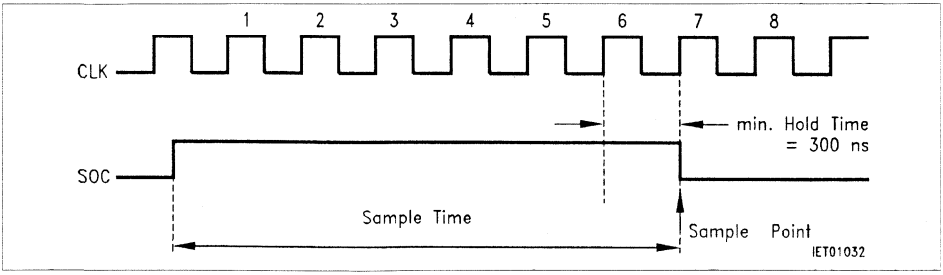


Figure 2b

Data Interface (SDA 2812 A)

The SDA 2812 A contains a programmable serial data interface. Pin 15 (MLQC) defines a MSB-first by using a high signal or a LSB-first serial data format using a low signal.

This serial output mode features an internal / external serial data clock using an intelligent SCLK pin. If there is an external CLK source it will use this CLK, if this pin is high Z an internal generated gated clock will be applied to this pin.

With the rising edge of SOC pin 6 is pulled high for 2 CLK periods (with 200 nA current source). If pin 6 really goes high it will be defined as high Z and an internal gated clock will be generated if the data are ready.

If pin 6 remains low an external CLK source will be detected and the SDA 2812 A waits for an external SCLK after EOC to shift the serial data out.

Internal Gated (SDA 2812 A)

After the calculation of the MSB during conversion an internal gated clock is generated and put out at pin 6 (SCLK). This clock has been derived from the central clock (CLK) and shifts out the data at pin 12, beginning with the MSB (**see figure 3a**) or LSB (**see figure 3b**).

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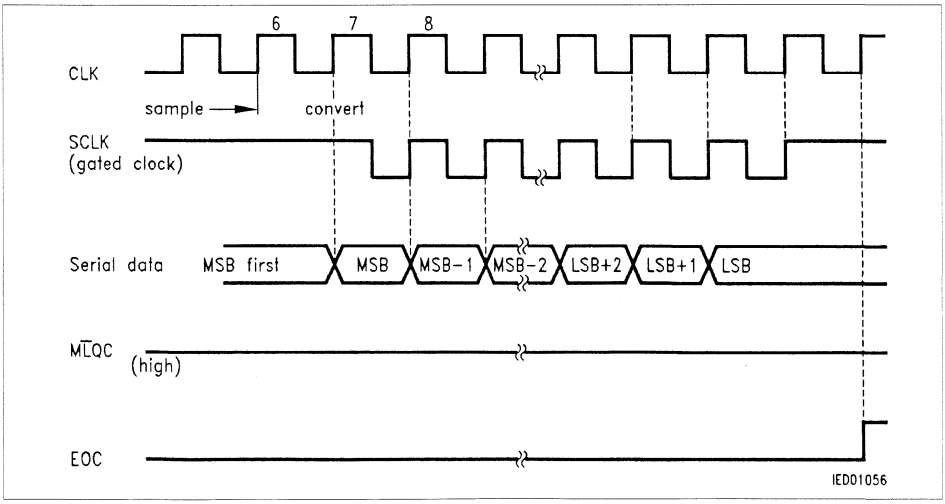

Figure 3a (SDA 2812 A)
Serial Data Out with Internal Gated Clock (MSB first)

The serial data appears MSB or LSB first as defined by MLQC (pin 15).

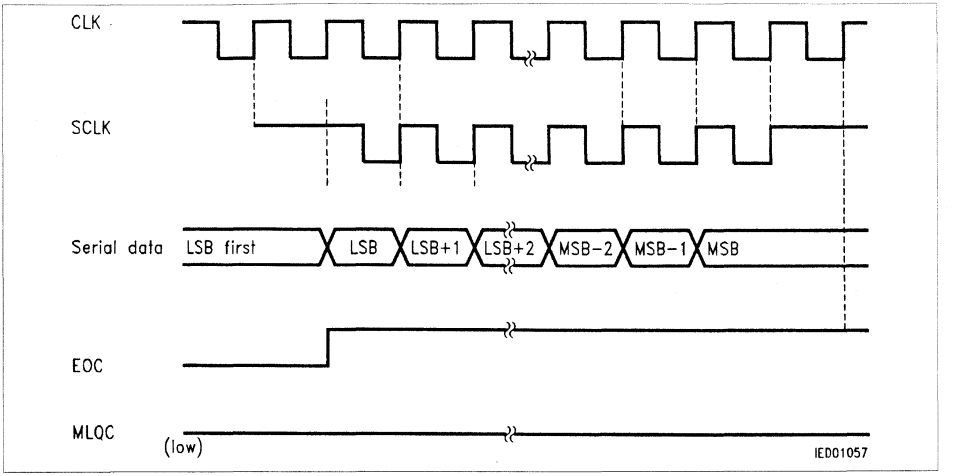

Figure 3b (SDA 2812 A)
Serial Data Out with Internal Gated Clock (LSB first)

The serial data appears MSB or LSB first as defined by MLQC (pin 15).

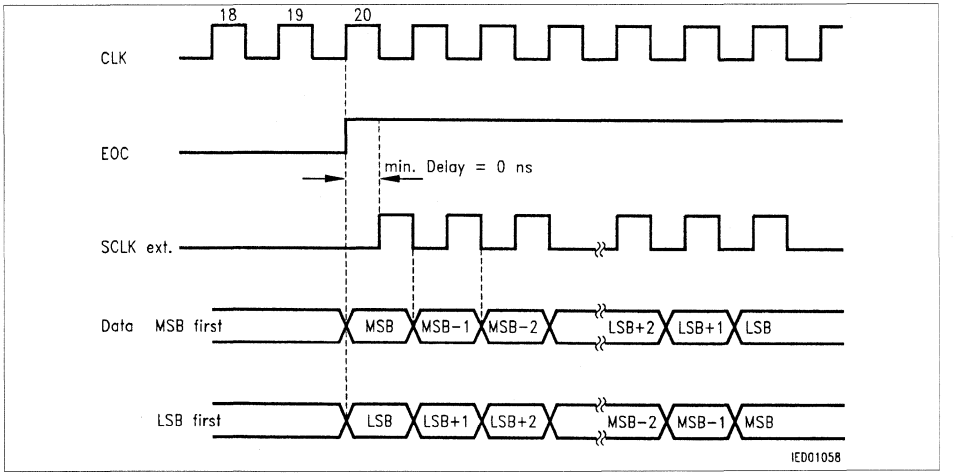

Figure 4a (SDA 2812 A)
Serial Data Out with External SCLK

The serial data are clocked out MSB or LSB first as defined by MLQC (pin 15).

The timing requirements for the external SCLK are: f_{min} = 0 Hz, f_{max} = 20 MHz.

Data Interface (SDA 3812 A)

The SDA 3812 A contains a 12-bit parallel and serial data interface. $S\overline{P}OC$ defines the output format, logic 0 at SPOC gives full parallel 12-bit data output, logic 1 at SPOC gives serial output at pin 21 (MSB).

Parallel Output (SDA 3812 A)

$S\overline{P}OC$ has to be connected to GND. An external OEN signal (on pin OEN/SCLK) enables the 12 bits parallel to the output buffers.

Serial Output (SDA 3812 A)

$S\overline{P}OC$ has to be connected to V_{DD}. The serial output mode features an internal / external serial data clock. The OEN/SCLK pin 9 is programmed into an intelligent SCLK pin. If there is an external CLK source it uses this CLK, if this pin is high Z an internally generated gated clock is applied to this pin. With the rising edge of SOC pin 9 (OEN/SCLK) is pulled up to high 2 CL periods (with 200 nA current source). If pin 9 really goes high it is defined as high Z and an internal gated clock is generated if the data are ready.

If pin 9 remains low an external CLK source will be detected and the SDA 3812 A will wait for an external SCLK after EOC to shift the serial data out.

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Internal Gated SCLK (SDA 3812 A)

After the calculation of the MSB during conversion an internal gated clock is generated and put out at pin 9 (OEN/SCLK). This clock has been derived from the central clock (CLK) and shifts out the data at pin 21, beginning with the MSB (**see figure 3c**).

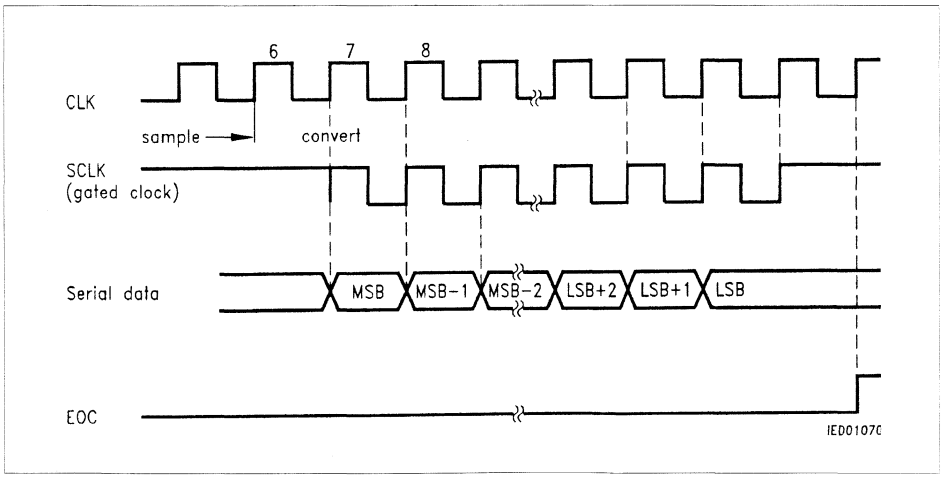


Figure 3c (SDA 3812 A)
Serial Data Out with Internal Gated Clock

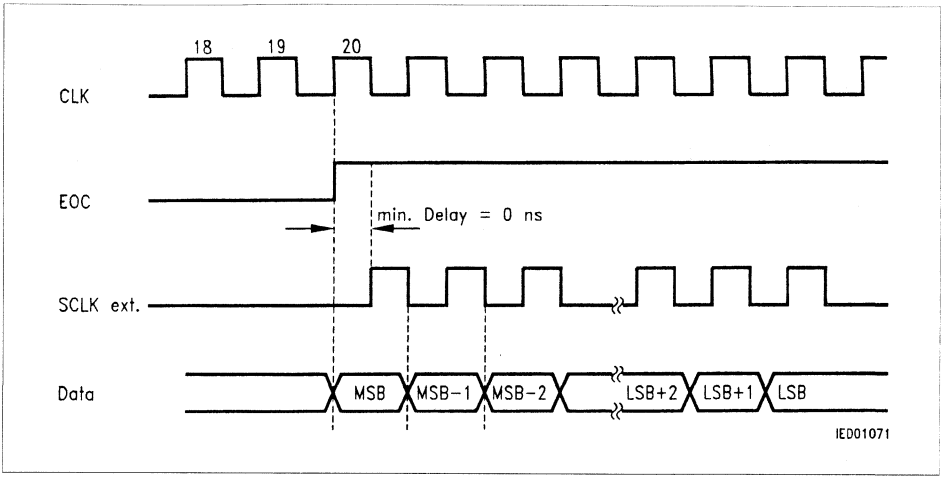


Figure 4b (SDA 3812 A)
Serial Data Out with External SCLK

External SCLK (SDA 3812 A)

If an external SCLK source is detected the SDA 3812 A will expect an external shift signal for pin 9 after end of conversion (EOC high). The serial data are shifted out MSB first with this clock source (**see figure 4b**).

The timing requirements for the external SCLK are: f_{min} = 0 Hz, f_{max} = 20 MHz.

Internal Clock Operation

The external circuitry for internal clock operation is shown in **figure 5**.

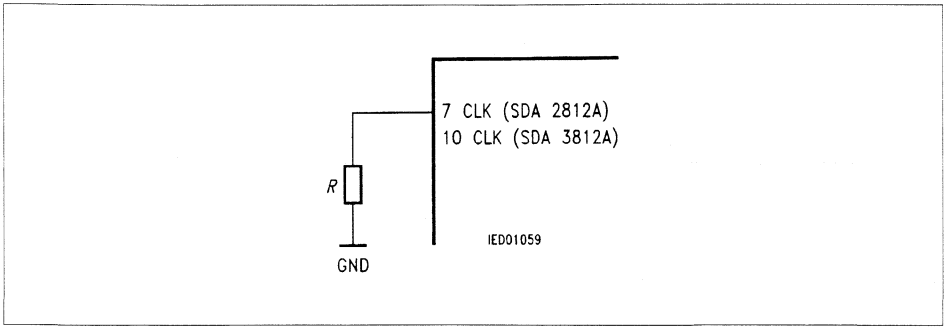


Figure 5
The Internal Clock Frequency only Depends on the R Value

The clock generator can be operated between 100 kHz and 2 MHz. Note that the specifications are referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.0 MHz.

The actual operating frequency of the internal clock oscillator can vary from device to device.

Therefore, for precisely defined conversion times use of an external clock generator is recommended.

External Clock Operation

The required circuitry for external clock operation is shown in **figure 6**.

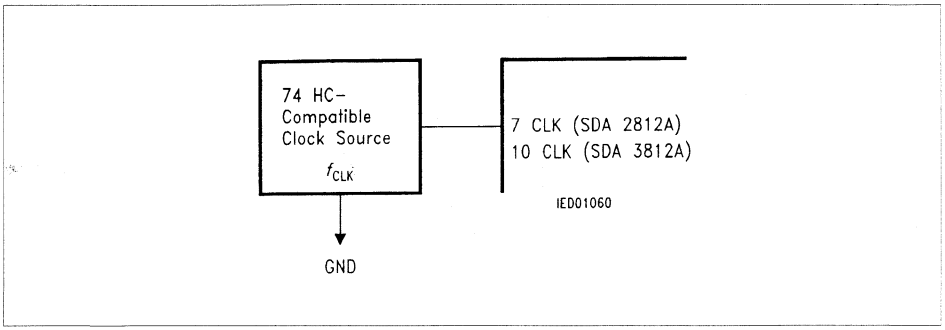


Figure 6
Circuitry for External Clock Operation

The external clock source has to provide 0.8 V max. for low voltage level and 3.5 V min. for high voltage level. The rise and fall times have to be 200 ns max. The minimal pulse width of ext. CLK has to be 200 ns.

There is no synchronizing between external clock and ext. T/$\overline{H}$ signal (see SOC). Synchronizing should be provided for optimum performance (see A/D converter timing). Note that the specification is referenced to f_{CLK} = 2 MHz. Typically, the specified accuracy is maintained from 0.5 to 2.2 MHz.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltages [1]	V_{CC}	–	–	6.5	V	–
Input voltage range (all inputs)	V_I	– 0.3	–	V_{CC} + 0.3	V	–
Thermal resistance system-air P-DIP-16	$R_{th\ SA}$	–	–	50	K/W	–
P-DSO-16-3	$R_{th\ SA}$	–	–	70	K/W	–
Junction temperature	T_j	–	–	125	°C	–
Storage temperature	T_{stg}	– 65	–	125	°C	–

Operating Range

Supply voltage	V_{CC}	4.5	5	6	V	–
Upper ref. voltage [2]	+ V_{REF}	–	V_{CC}	V_{CC} + 0.1	V	–
Lower ref. voltage	– V_{REF}	– 0.1	0	–	V	–
Differential ref. voltage	ΔV_{REF}		5	–	V	–
Analog input voltage	V_{AIN}	– V_{REF}	–	+ V_{REF}	V	–
Start pulse duration	t_{ws}	100	–	–	ns	–
Address load control pulse width	t_{wALE}	–	–	–	ns	–
Address setup time	t_{su}	20	–	–	ns	–
Address hold time	t_h	20	–	–	ns	–
Clock frequency	f_{CLK}	500	–	2200	kHz	–
Ambient temperature	T_A	– 40	–	85	°C	–

1) All voltages are referred to ground.

2) Care must be taken that this rating is observed even during power up.

Note: $\Delta V_{REF} = + V_{REF} - (- V_{REF})$.

Characteristics

V_{CC} = 4.75 to 5.25 V, unless otherwise specified; f_{CLK} = 2 MHz

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High-level input voltage, control inputs	V_{IH}	V_{CC} – 1.5	–	–	V	V_{CC} = 5 V
Low-level input voltage, control inputs	V_{IL}	–	–	1.5	V	V_{CC} = 5 V
High-level output voltage	V_{QH}	V_{CC} – 0.4	– –	–	V	I_Q = – 360 µA
Low-level output voltage data outputs	V_{QL}	–	–	0.45	V	I_Q = 1.6 mA
End of conversion	V_{QL}	–	–	0.45	V	I_Q = 1.2 mA
OFF-state (high impedance) Output current	I_{QZ} I_{QZ}	– –	– –	3 – 3	µA µA	V_Q = 5 V V_Q = 5 V
Control input current at max. input voltage	I_I	–	–	1	µA	V_I = 5 V
Low-level control input current	I_{IL}	–	–	– 1	µA	V_I = 5 V
Supply current	I_{CC} –	– –	2.0 10	2.5 50	mA µA	during conversion idle
Input capac., control inputs	C_I	–	10	15	pF	T_A = 25 °C
Outputs capacitance, data outputs	C_Q	–	10	15	pF	T_A = 25 °C
Resistance from pin 12 to 16	R	1	1000	–	kΩ	–

Characteristics (cont'd)

V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V; f_{CLK} = 2 MHz; T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog Multiplexer V_{CC} = 5 V						
Channel ON-state current [1]	I_{ON}	–	–	2	µA	V_I = 5 V
	–	–	–	– 2	µA	V_I = 0 V
Channel ON-state resistance	R_{ON}	–	1	–	kΩ	–
OFF-state current (High impedance state)	I_{OFF}	–	10	200	nA	V_{CC} = 5 V, T_A = 25 °C V_I = 5 V
	–	–	– 10	– 200	nA	V_{CC} = 5 V, T_A = 25 °C V_I = 0 V
	–	–	–	1	µA	V_{CC} = 5 V, V_I = 5 V
	–	–	–	– 1	µA	V_{CC} = 5 V, V_I = 0 V
Supply voltage sensitivity [2]	k_{SVS}	–	± 0.05	–	% / V	V_{CC} = + V_{REF} = 4.75 V to 5.25 V
Total unadjusted error [5]	*TUE*	–	± 0.75	± 1.5	LSB	–
Zero error [4]	*OFS*	–	± 0.5	± 1.0	LSB	–
Integral nonlinearity [3]	*INL*	–	± 0.5	± 1.0	LSB	–
Differential nonlinearity [3]	*DNL*	–	± 0.5	± 1.0	LSB	–
Gain error	*GE*	–	± 0.5	± 1.0	LSB	–
Sampling rate	f_s	–	–	100	kHz	f_{CLK} = 2 MHz
Effective number of bits	*ENOB*	–	11	–	bits	f_{AIN} = 50 kHz
Output enable time (**figure 8**)	t_{en}	–	25	50	ns	C_L = 50 pF, R_L = 10 kΩ
Output disable time (**figure 8**)	t_{dis}	–	40	95	ns	C_L = 10 pF, R_L = 10 kΩ
Output switch-OFF time (**figure 8**)	t_{OFF}	–	10	20	ns	C_L = 10 pF, R_L = 10 kΩ
Sample time [6]	t_{sample}	2.5	6	12	µs	f_{CLK} = 2 MHz / 1 MHz /
Conversion time [6]	t_{conv}	7	12	28	µs	500 kHz
Delay time, output EOC [7]	$t_{d\,EOC}$	0	20	50	µs	–

7

Characteristics (cont'd)

V_{CC} = + V_{REF} = 5 V, – V_{REF} = 0 V; f_{CLK} = 2 MHz; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Dynamic Performance [10) 11)]						
Signal-to-noise ratio	*SNR*	67	69	–	dB	Full scale input sinewave 1 kHz, f sampling is 100 kHz
	–	65	67	–	dB	Full scale input sinewave 1 kHz, f sampling is 100 kHz
Total harmonic distortion	*THD*	–	70	–	dB	Full scale input sinewave 50 kHz, f sampling is 100 kHz
Full power bandwidth (– 3 dB)	*BW*	–	4	–	MHz	–
Aperture delay time	–	–	5	–	ns	SOC pin, T/$\overline{H}$ condition

1) Channel on state current is primarily generated by the bias current into or out of the threshold detector and it varies directly with the clock frequency.

2) The supply voltage sensitivity relates to the ability of an A/D converter to maintain accuracy as the supply voltage varies.

3) The linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.

4) The zero error is the difference between the output of an ideal converter and that of the present A/D converter at zero input voltage.

5) Total unadjusted error is the max. sum of linearity error, zero error, integral and differential nonlinearity.

6) $t_{conv\ max}$ = 14.1/f_{CLK}, $t_{sample\ min}$ = 5.1 / f_{CLK}, $t_{sample\ max}$ = 6.1 / f_{CLK};

7) Refer to operating pulse diagram.

8) *SNR* includes harmonic distortion.

9) Sample tested at 25 °C.

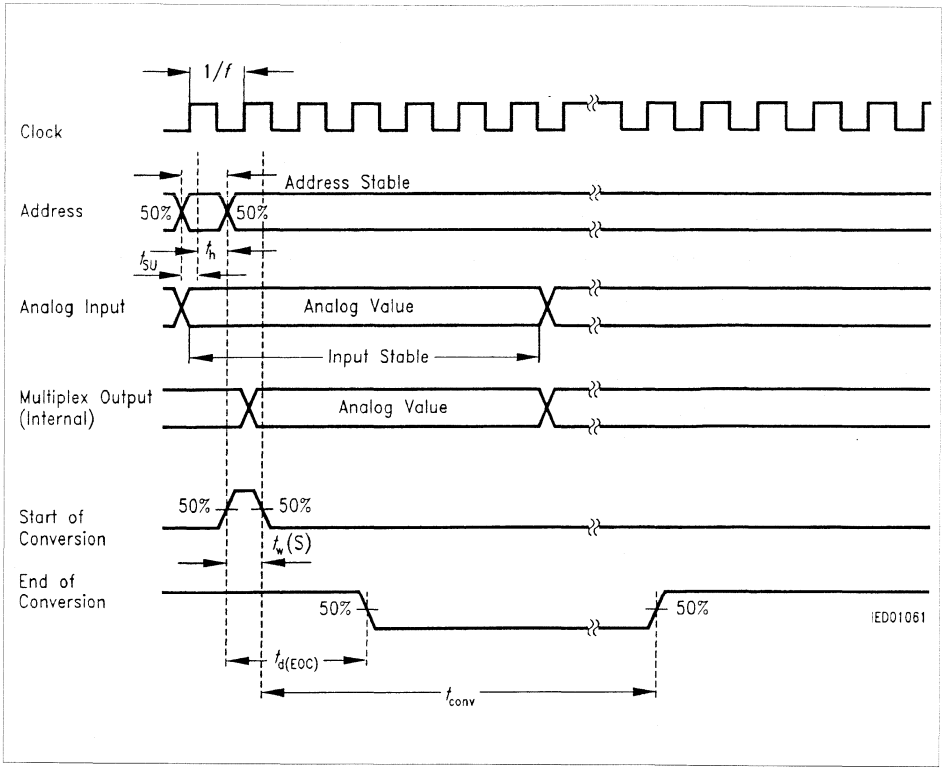


Figure 7a (SDA 2812 A)
Operational Pulse Diagram

7

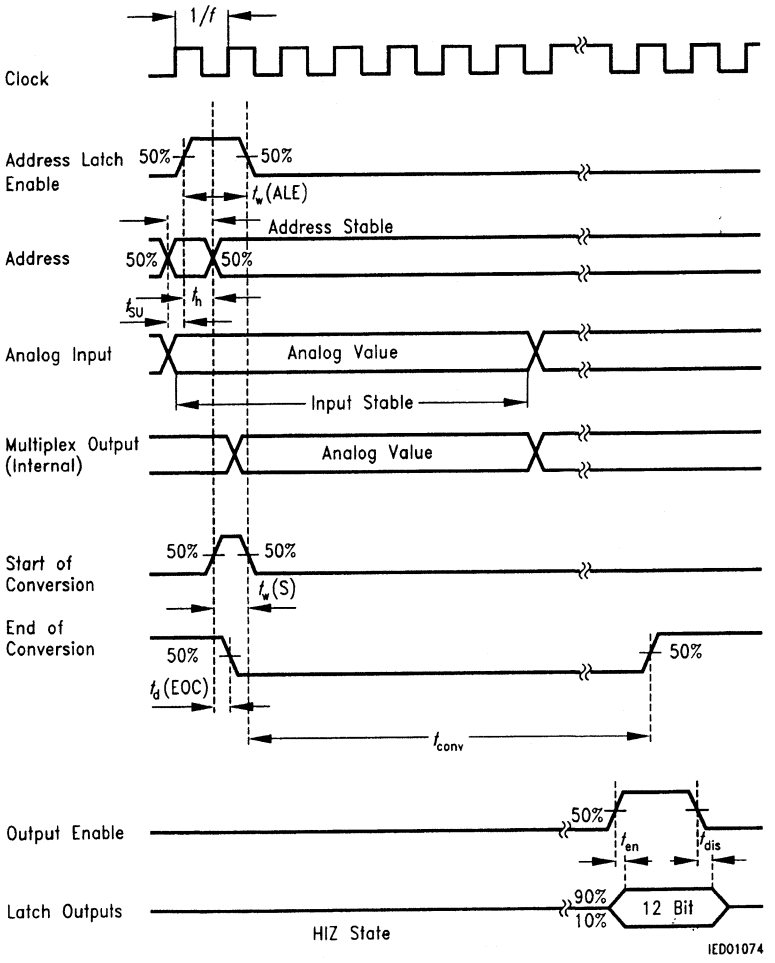


Figure 7b (SDA 3812 A)
Operational Pulse Diagram

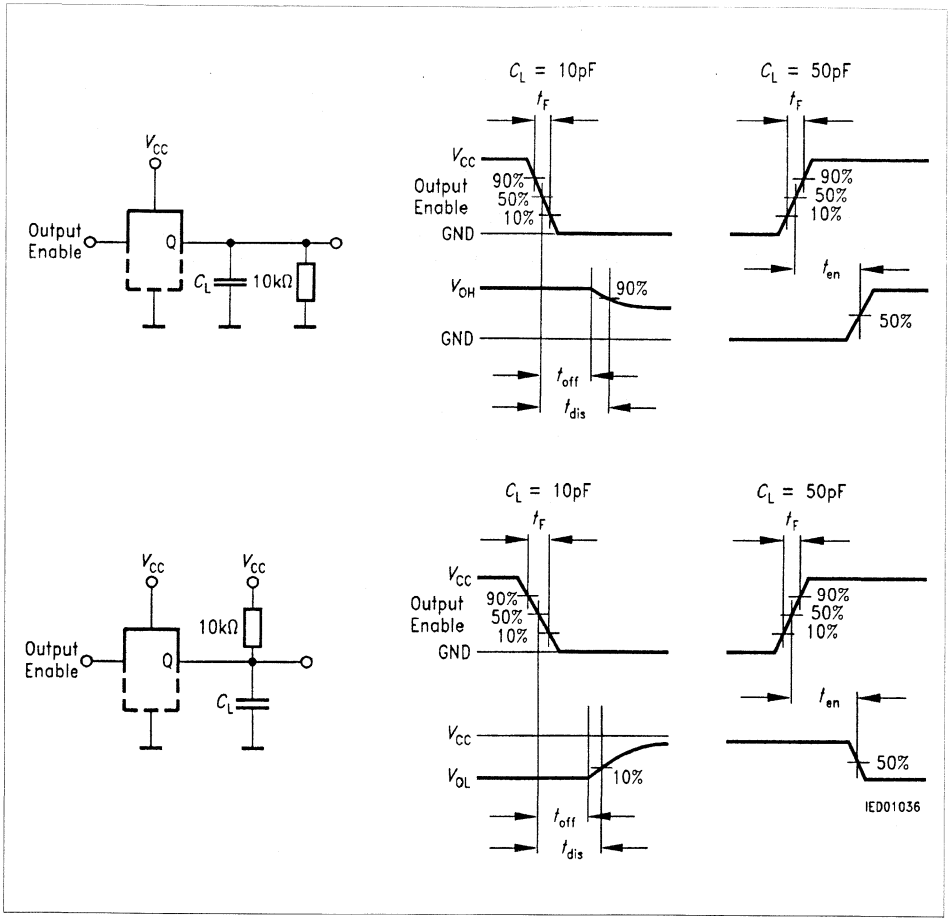


Figure 8
Tristate Test Circuits and Pulse Diagrams

Microcontroller Interface (SDA 2812 A)

A typical interface is shown in **figure 9a**.

- Start of conversion
  After applying the address for the input channel a SOC pulse starts the conversion.
- Reading the conversion result
  The serial interface of the microcontroller works as a shift register for data input. For using external SCLK, sent from TxD, the SCLK line of the ADC must be pulled down for at least two ADC-CLK periodes after the rising edge of SOC.
  The end of conversion-signal (EOC) can be used for producing an interrupt in the microcontroller. The lower 8 bits are transmitted to the microcontroller with the first serial data receiver instruction, the higher 4 bits with the second instruction.

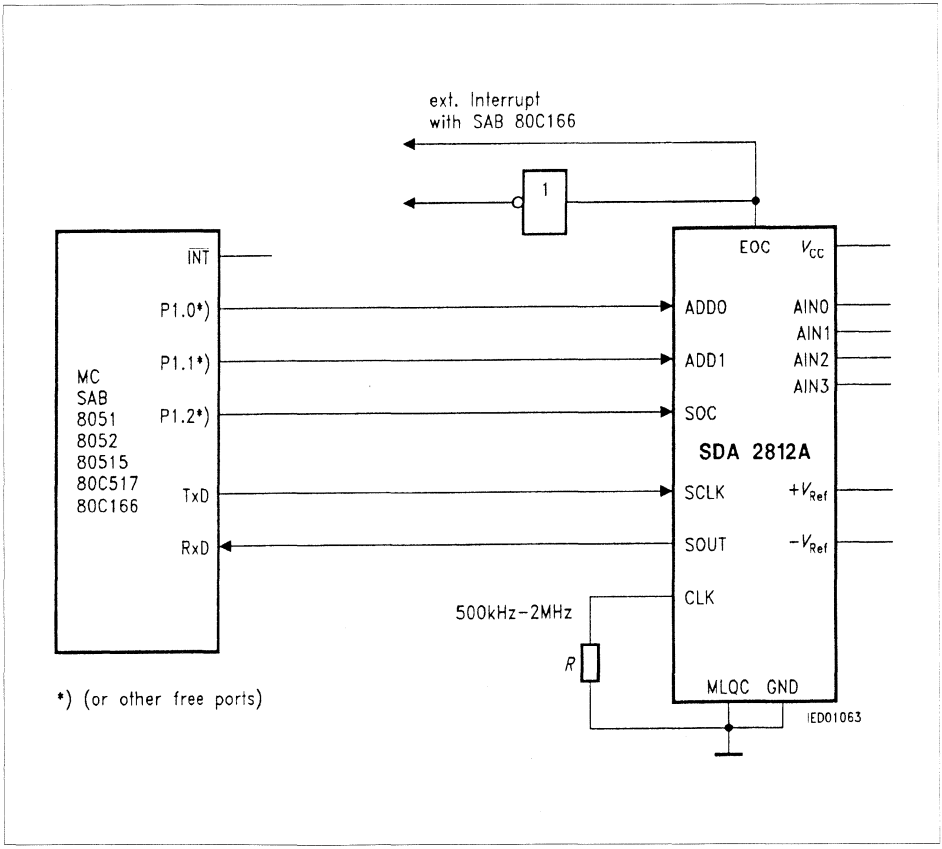


Figure 9a (SDA 2812 A)
Microcontroller Interfacing

Microprocessor Interface (SDA 3812 A)

Microprocessor interfacing is straightforward and requires only a few external gates.

Siemens Microprocessors / Microcontrollers

A typical interface is shown in **figure 9b**.

- Start of conversion
  A write instruction selects one of the analog input channels and starts the conversion.
  Write address: $\overline{\text{ADC\_CS}}$
  The end of conversion-signal (EOC) can be used for producing an interrupt in the microprocessor (INT or $\overline{\text{INT}}$).
- Reading the conversion result
  With a read instruction the 12 bits are read from the $\overline{\text{ADC\_CS}}$ address. For meeting the timing requirements of SDA 3812 A, bus wait states may be required.

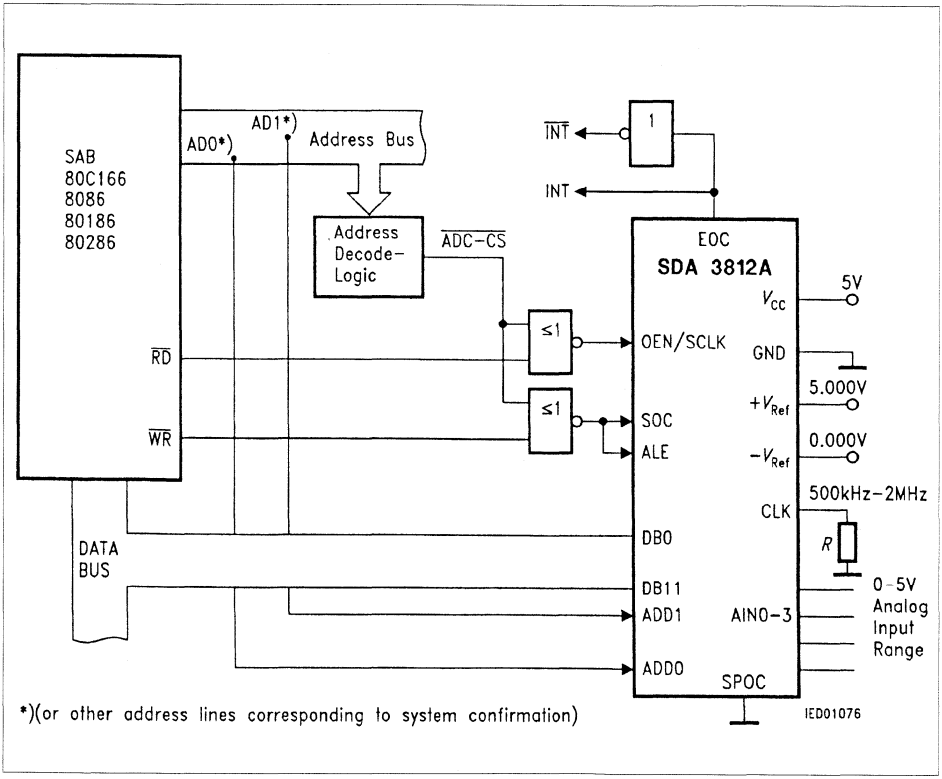


Figure 9b (SDA 3812 A)
Microcontroller Interfacing

Application

Power Supply Decoupling

The power supply of SDA 2812 A and SDA 3812 A should be connected with a 10 µF tantalum or an electrolytic capacitor. To insure good high frequency performance, this capacitor should be connected in parallel with an 0.01 µF ceramic capacitor. These capacitors should be placed as close as possible to the converter.

Reference Voltage

To avoid dynamic errors a 10 µF tantalum or electrolytic capacitor connected in parallel with an 0.01 µF ceramic capacitor should be placed as close as possible to the component between pins + V_{REF} and – V_{REF}. Also an 0.1 µF ceramic capacitor should be placed between pins – V_{REF} and GND.

Analog Input

The high input impedance of the analog innput channels AIN0-AIN3 allows simple analog interfacing. Signal sources (– V_{REF} ≤ AIN ≤ + V_{REF}) can directly be connected to the analog input channels, that is without additional buffering, if they are able to supply the current that is necessary to load the sample and hold capacitance being approx. 30 pF, within 5 clock cycles.

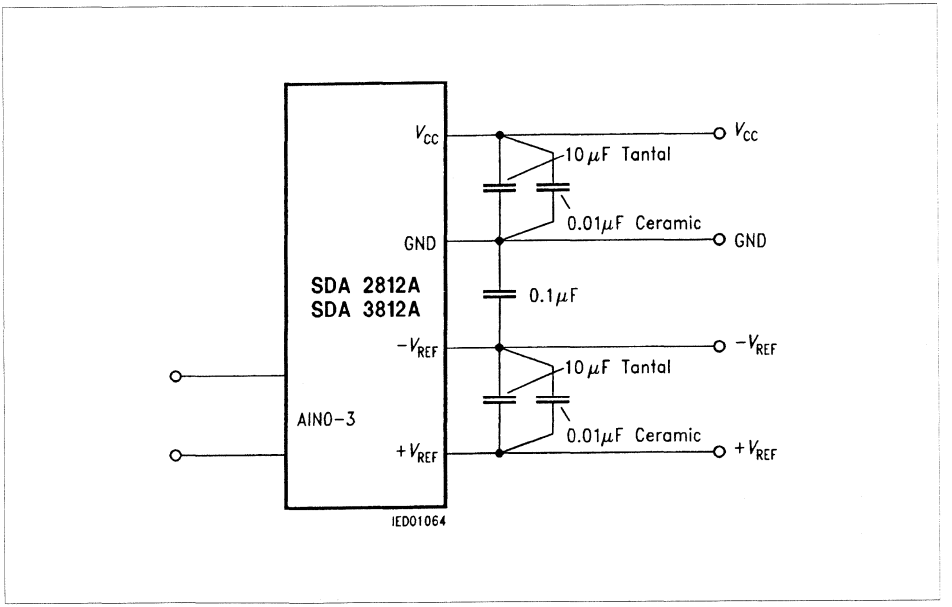


Figure 10
Capacitors

Selector Guide

Type	Package	Function	Page
SAE 0530	P-DIP-18-1	Programmable Timer for 50-Hz Line Frequency	471
SAE 0531	P-DIP-18-1	Programmable Timer for 60-Hz Line Frequency	471
SAE 0532 G	P-DSO-20-1	Timer for 50/60-Hz Line Frequency Switchable	471
TBB 278 B	P-DIP-22	Video Pulse Generator	492

= SMD

SIEMENS

Programmable Timer

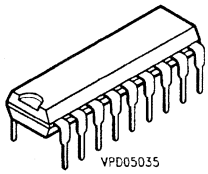
SAE 0530; SAE 0531; SAE 0532

Preliminary Data

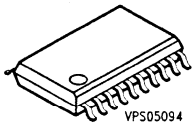
Bipolar IC

Features

- Direct operation from AC line or DC supply
- Time base: 50/60 Hz line frequency or any clock frequency up to 10 kHz
- Triac triggering with voltage synchronization for resistive loads, or with current synchronization for inductive and capacitive loads
- Triac gate trigger current up to 150 mA
- Continuous output current to relay actuation (max. 100 mA)
- Input and output delay can be retriggered
- 8 overlapping timing periods between 1 second and 32.5 hours
- Extended temperature range: – 25 to 85 °C



P-DIP-18-1

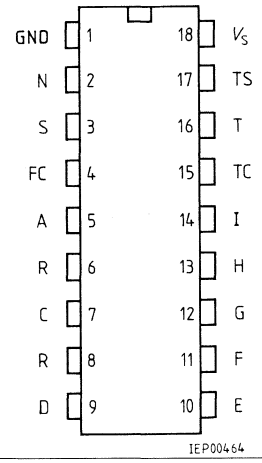


P-DSO-20-1

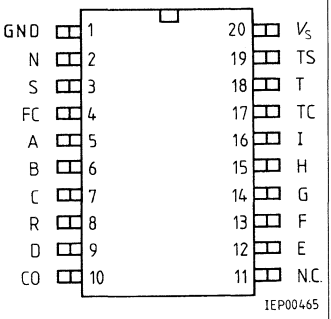
Type	Ordering Code	Package	Line Frequency
S SAE 0530	Q67000-H8403	P-DIP-18-1	50 Hz
S SAE 0531	Q67000-H8431	P-DIP-18-1	60 Hz
S SAE 0532 G	Q67000-H8432	P-DSO-20-1 (SMD)	50/60 Hz

With these programmable timers (50 Hz, 60 Hz, 50/60 Hz, respectively) delay times between 1 second and 31.5 hours can be set. Among other purposes they serve for triggering triacs in an AC line. The power may be supplied either by the AC line or by a DC source. The time base is the line frequency. The versatile programmable timers can be imployed in a great variety of applications, such as electronic timers, cooking equipment control, espresso machines, hand driers, coin changing machines and slot machines, stairwell-light time switches, industrial controls, developing systems for photographic labs, automatic starters (to preheat car engines), and operating-hours counters.

SAE 0530
SAE 0531



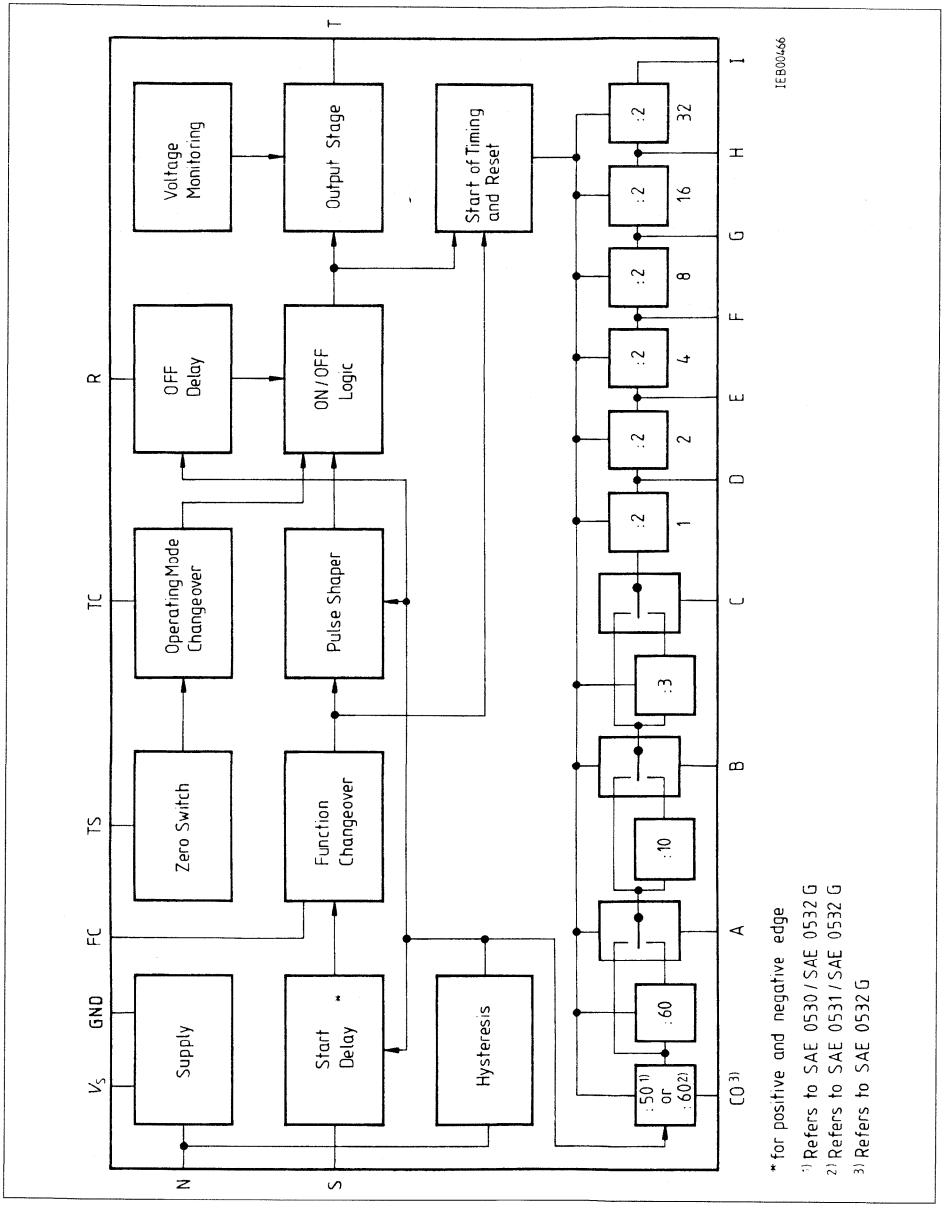
SAE 0532 G



Pin Configurations (top view)

Pin Definitions and Functions

SAE 0530 SAE 0531			SAE 0532 G		
Pin	**Symbol**	**Function**	**Pin**	**Symbol**	**Function**
1	GND	Circuit Ground	1	GND	Circuit Ground
2	N	Line voltage	2	N	Line voltage
3	S	Start	3	S	Start
4	FC	Function changeover	4	FC	Function changeover
5 6 7	A B C	Programming of basic timing unit	5 6 7	A B C	Programming of basic timing unit
8	R	Reset	8	R	Reset
9	D	Basic timing unit × 1	9	D	Basic timing unit × 1
10	E	Basic timing unit × 2	10	CO	50/60 Hz changeover
11	F	Basic timing unit × 4	11	N.C.	not connected
12	G	Basic timing unit × 8	12	E	Basic timing unit × 2
13	H	Basic timing unit × 16	13	F	Basic timing unit × 4
14	I	Basic timing unit × 32	14	G	Basic timing unit × 8
15	TC	Triac op. mode setting	15	H	Basic timing unit × 16
16	T	Triac triggering	16	I	Basic timing unit × 32
17	TS	Triac synchronization	17	TC	Triac op. mode setting
18	V_S	Positive supply voltage	18	T	Triac triggering
			19	TS	Triac synchronization
			20	VS	Positive supply voltage



Block Diagram

8

Functional Description

Programming of Delay Times

On input N there is a Schmitt trigger for detecting the clock signal plus rectifier and Z-diodes for deriving the operating voltage from the clock source (e.g. line voltage).

The clock signal is applied to a basic divider (1:50 or 1:60) to generate a seconds clock from the line frequency, three switchable dividers (1:60, 1:10 and 1:3) for setting the basic timing and six 1:2 dividers with open-collector outputs. The set time will have expired when the appropriate outputs go high. The basic-timing dividers are controlled by the wiring of inputs A, B and C (and CO)*. At 50- or 60-Hz clock frequency it is possible to set the following basic timing:

Changeover (SAE 0532 G)

CO	Line Frequency
L	60 Hz
H	50 Hz

Timing Range	A	B	C	Basic Timing	Max. Time
1	L	L	L	1"	1'3"
2	L	L	H	3"	3'9"
3	L	H	L	10"	10'30"
4	L	H	H	30"	31'30"
5	H	L	L	1'	1h3'
6	H	L	H	3'	3h9'
7	H	H	L	10'	10h30'
8	H	H	H	30'	31h30'

L: connected to 0; H: connected to V_S

The basic timing of the set range is doubled in flipflops 1, 2, 4, 8, 16 and 32. The flipflops are connected to pins D, E, F, G, H and I so that the latter adopt a certain value, i.e. 1, 2, 4, 8, 16 and 32. The required delay time on output T (triac driver) is calculated by the following equation: delay = basic timing × value D through I. This time is then produced by connecting the appropriate pins D through I to pin R (reset). If a number of the outputs D through I are connected to R, the times add up.

* Information in parentheses apply to SAE 0532 G.

Output	Period	Contribution to Delay
D	2 × basic timing	1 × basic timing
E	4 × basic timing	2 × basic timing
F	8 × basic timing	4 × basic timing
G	16 × basic timing	8 × basic timing
H	32 × basic timing	16 × basic timing
I	64 × basic timing	32 × basic timing

Example:

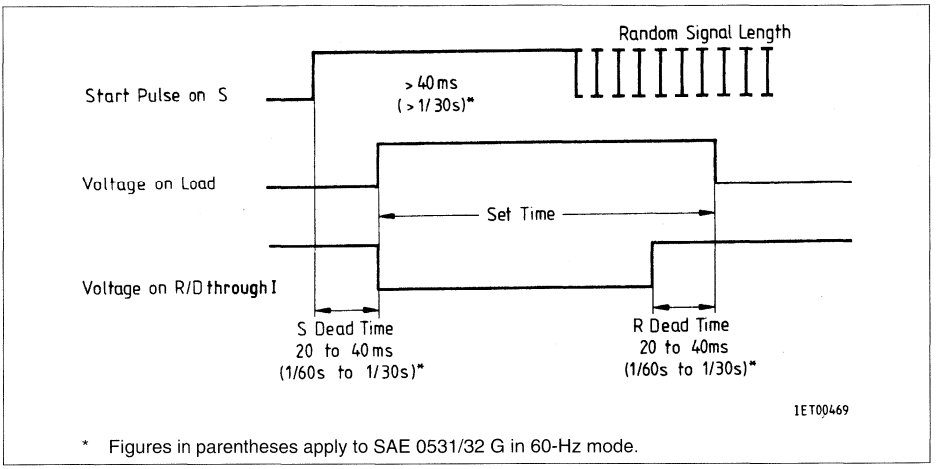
Line frequency 50 Hz (SAE 0530/31G) or 60 Hz (SAE 0531/32); set range 1 (basic timing = 1 s); D, F and I connected to R (value = 37): so the delay is 37 s.

Types of Delay

The circuit permits two different functions, which are selected on pin FC (function changeover). The two functions can be retriggered while the timing is running.

1. Turn-on interval DIN 46120 **(figure 1)**
   The triac connected to T turns on with the rising edge on the start input S and off when the set time has elapsed, and does this independently of the length of the start pulse. The effect of noise pulses on the start input is minimized by the dead times.
2. Dropout delay to DIN 46120 **(figure 2)**
   The triac turns on with the rising edge on S. The falling edge on S triggers the timing. The triac remains turned on until the set time has expired.

FC	Function
L	Turn-ON interval
H	Dropout delay



* Figures in parentheses apply to SAE 0531/32 G in 60-Hz mode.

Figure 1
Turn-ON Interval

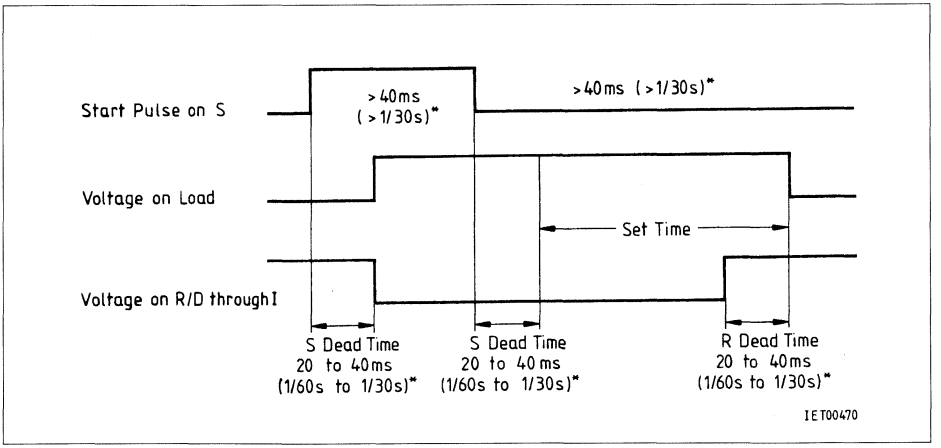


Figure 2
Dropout Delay

Start of Time Measurement (Figure 1, 2)

The frequency divider (and thus the time measurement) is started

- for the turn-on interval function (FC = L) with start input S = H by two negative edges on N,
- for the dropout delay function (FC = H) with S = H during at least two negative edges on N and then S = L by two more negative edges on N.

New Start of Time Measurement and Counter Reset

If, with the reset input R = L, the start input S is toggled (observing the condition: at least two negative edges on N), the time measurement is started again each time (retrigger function). When R = H and there are two negative edges on N, the counter is reset (reset function). This clocked control ensures a large degree of resistance to noise pulses that are coupled in. The reset function is also enabled by turning on the supply voltage, because the IC has a startup circuit. But this only takes effect if the preceding interruption of the supply voltage was long enough (in the region of a few ms). This avoids reset caused by interference on the supply voltage.

Output Stage

The output stage is also controlled by S and R. The open-collector output T is enabled by S = H and disabled by R = H when there are two negative edges on N (and when the supply voltage is turned on).

If start input S and reset input R are high at the same time, the output is enabled by the second negative edge and turned off again by the next positive edge (as long as R has not gone low in the meantime, as is usually the case). If the operating voltage drops below the operating limit of the circuit (approx. 3 V), the output is turned off for this duration.

Triac Modes (Figure 3, 4)

Different modes can be set for the enabled output by appropriate wiring of inputs TC (triac mode) and TS (triac synchronization):

- Mode 1 (TC on V_S) (voltage synchronization)
  Output T is connected to the zero-voltage switch. T conducts when $V_S - 1.3\ V \leq V_{TS} \leq V_S + 1.3\ V$; **see Application Circuit 1** (operation of resistive loads).
- Mode 2 (TC via C_e on GND or open) (current synchronization)
  Output T is connected to the zero-voltage switch via a monoflop. T issues a driving pulse, determined by C_e, when $V_S - 1.3$ V is no longer maintained on TS or $V_S + 1.3$ V is exceeded; **see Application Circuit 2.**
  In the current-synchronization mode, gate-trigger current is supplied to T until the triac has fired. If the triac does not fire because the load current is too small, the trigger current flows permanently, which can lead to a drop in the supply voltage. In this way the current is reduced further and the supply voltage continues to drop until ultimately the output is turned off because the lower limit of the operating voltage is reached. The circuit remains in this state until T is finally disabled by the timing control. This process can be avoided by ensuring that the triac fires in all operating conditions.
- Mode 3 (TC and TS on V_S)
  Output T conducts after the start pulse. This is used for any load in continuous driving of the triac (e.g. at low power levels) or if, instead of the triac, another load is operated; **see Application Circuits 3, 4 and 5.**

Inputs N, S, R, FC, A, B, C (and CO) * have an internal pullup resistor, i.e. they are high if not wired. On start input S there are also clamping diodes to V_S and GND so that it is possible to start with external potential. Reset input R is usually connected to one or more of the open-collector outputs D through I, enabling cutout of the load and resetting of the counter when the set delay has elapsed. These outputs are turned off (R = H) in their basic state (after reset), conduct when the time measurement starts (R = L) and are turned off again (R = H) after the delay **(see Figure 1 and 2)**.

* Figures in parentheses apply to SAE 0532 G.

Operation with Line Voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC network **(see Application Circuit 6).**

Operation with DC Voltage

This IC can also be operated with DC voltage or current
(see Application Circuits 4 and 5).

Useful Hints

- To obtain better noise immunity the pins D through I which are not connected are to be applied to GND.
- C_L
  If short-term line failures are to be compensated, C_L has to be accordingly higher.
- **Application Circuit 1** (voltage synchronization for resistive load)
  An average I_{TS} of 0.025 mA was inserted into the formula approximating R_{SYN}. As I_{TS+} and I_{TS-} contain production deviations, utilizing the determined R_{SYN} requires certain tolerances to be taken into account for pulse length Z.
- **Application Circuit 2** (current synchronization)
  In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the hold current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering. The noise band and/or the noise amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYN} and should not exceed 20 V.
- **Application Circuit 6**
  To limit the inrush current, R_{SS} has to be $\geq 0.2\ R_S$. Otherwise, the circuit might be destroyed.
- **Application Circuit 9**
  If the delay is made selectable by using a mechanical switch, it should be noted that all inputs, because of the pullup, are high in an unwired condition.
- Brief interruptions can be made ineffective by wiring with a capacitor. On S and R there is extra protection through the clocked control with a decision interval of one to two clock cycles.

8

Pulse Diagrams for Triac Operating Modes 1 and 2

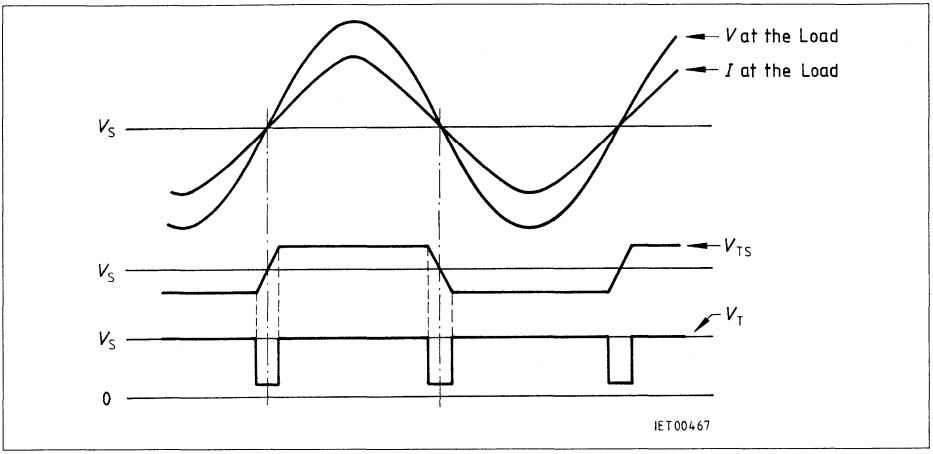


Figure 3
Operating Mode 1: Voltage Synchronization with Resistive Loads (TC at V_S)

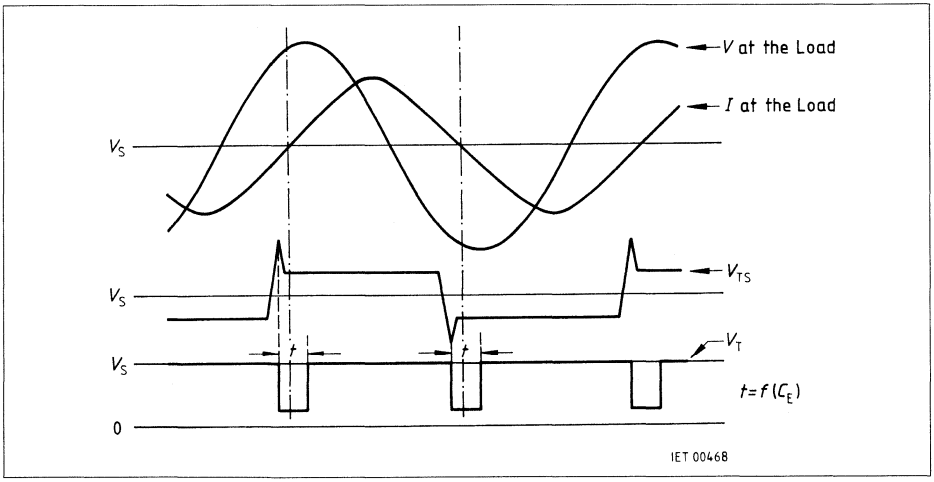


Figure 4
Operating Mode 2: Current Synchronization with Non-Resistive Loads
(Capacitance C_e at TC)

Absolute Maximum Ratings

T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage[1]	V_S	– 0.3	5.5	V	
AC at N[2]	$I_{N\,rms}$		35	mA	RMS value
DC from N[2]	$-I_N$	– 18	18	mA	Average value
Peak current at N[2]	I_{Np}	– 200	200	mA	2 ms, 100 ms interval
Voltage at A, B, C, FC, N, R, S, TC, CO	$V_{A...}$	– 0.3	V_S + 0.3	V	
Voltage at D, E, F, G, H, I, T	$V_{D...}$	– 0.3	20	V	D ... T off-state
Voltage at TS	V_{TS}	V_S – 0.7	V_S + 0.7	V	
Current in D, E, F, G, H, I	$I_{D...}$		0.5	mA	D ... I on-state
Current at S[3]	I_{IS}	– 2	2	mA	
Continuous current in T	I_T		100	mA	T on-state
Peak current in T	I_{Tp}		150	mA	1 ms/10 ms interval
Current at TS	I_{TS}	– 4	4	mA	
Junction temperature	T_j		125	°C	
Storage temperature range	T_{stg}	– 55	125	°C	
Thermal resistance system - air	$R_{th\,SA}$		70	K/W	P-DIP-18-1
	$R_{th\,SA}$		90	K/W	P-DSO-20

Operating Range

Supply voltage[4]	V_S	4.5	5.5	V	
Supply current (DC)[4]	$-I_N$	2.5	18	mA	[5]
Supply current (AC)[4]	$I_{N\,rms}$	5	35	mA	[5]
Ambient temperature	T_A	– 25	85	°C	

Notes

1) with impressed voltage at V_S

2) with impressed current at N

3) with impressed current at S

4) The IC can be operated with impressed voltage or with impressed current. With impressed voltage at V_S the voltage that is applied can be between 0 and $V_{S\,max}$ V (see maximum ratings). With impressed DC or AC at N, V_S is internally limited and thus ranges between 6 and 8.2 V (typ. 7.5 V). Operation, however, is also ensured if V_S falls to 4.5 V.

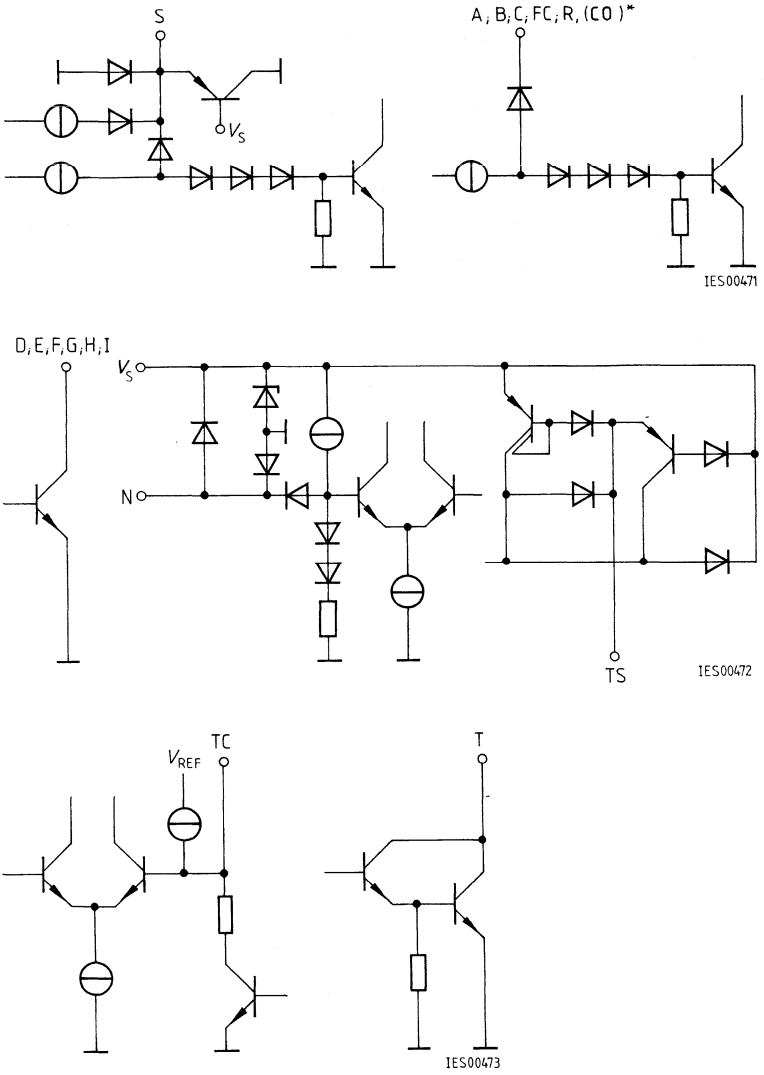
5) Only supply current for I_S, i.e. without triac gate current. The rms gate current additionally flows through N.

Characteristics

V_S = 5.5 V; T_A = 25 °C

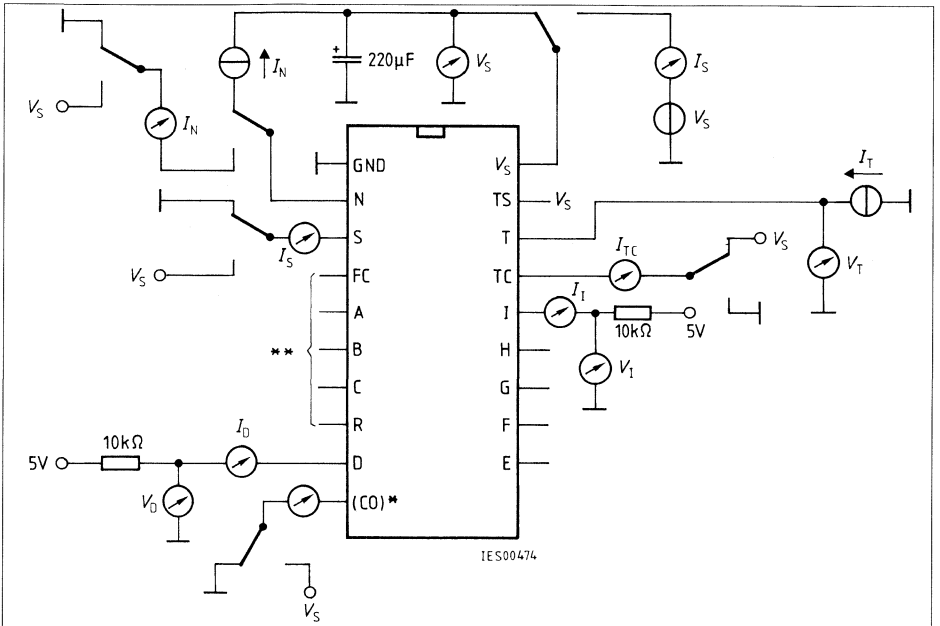
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current [1]	I_S		1.6	2.5	mA	V_{IS} = 0 V	1
V_S (impressed DC) [2]	V_S		7.5	8.0	V	$-I_N$ = 2.5 mA	1
V_S (impressed AC) [2]	V_S		7.5	8.0	V	$I_{N\,rms}$ = 5 mA	1
Voltage at S [3]	V_{IS}		V_S + 0.9	V_S + 1.0	V	I_{IS} = 2 mA	
		−0.9	− 0.8		V	$-I_{IS}$ = 2 mA	
Switching threshold at A, B, C, S, FC, R, CO	$V_{A...}$	1.0	1.8	2.4	V		2
H-switching threshold at N [4]	V_N		1.8	2.4	V		2
L-switching threshold at N [4]	V_N	0.8	1.2		V		2
Switching hysteresis at N [4]	V_N	0.4	0.6	0.9	V		2
Switching threshold at TC (capacitor charge)	V_{TC1}	0.8	1.4	2.2	V		2
Switching threshold at TC	V_{TC2}	2.5	3.3	4.0	V		2
Switching threshold at TS	V_{TS+}		V_S + 1.3		V	$V_{TS} > V_S$	2
	V_{TS-}		V_S − 1.3		V	$V_{TS} < V_S$	2
L-input current at A, B, C, FC, R, CO	$-I_{A...}$		20	35	µA	$V_{A...}$ = 0 V	1
L-input current at S	$-I_{IS}$		60	105	µA	V_{IS} = 0 V	1
L-input current at N [4]	$-I_N$		40	70	µA	V_N = 0 V	1
H-input current at A, B, C, S, FC, R, CO	$I_{A...}$			1	µA	$V_{A...} = V_S$	1
H-input current at N [4]	I_N			1	µA	$V_N = V_S$	1
H-input current at TC	I_{TC}		20	45	µA	$4.5 \le V_{TC} \le V_S$	1
L-input current at TC	I_{TC}		20	45	µA	V_{TC} = 0 V	1
Pos. switch-over current at TS	I_{TS+}	10	25	40	µA	R_{SYN} = 0	2
Pos. switching hysteresis at TS	I_{Hy+}	0.3	1.0	4	µA	R_{SYN} = 0	2
Neg. switch-over current at TS	I_{TS-}	10	25	40	µA	R_{SYN} = 0	2
Neg. switching hysteresis at TS	I_{Hy-}	0.3	1.0	4	µA	R_{SYN} = 0	2
L-voltage at D, E, F, G, H, I	$V_{D...}$		0.15	0.4	V	$I_{D...}$ = 0.5 mA	1
H-reverse current at D, E, F, G, H, I	$I_{D...}$			1	µA		1
L-output voltage at T	V_Q		0.7	1.0	V	I_T = 1 mA	1
	V_Q		0.8	1.2	V	I_T = 10 mA	1
	V_Q		1	1.5	V	I_T = 100 mA	1

[1] with impressed voltage at V_S
[2] with impressed current at N
[3] with impressed current at S
[4] if N is clock input



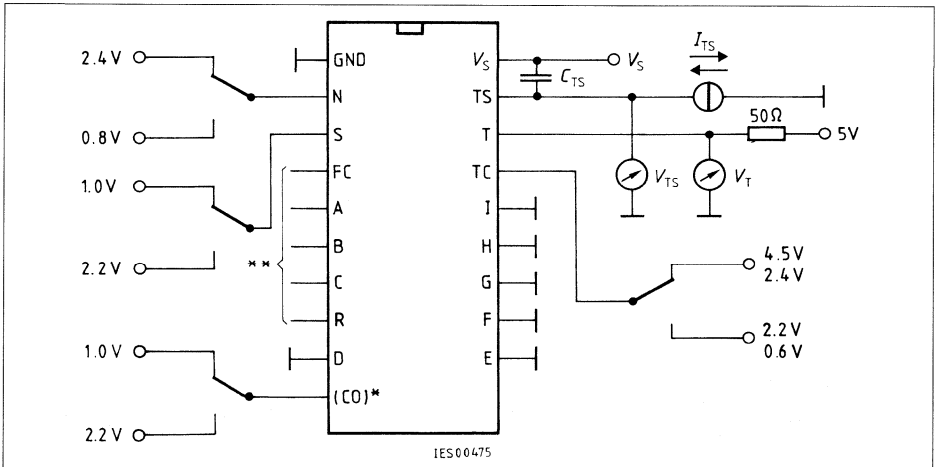
* Figures in parentheses apply to SAE 0532 G.

Internal Wiring of Inputs/Outputs and Supply Pins



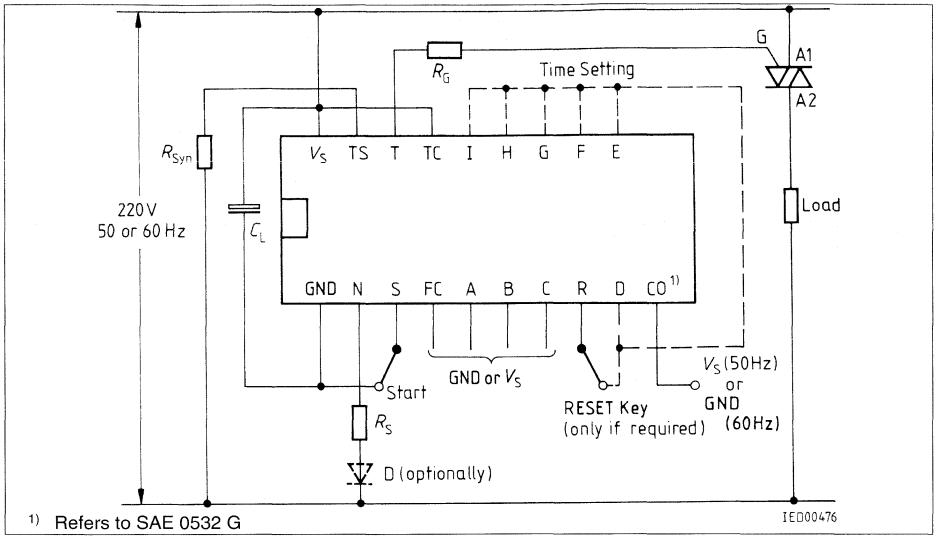
* The symbol in parentheses applies to SAE 0532.
** The external wiring of pins FC to R equals to that of pin S (Test Circuit 1)

Test Circuit 1

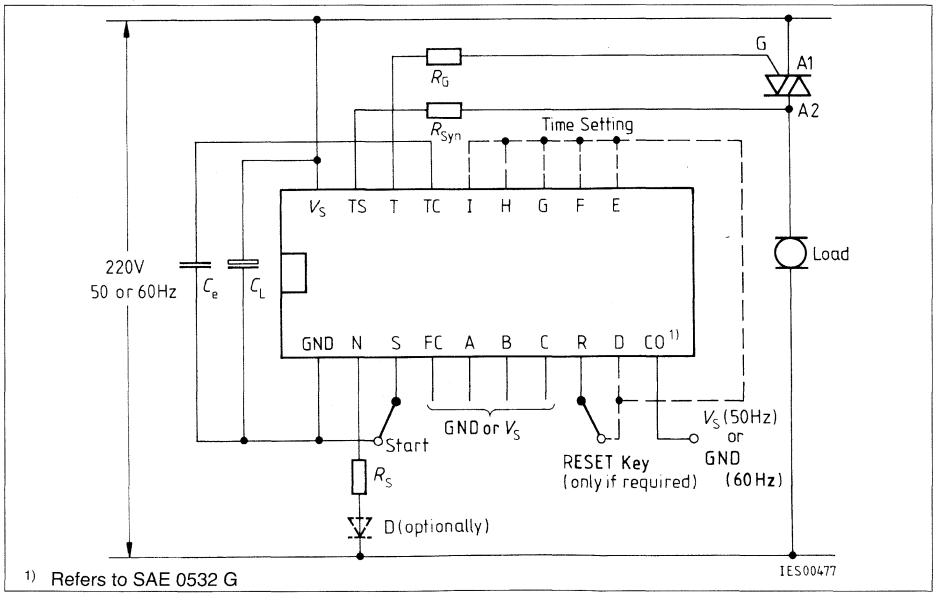


* The symbol in parentheses applies to SAE 0532.
** The external wiring of pins FC to R equals to that of pin S (Test Circuit 2)

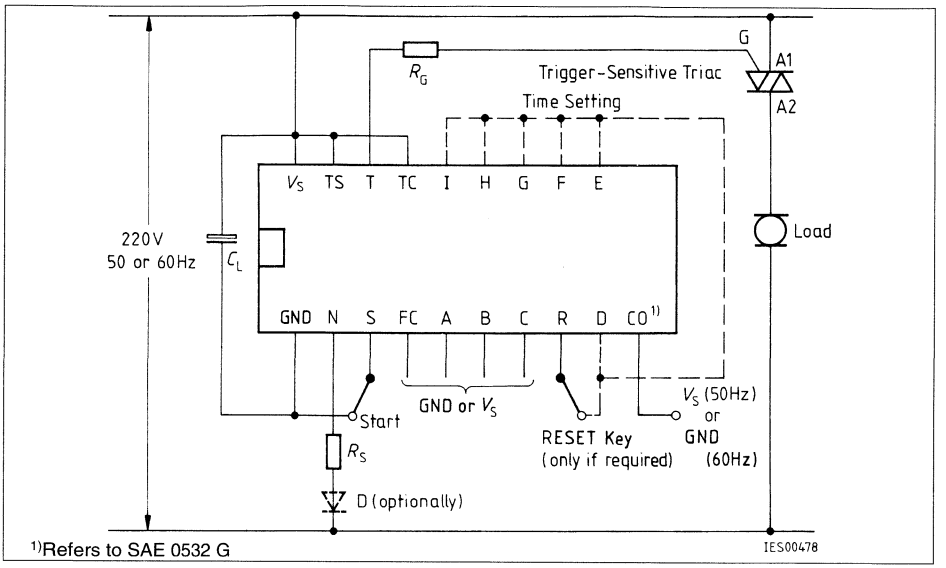
Test Circuit 2



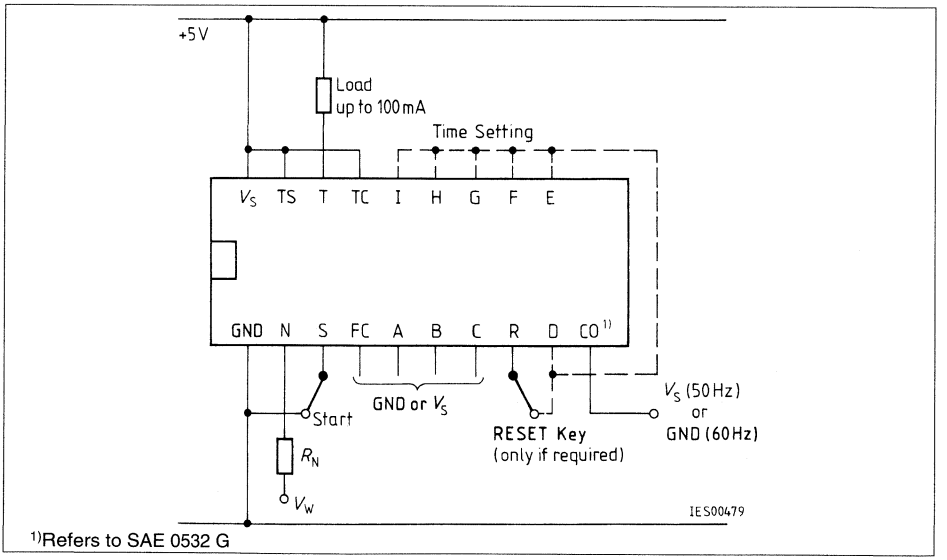
Application Circuit 1
Operation with resistive load



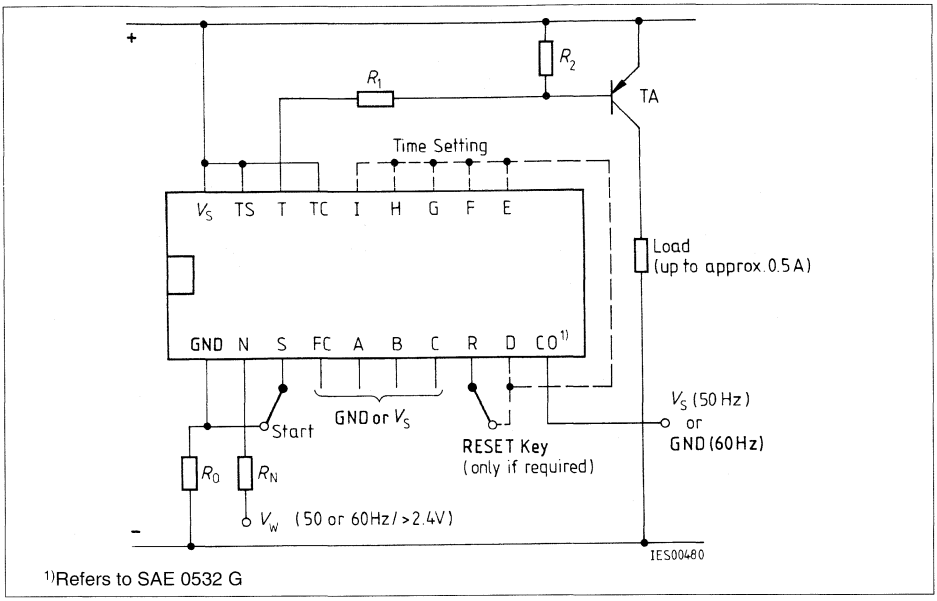
Application Circuit 2
Operation with resistive, capacitive and inductive load



Application Circuit 3
Operation with any load and continuous triac triggering

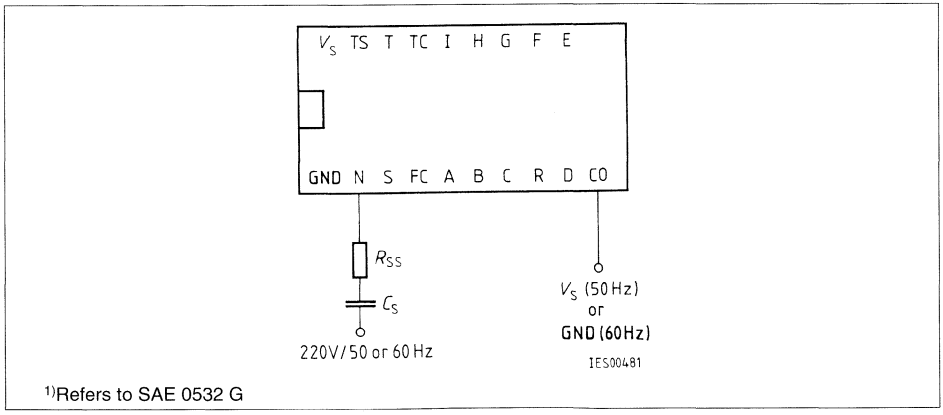


Application Circuit 4
Operation with 5-V DC voltage



1) Refers to SAE 0532 G

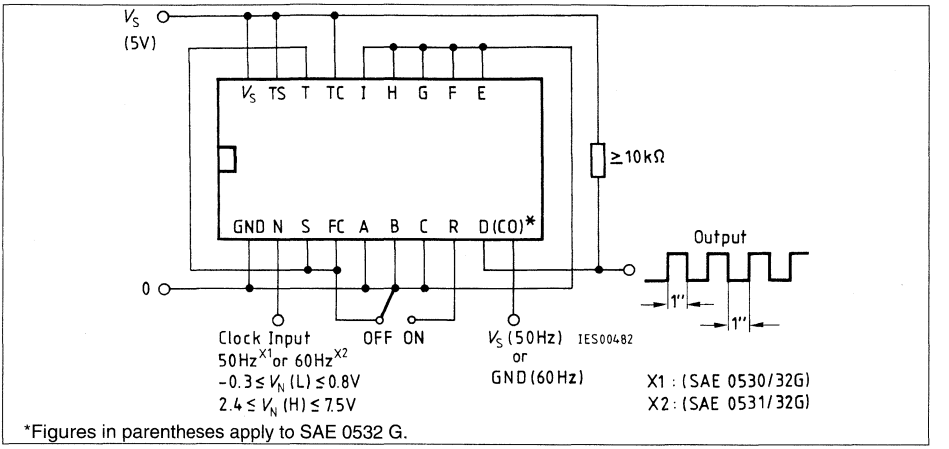
Application Circuit 5
Operation with DC voltage > 5.5 V



1) Refers to SAE 0532 G

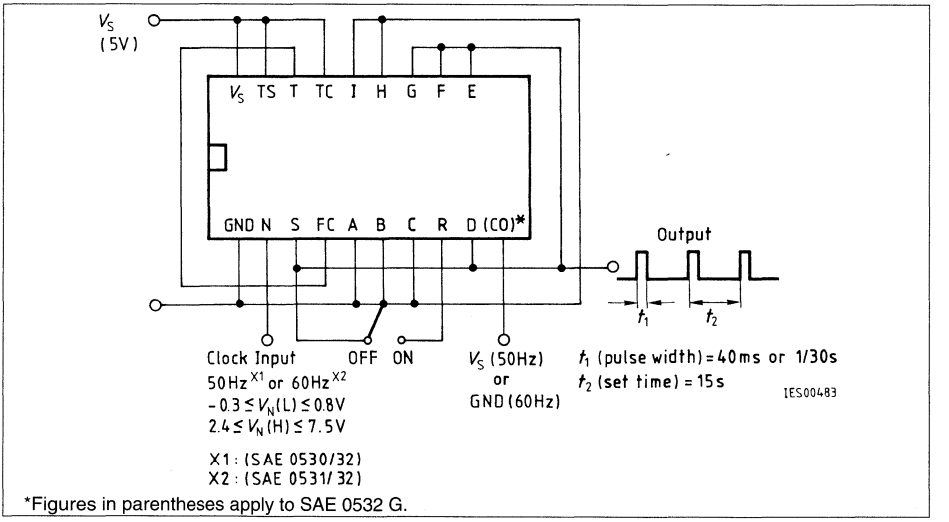
Application Circuit 6
Operation with capacitive series resistor

In the application circuits 1 to 3 a series connection of R and C may be utilized instead of R_S or R_S and D.



*Figures in parentheses apply to SAE 0532 G.

Application Circuit 7
Squarewave Generator Pulse Generator



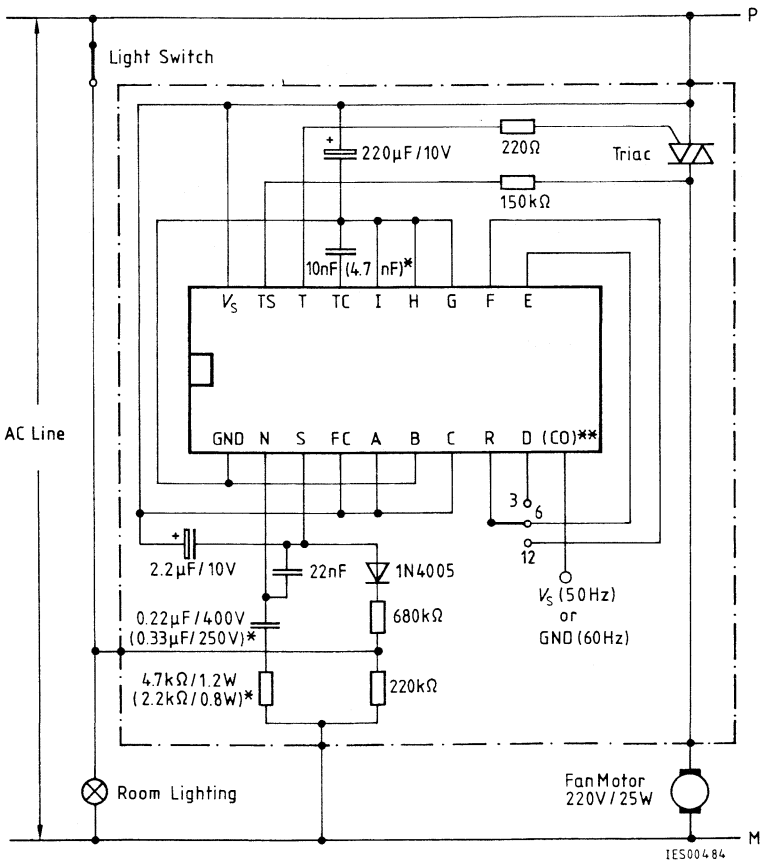
*Figures in parentheses apply to SAE 0532 G.

Application Circuit 8
Pulse Generator

Note:

The pulse width t_1 is determined only by the clock frequency f = 50 Hz (SAE 0530/32 G) or f = 60 Hz (SAE 0531/32 G) on input N: for 50/60 Hz: $t_1 = 2/f = 2/50$ (or 2/60) = 40 ms (or 1/30 s). Immediately after turn-on the first pulse t_1 and accordingly the first cycle t_2 can be up to 20 ms (or 1/60 s) shorter (according to the phase of the 50-Hz or 60-Hz network).

After turn-on output T conducts and stays on L potential throughout operation.



* Figures in parentheses apply to 60-Hz mode (SAE 0531/32 G), all other figures to 50-Hz mode (SAE 0530/32 G).
** Figures in parentheses apply to SAE 0532 G.

Application Circuit 9
Timing Control for Ventilator
(Adjustable to 3, 6 or 12 min follow-up)

Function of Circuit

The fan motor starts up when the room lighting is turned on and switches itself off automatically 3 (6 or 12) ** minutes after the lighting is turned off.

Dimensioning of Application Circuits

The following equations provide guideline values for operation with sinusoidal alternating voltages of 50 Hz (SAE 0530/32 G) or 60 Hz (SAE 0531/32 G). The firing of the triac always occurs in the 2nd and 3rd quadrant (negative trigger current).

$$\text{T (trigger-pulse length)} = \frac{5\ (4.18)^{*)} \times \text{holding current}}{\text{rms load current}}\ \text{[ms]}\quad (\text{for } T \leq 1.5\,\text{ms})$$

$$R_G = \frac{V_S - V_{TL} - \text{trigger voltage}}{\text{trigger current}}$$

$$R_V = \frac{0.5 \times \text{rms line voltage} - V_S}{I_S + \text{averaged trigger current}}\quad (\text{with or without diode D})$$

Averaged trigger current = 0.1 (0.12)*) × trigger current × T (T in ms)

$$\text{Dissipation on } R_V \text{ (without diode D)} = \frac{(\text{rms line voltage})^2}{R_V}$$

$$\text{Dissipation on } R_V \text{ (with diode D)} = \frac{0.5 \times (\text{rms line voltage})^2}{R_V}$$

$$C_L = \frac{20\ (17)^{*)} \times \text{rms line voltage}}{R_V}\ [\mu\text{F, V, k}\Omega]\ (\text{residual AC voltage on } V_S \leq 0.5\,V_{pp})^{***)}$$

Application Circuit 1 (voltage synchronization for resistive load)

$$R_{syn} = \frac{0.22\ (0.27)^{*)}\ T \times \text{rms line voltage} - 1.3}{0.025} \geq \frac{\text{peak line voltage}}{4}$$

[kΩ, V, ms] (for T ≤ 1.5 ms)

Application Circuit 2 (current synchronization)

$C_e = 16.7 \times T\ [\text{nF, ms}]^{***)}$

$$R_{syn}{}^{**)} \geq \frac{\text{max. forward voltage} - 1.3}{I_{TSmin}}\ [\text{k}\Omega, \text{V, mA}]$$

$$R_{syn}{}^{**)} \geq \frac{\text{peak line voltage}}{4}\ [\text{k}\Omega, \text{V}]$$

$$R_{syn} \leq \frac{\text{trigger voltage} - 1.3}{I_{TSmax}}\ [\text{k}\Omega, \text{V, mA}]^{***)}$$

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32 G).
**) The larger value applies.
***) See application notes.

Application Circuit 3

See R_G, R_V, C_L

Application Circuit 4

The level of the AC voltage V_{ac} must be greater than 2.4 V_p.
$R_N \approx 5 \times V_{ac} + 5$ [kΩ, V_p]

Application Circuit 5

V_{ac}, R_N: see application circuit 4 (V_{ac} referred to pin 0)

$$R_0 = \frac{V_S - 5.5}{I_S + I_{R1}}$$

$$R_1 = \frac{5.5 - V_{TL} - V_{B\,(TA)}}{I_{R1}}$$

$$R_2 = \frac{V_{B\,(TA)}}{I_{R2}}$$

$I_{R1} = I_{B\,(TA)} + I_{R2}$
$I_{R2} \approx 0.05 \times I_{B\,(TA)}$

Application Circuit 6

$$C_V \approx \frac{4\ (3.3)^{*)}}{R_V}\ [\mu F, k\Omega]$$

$R_{VV} = 0.2 \times R_V$**)

*) Figures in parentheses apply to 60-Hz version (SAE 0531/32 G).
**) See application notes.

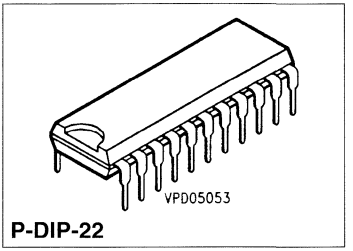
SIEMENS

Video-Pulse Generator — TBB 278 B

Preliminary Data — **CMOS**

Features

- Free-running or external synchronization
- External synchronization optionally with S signal and PLL or with basic timing signal t_0 and frame reset signal
- Parallel or serial programming
- Line interlacing can be disabled
- Parallel programming:
  - 16 systems with firmly assigned line numbers and pulse widths (CCIR 624-3, EIA RS 343 A, CCIR AZ 11, HDTV and others)
- Serial programming:
  - Line number per field selectable between 1 and 4095
  - Pulse widths selectable in steps
  - Identification signals for PAL, PAL-M, SECAM and NTSC color systems
  - Equalizing signals and V_{sync}-interruptors can be disabled
  - TLL-compatible serial interface
  - Power-on reset on PAL system



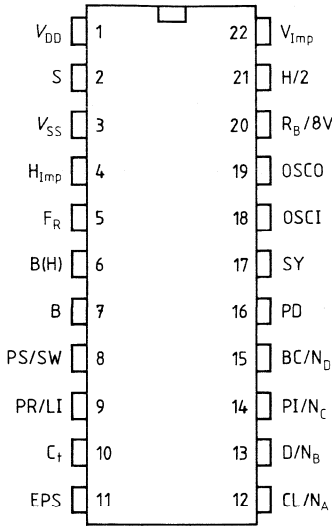
P-DIP-22

Type	Ordering Code	Package
S▼ TBB 278 B	Q67100-H8759	P-DIP-22

▼ New type

The TBB 278 B video-pulse generator is an LSI circuit generating the sync, control and color-subcarrier-window signals that are necessary for controlling cameras, monitors, mixing consoles and similar items of equipment. Up to 4095 lines and the pulse widths of output signals can be serially programmed. Alternatively to serial programming, 16 standards or systems based on standards can be selected on a parallel interface or by switches or hardwiring.

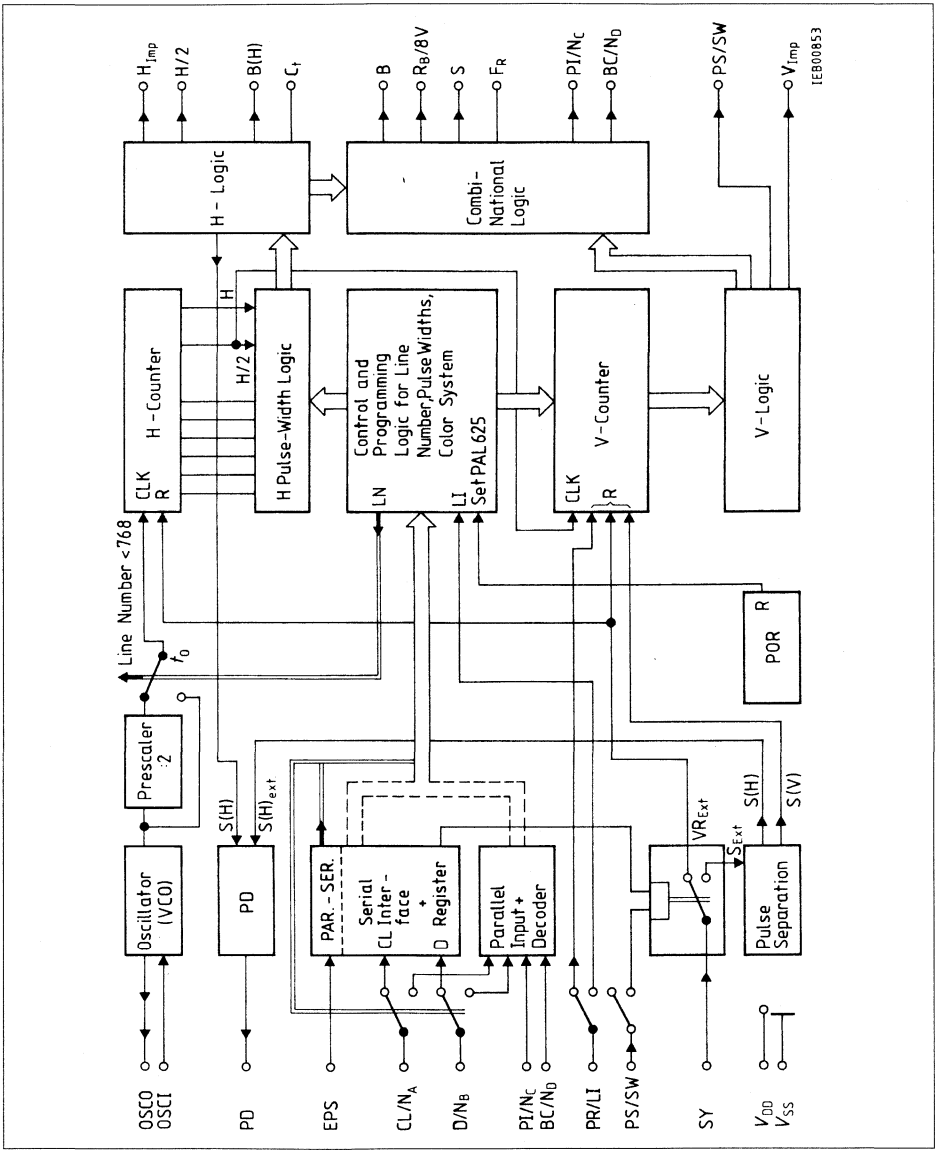
Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	Supply voltage
3	V_{SS}	Ground
19	OSCO	Crystal connection/ext. clock
18	OSCI	Crystal connection
16	PD	PLL output
12	CL/N_A	Clock/parallel programm. input
13	D/N_B	Data/parallel programm. input
11	EPS	Parallel/serial programming switchover, transfer to serial latch
17	SY	Ext. sync signal input
4	H_{Imp}	Horizontal pulse (line freq.)
21	H/2	Double line frequency
6	B(H)	Horizontal blanking pulse
10	C_t	Clamping pulse
7	B	Blanking signal
20	R_B/8 V	Vidicon blanking signal output/ output for color-subcarrier-phase identification signal
2	S	Sync signal
5	F_R	Frame reset signal
22	V_{Imp}	Vertical pulse
14	PI/N_C	Output for PAL identification pulse or SECAM identification/ parallel programming input
15	BC/N_D	Burst window output (PAL, PAL-M, NTSC), color-subcarrier blanking-window output (SECAM)/ parallel programming input
8	PS/SW	PAL squarewave output/input for external sync selection
9	PR/LI	Reset input for PAL square on 1st field, set input for S9, S10 on 4th field/ disactivate line interlacing

8



Block Diagram

Functional Description

The block diagram illustrates the basic design of the circuit.

The TBB 278 B is parallelly or serially programmed according to the level on pin EPS. Pins with names separated by a slash have a different function for parallel and serial programming.

Parallel Programming (EPS = High)

16 systems can be selected with firmly assigned numbers of lines and pulse widths (**see tables 1 and 2**).

Pins CL/N_A, D/N_B, PI/N_C, BC/N_D, PS/SW and PR/LI are activated as parallel programming inputs. In addition to the PS/SW selection of the sync mode, the line interlacing PR/LI can also be freely selected for all 16 programs (**see table 1**). In systems S9 and S10 four fields have the standard line numbers 1023 and 1249, respectively. (Because of the odd number of lines the fourth field has a different number of lines to the preceeding three fields.)

Apart from the input signal PS/SW, which is effective immediately, parallel systems newly programmed with PR/LI, CL/N_A, etc are not adopted until the following (internal) F_R pulse occurs, i.e. the TBB 278 B does not start to operate according to the new system until the beginning of the next frame.

The sync input signals SY and PR/LI (PR only for S9, S10) are effective immediately (**see figure 1**).

8

Serial Programming (EPS = Low)

It is possible to design systems with any line numbers and pulse widths (**see table 3**). Pins CL/N_A and D/N_B are activated as serial programming inputs, PI/N_C, BC/N_D, PS/SW and R_B/8V as color-identification signal outputs and PR/LI as a PAL square reset input.

The power-on reset automatically programs the serial register to the PAL-system with 625 lines/frame. Another system can be written in with shift clock CL/N_A and data D/N_B, and transfer by the following (internal) F_R pulse can be activated with a short high-pulse on pin EPS. (A high pulse that is substantially longer than 5 µs will switch the TBB 278 B to "parallel", but the information in the shift register will not be lost.) As in the parallel mode, the TBB 278 B does not start to operate according to the new system until the beginning of the next frame.

Only the sync selection bit # 1 is effective immediately with the EPS high edge, and likewise of course the sync input signals SY and PR/LI (**see figure 3**).

Serial Coding Comprises a Total of 71 Bits:

12 bits	2^0 thru 2^{11}	for line number per field, 1-4095
3 bits		for selecting color system
47 bits		for flexible setting of pulse widths and delays of horizontal and vertical output signals as multiples of oscillator basic timing t_o or of line period H.
6 bits		number of equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without equalizing pulses and V_{sync}-interrupt pulses
1 bit		with or without line interlacing
1 bit		for selecting synchronization mode N_B : for external timing = master timing, intern. osc. is disabled.

Functional Description
Systems Selectable on Parallel Interface

System	Lines/Frame	Field/Frame Freq.	Standard
S1	625	50/25	CCIR report 624-3
S2	525	60/30	CCIR report 624-3
S3	735	60/30	Based on EIA RS 343 A
S4	875	50/25	Based on CCIR
S5	1125	60/30	HDTV Japan
S6	1023	60/30	EIA RS 343 A
S7	1249	50/25	Based on EIA RS 343 A
S8	1249	80/40	Flickerfree monitors
S9	3 × 256 1 × 255	120	Progressive scanning
S10	3 × 312 1 × 313	100	Progressive scanning
S11	1023	30	Progressive scanning
S12	1249	25	Progressive scanning
S13	2046	3	High-definition progressive scanning
S14	2498	2.5	High-definition progressive scanning
S15	1251	50/25	Based on EIA RS 343 A
S16	1125	60/30	CCIR report AZ 11

Absolute Maximum Ratings
$T_A = -25$ to 75 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input voltage	V_I	− 0.3	V_{DD} + 0.3	V
Supply voltage	V_{DD}	− 0.3	6	V
Storage temperature	T_{stg}	− 50	125	°C
Total power dissipation Power dissipation per output	P_{tot} P_Q		500 50	mW mW

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output load)	I_{DD}			5	mA
Operating frequency	f_{OSC}			15	MHz
Ambient temperature	T_A	− 25		75	°C

DC Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inputs						
PI/N_C, BC/N_D SY, PS/SW, OSCI, OSCO						(OSCO for ext. clock)
H-input voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		0.3 V_{DD}	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Inputs (TTL-compatible)						
EPS, CL/N_A, D/N_B						
H-input signal	V_{IH}	2		V_{DD}	V	
L-input signal	V_{IL}	V_{SS}		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_I			1	µA	
Outputs						
H/2, B(H), C_t, B PI/N_C, BC/N_D, PS/SW, R_B/8V						
H-output voltage	V_{QH}	4.5		V_{DD}	V	I_{QH} = 2.5 mA
L-output voltage	V_{QL}	0		0.5	V	I_{QL} = 2.5 mA
PD						
H-output voltage	V_{QH}	4		V_{DD}	V	I_{QH} = 100 µA
L-output voltage	V_{QL}	0		1	V	I_{QL} = 100 µA
OSCO						
H-output voltage	V_{QH}	4		V_{DD}	V	I_{QH} = 200 µA
L-output voltage	V_{QL}	0		1	V	I_{QL} = 200 µA
H_{Imp}, S, F_R; V_{Imp}						
H-output voltage	V_{QH}	4.5		V_{DD}	V	I_{QH} = 5 mA
L-output voltage	V_{QL}	0		0.5	V	I_{QL} = 5 mA

8

AC Characteristics

T_A = 25 °C

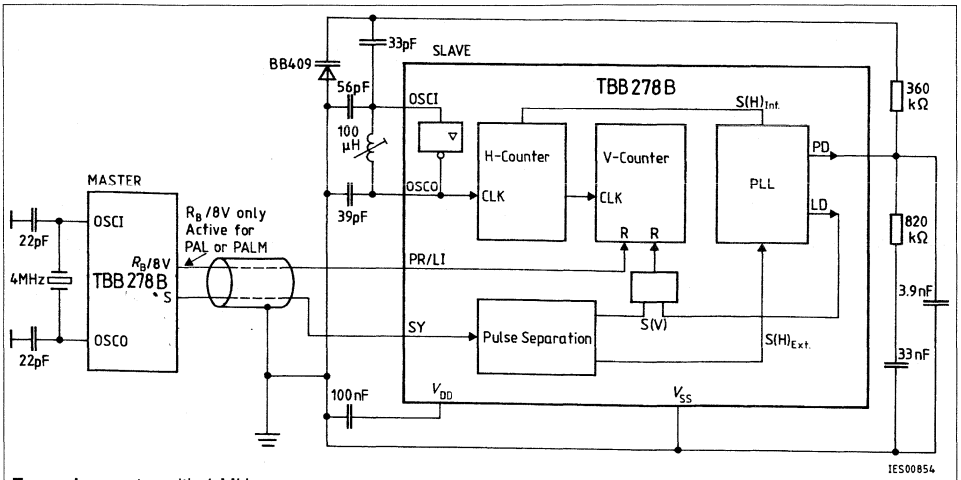
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Inputs						
CL/N_A						
Clock period	t_{CL}	1			µs	
D/N_B						
Data setup	t_{SD}	50			ns	
Data hold	t_{HD}	50			ns	
EPS						
Transfer pulse, duration	t_L			2	µs	
Propagation time	t_P			50	ns	OSCO clock edge to signal o/p
PR/LI						
PAL square reset, duration	t_{PR}	100			ns	
Outputs						
H_{Imp}, S, F_R						
Rise time	t_{LH}			15	ns	C_L = 20 pF
Fall time	t_{HL}			5	ns	C_L = 20 pF
H/2, B(H), C_t, B, V_{Imp}						
PI/N_C, BC/N_D, PS/SW, R_B/8V						
Rise time	t_{LH}			50	ns	C_L = 20 pF
Fall time	t_{HL}			20	ns	C_L = 20 pF

Synchronization

(applies to parallel and serial programming)

Synchronization of Slave with Combined S Signal

A PLL compares the phase of the internal and external S (H) pulses and adjusts the oscillator frequency accordingly. The S (V) signal resets the V counter to the beginning of the field if the phase difference between the external and internal S (H) pulse is smaller than ± 8 t_0 (see Lock Detect LD). Master and slave must be programmed for the same system (same number of lines and equalizing signals). V_{Imp}, S(V), B(V) and F_R will appear on the slaves' outputs if the line number of the master is smaller than that of the slave. The V_{Imp}, S(V), B(V) signals will be shortened by one half line.

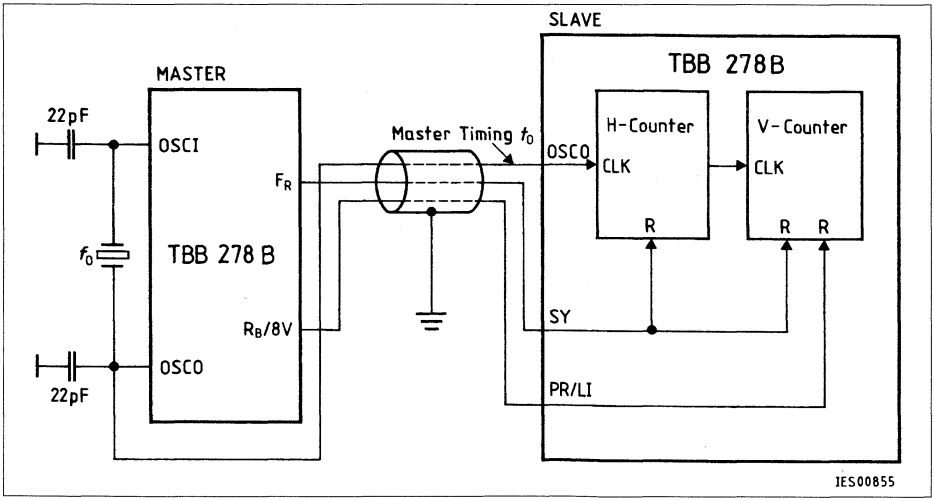


Example: master with 4-MHz crystal oscillator for PAL 625. slave with LC oscillator and PD filter.

8

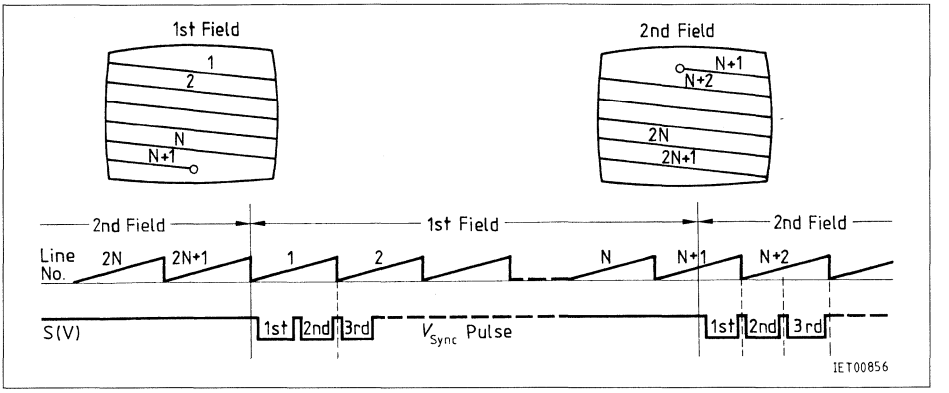
Synchronization with Master Timing and F_R Reset

Same timing: master and slave are synchronous. After any disturbance the next falling edge of F_R resets the V counter to the beginning of the frame and the H counter to the beginning of the line. The supply to the oscillator inverter is disabled and thus OSCI too.



This kind of synchronization is advisable for high-definition systems because less jitter is produced than with the PLL.

Line Interlacing
(applies to even and odd numbers of equalizing pulses)



Systems with Line Interlacing

The 1st field begins with a whole line and ends after a half.

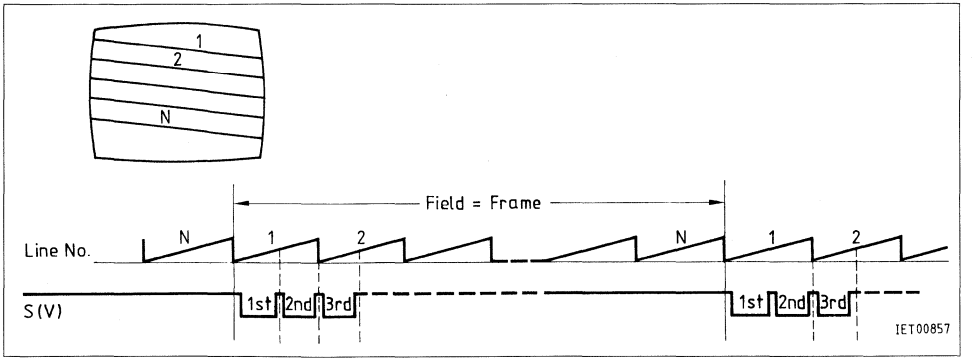
The 2nd fields begins with a half line and ends with a whole one, so it is automatically written into the spaces between the lines of the 1st field.

Both fields are initiated by the 1st V_{sync} pulse, each have (N + 1/2) lines and produce a frame of (2N + 1) lines.

(NB: Because of the finite picture flyback time the first lines of a field are not as visible as illustrated above).

Systems without Line Interlacing

The same field is written each time, into the same raster as the previous one. The field begins and ends with a whole line.



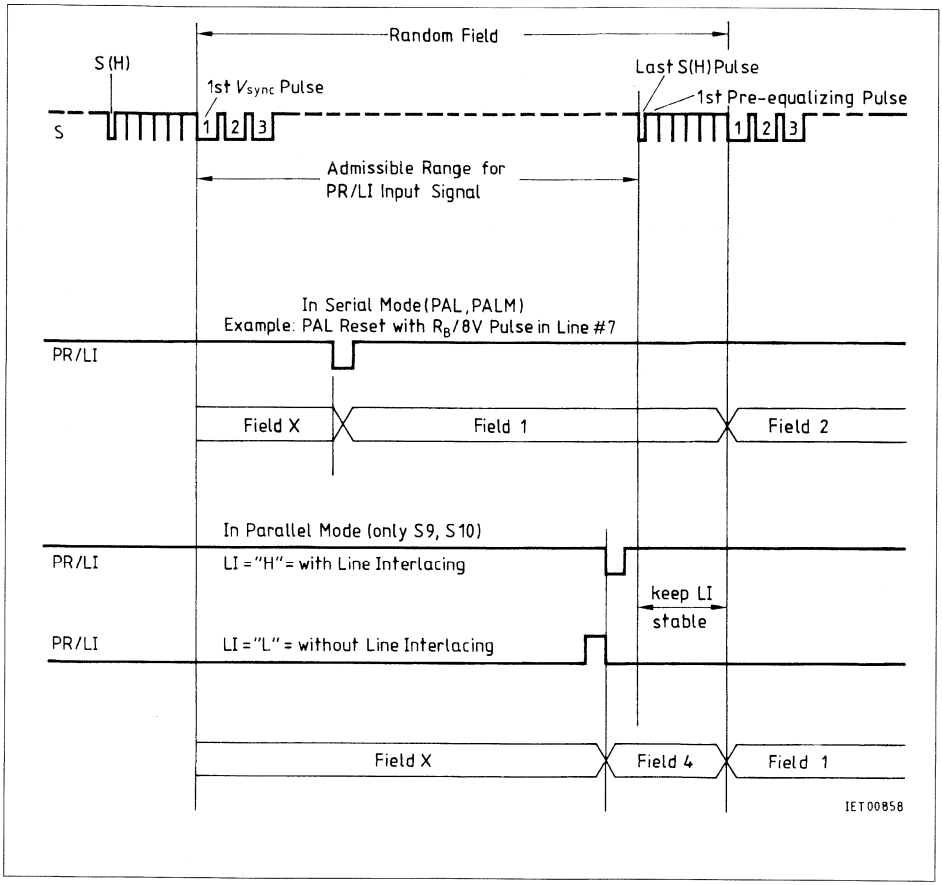


Figure 1
Timing Diagram for PR/LI Signal

8

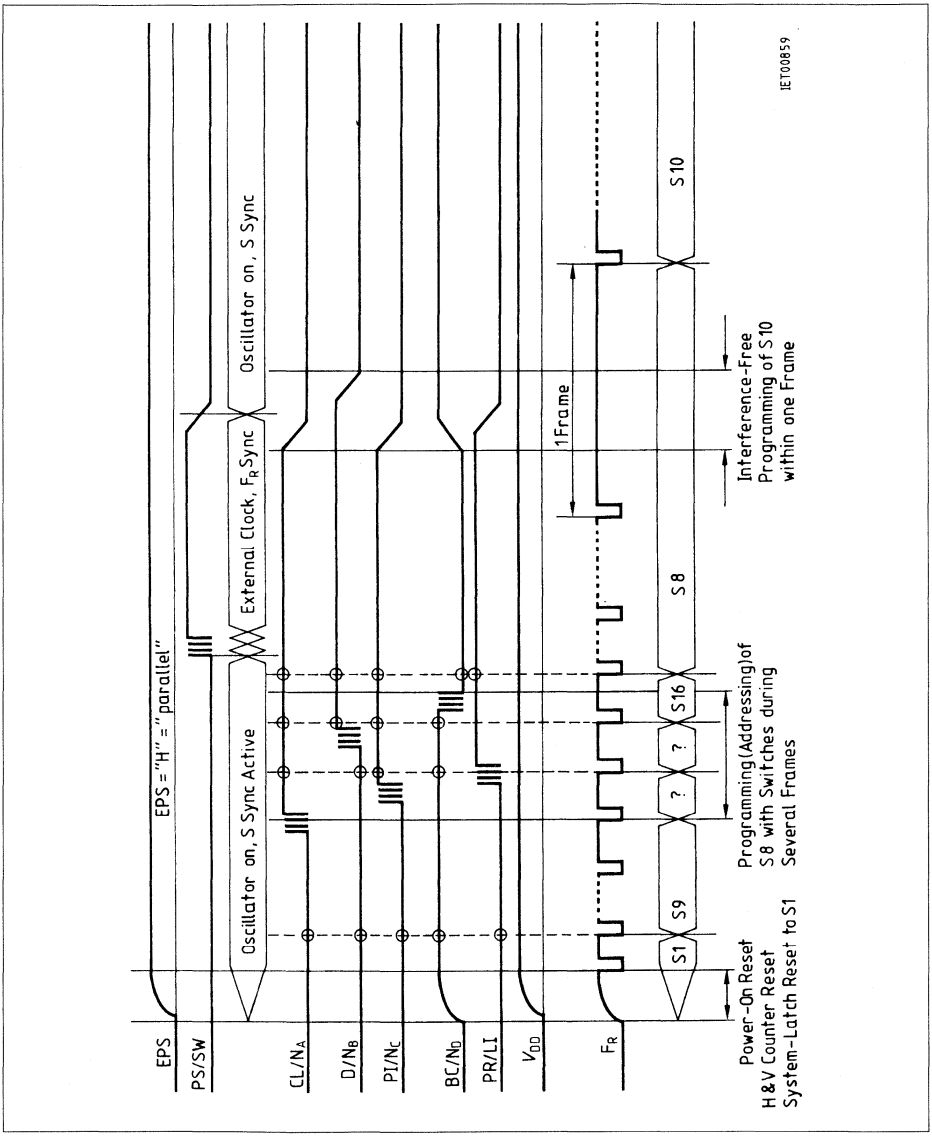


Figure 2
Pulse Diagram for Parallel Programming

Table 1
Parallel Programming

System	Lines per frame	Lines per field	Picture Frequency/Hz frame	Picture Frequency/Hz field	No. of Equ. & Int.	f_{osc} /MHz	f_o / $f_{\mu s}$	remarks	Coding EPS	Coding PR/ LI	Coding BC/ N_D	Coding PI/ N_C	Coding D/ N_B	Coding CL/ N_A	PS/ SW
S1	625	312 ½	25	50	5	4.000	0.5	**For LI = "L":** Number of lines/field is reduced by ½ to eliminate line interlacing.	H	H	L	L	L	L	**"H"** external clock with f_{in}-synchronization
S2	525	262 ½	30	60	6	4.032	0.49603		H	H	L	L	L	H	
S3	735	367 ½	30	60	6	5.6448	0.3543		H	H	L	L	H	L	
S4	875	437 ½	25	50	5	5.600	0.3571		H	H	L	L	H	H	
S5	1125	562 ½	30	60	10	8.640	0.23148	Frame frequency is doubled	H	H	L	H	L	L	**or "L"** Oscillator mode with S-synchronization
S6	1023	511 ½	30	60	6	3.92832	0.2546		H	H	L	H	L	H	
S7	1249	624 ½	25	50	6	3.9968	0.2502		H	H	L	H	H	L	
S8	1249	624 ½	40	80	none	12.7898	0.1564		H	H	L	H	H	H	
S9	3 × 256, 1 × 255		120		6	3.92832	0.2556	**for LI = "H":** Number of lines/field is reduced by ½	H	L*)	H	L	L	L	
S10	3 × 312, 1 × 313		100		6	3.9968	0.2502		H	L*)	H	L	L	H	
S11	1023		30		12	3.9283	0.2546	**for LI = "H":** Number of lines/field is increased by ½ to produce line interlacing	H	L	H	L	H	L	
S12	1249		25		12	3.9968	0.2502		H	L	H	L	H	H	
S13	2046		3		24	0.785664	1.2728		H	L	H	H	L	L	
S14	2498		2.5		24	0.79936	1.251		H	L	H	H	L	H	
S15	1251	625 ½	25	50	6	3.9968	0.2502	**For LI = "L":** like in S1 thru S8	H	H	H	H	H	L	
S16	1125	562 ½	30	60	10	8.64	0.23148		H	H	H	H	H	H	

*) PR/LI: falling edge sets TBB 278 B to 1rst field

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Table 2
Pulse Widths for Systems Selectable in Parallel Mode

Parallel system / Output signals		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Lines/frame		625	525	735	875	1125	1023	1249	1249	3×256 1×255	3×312 1×313	1023	1249	2046	2498	1251	1125
Frame frequency	/Hz	25	30	30	25	30	30	25	40	120	100	30	25	3	2.5	25	30
field frequency	/Hz	50	60	60	50	60	60	50	80	–	–	–	–	–	–	50	60
H line period	/µs	64	63.492	45.35	45.71	–	32.58	32.02	–	32.58	32.02	32.583	32.025	162.92	160.12	32.026	29.629
Line frequency	/KHz	15.625	15.750	22.05	21.877	33.75	30.69	37.224	49.95	30.69	31.22	30.69	31.226	6.138	6.245	31.224	33.75
f_o = H/128 = 1/t_o	/µs	.500	.49603	.3543	.3571	.23148	.2546	.2502	.1564	.2556	.2502	.2546	.2502	1.2728	1.251	.2502	.23148
f_{OSC}	/MHz	4.000	4.032	5.6448	5.600	8.64	3.92832	3.9968	12.7898	3.92832	3.9968	3.9283	3.9968	0.785664	0.79936	3.9968	8.64
t_{OSC} = 1/f_{OSC} [1]		0.5 to	0.5 to	0.5 to	0.5 to	0.5 to	to	to	0.5 to	to	to	to	to	to	to	to	0.5 to
Blanking signal	B(H)	24 to	22 to	20 to	24 to	26 to	28 to	24 to	34 to	28 to	24 to	28 to	24 to	28 to	24 to	24 to	16 to
	B(V)	25 H	20 H	30 H	30 H	42 H	39 H		40 H	20 H		80 H		160 H		39 H	45 H
Vidicon blanking signal	RB(H)	19 to	19 to	19 to	19 to	–	19 to		–	–	–	–	–	–	–	19 to	–
	RB(V)	15 H	15 H	20 H	20 H	–	30 H		–	–	–	–	–	–	–	30 H	–
Front porch	D	3 to	3 to	3 to	3 to	3 to	3 to	3 to	3 to	3 to	3 to	3 to		3 to		3 to	3 to
H-pulse		14 to	13 to	14 to	14 to	10 to	10 to	10 to	10 to	10 to	10 to	10 to		10 to		10 to	10 to
V-pulse		10 H	9.5 H	14.5 H	15 H	5 H	20 H	20 H	20 H	10 H	10 H	40 H		80 H		20 H	20 H
Clamping pulse	C_1	2 to	3 to	2 to	2 to	3 to	3 to	3 to	–	3 to	3 to	3 to		3 to		3 to	2 to
C_1 delay	DC_1	17 to	16 to	17 to	17 to	13 to	20 to	20 to	–	20 to	20 to	20 to		20 to		20 to	13 to
S signal	S(H)	9.5 to	9.5 to	7 to	7 to	10 to	11 to	11 to	10 to	10 to	10 to	10 to		10 to		11 to	2.5 to
Equalizing pulse	Equ.	4.5 to	4.5 to	4 to	4 to	5 to	5 to	5 to	–	4 to	4 to	4 to		4 to		5 to	2.5 to
V_{sync} interrupt	Int.	9.5 to	9.5 to	7 to	7 to	9 to	8 to	8 to	10 to[2]	7 to	7 to	7 to		7 to		8 to	3.5 to
No. of Equ. & Int. or DV$_{imp}$		5	6	6	5	10	6	6	–	6		12		24		6	10
		2.5 H	3 H	3 H	2.5 H	5 H	3 H	3 H	5 H	3 H		6 H		12 H		3 H	5 H

$f_o = 1/t_o = 128 \times$ line number (frame) $\times$ frame frequency

1) t_{OSC} = oscillator or external clock period. Prescaler is bypassed for $t_{OSC} = t_o$ (Systems S6, S7, S9 thru S14)

2) No Equ. & Int. in middle of line. Int. corresponds to S(H) shifted. **See figures 4 and 5.**

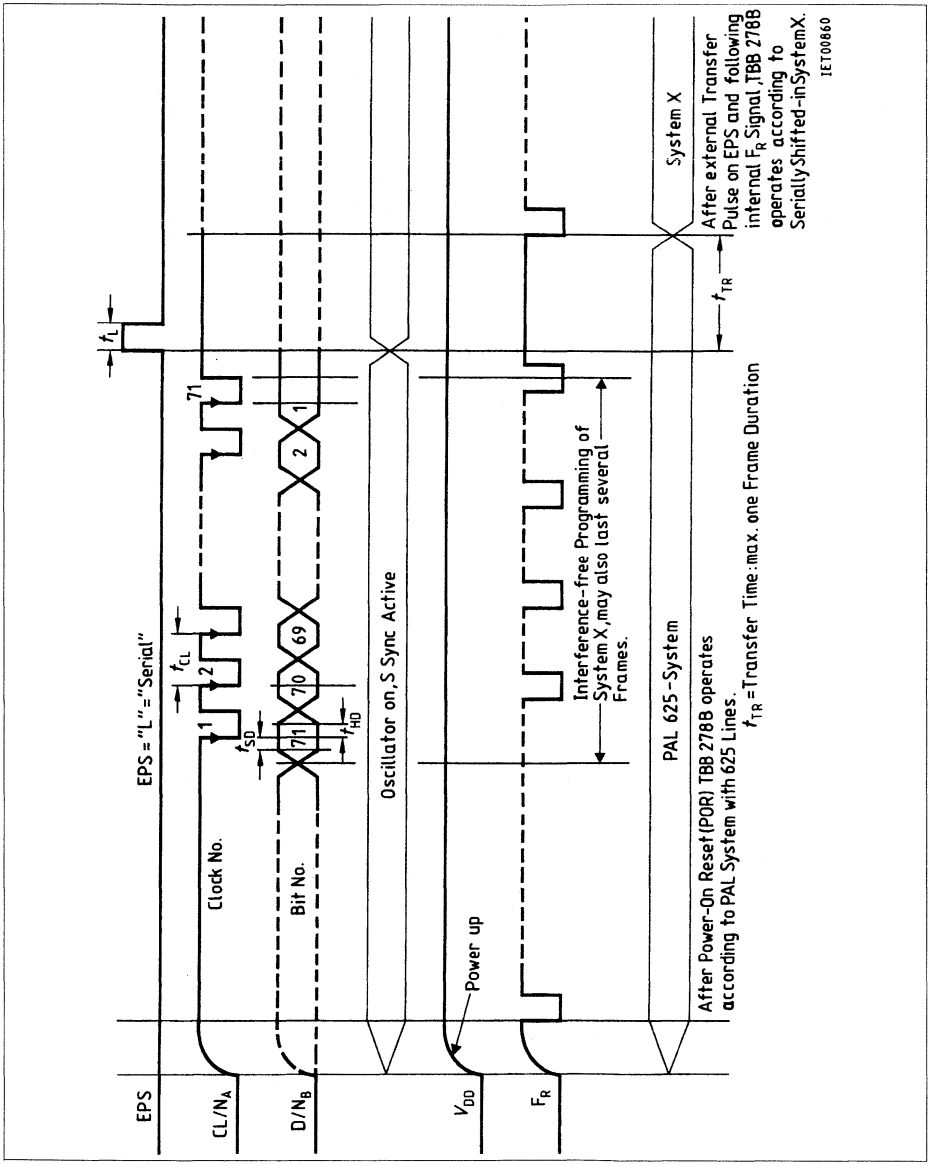

Figure 3
Pulse Diagram for Serial Programming

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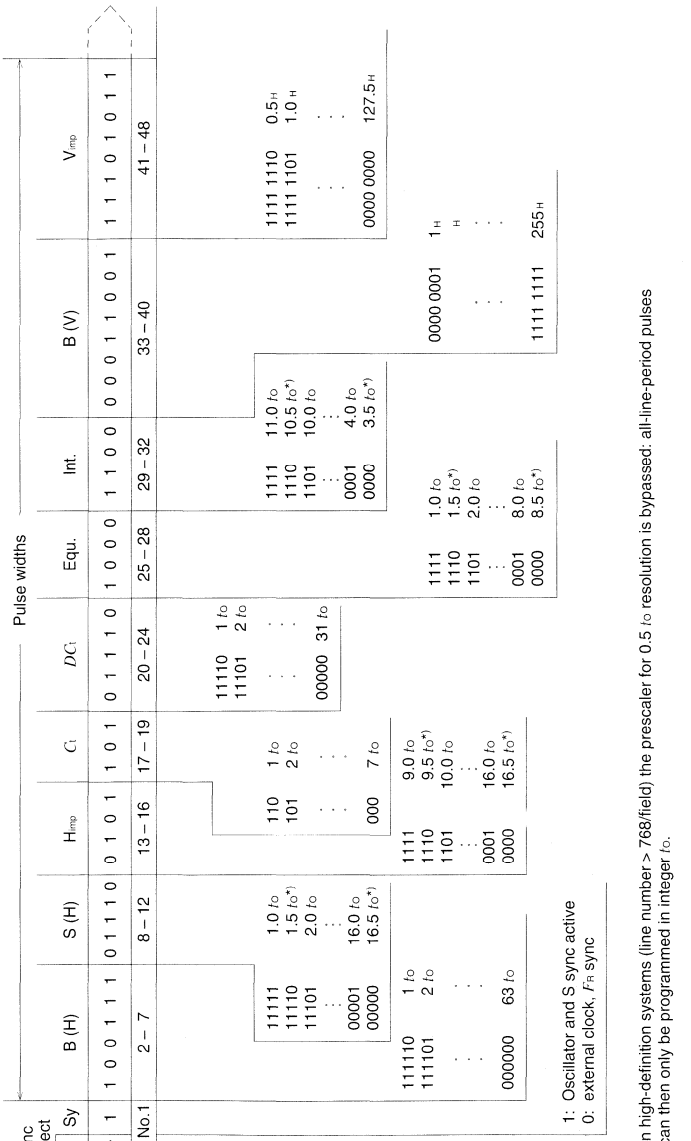
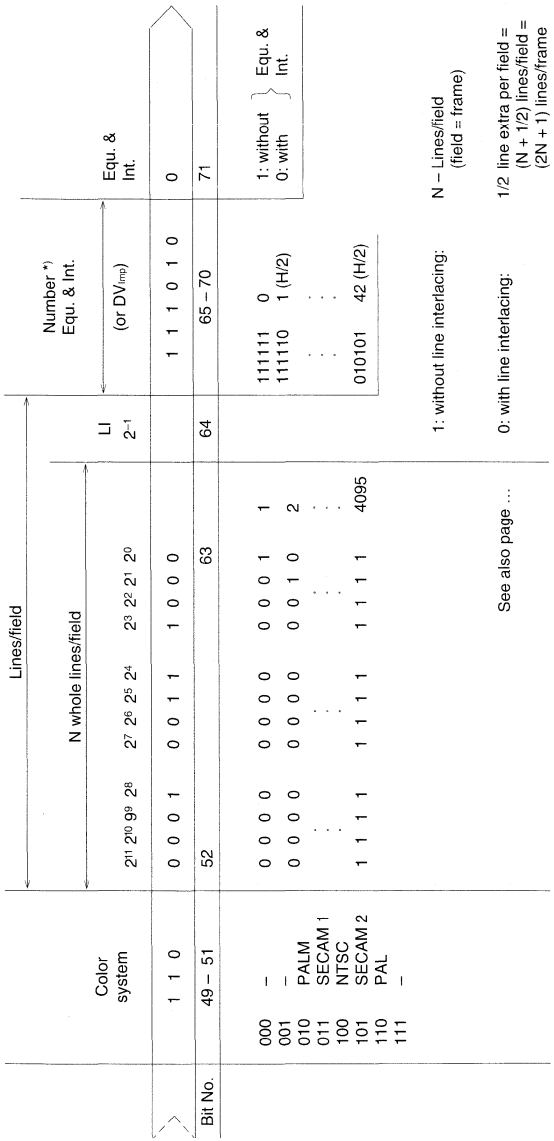
Table 3
Coding for Serial Programming

As an example the PAL system with 625 lines is entered in the register, which is written in automatically at power-on reset.



*) In high-definition systems (line number > 768/field) the prescaler for 0.5 t_O resolution is bypassed: all-line-period pulses can then only be programmed in integer t_O.

Table 3 (cont'd)
Coding for Serial Programming



*) Number Equ. & Int. = number of pre-equalizing pulses = number of V_{sync} pulses = number of post-equalizing pulses. Different numbers of equalizing and V_{sync} pulses cannot be programmed.

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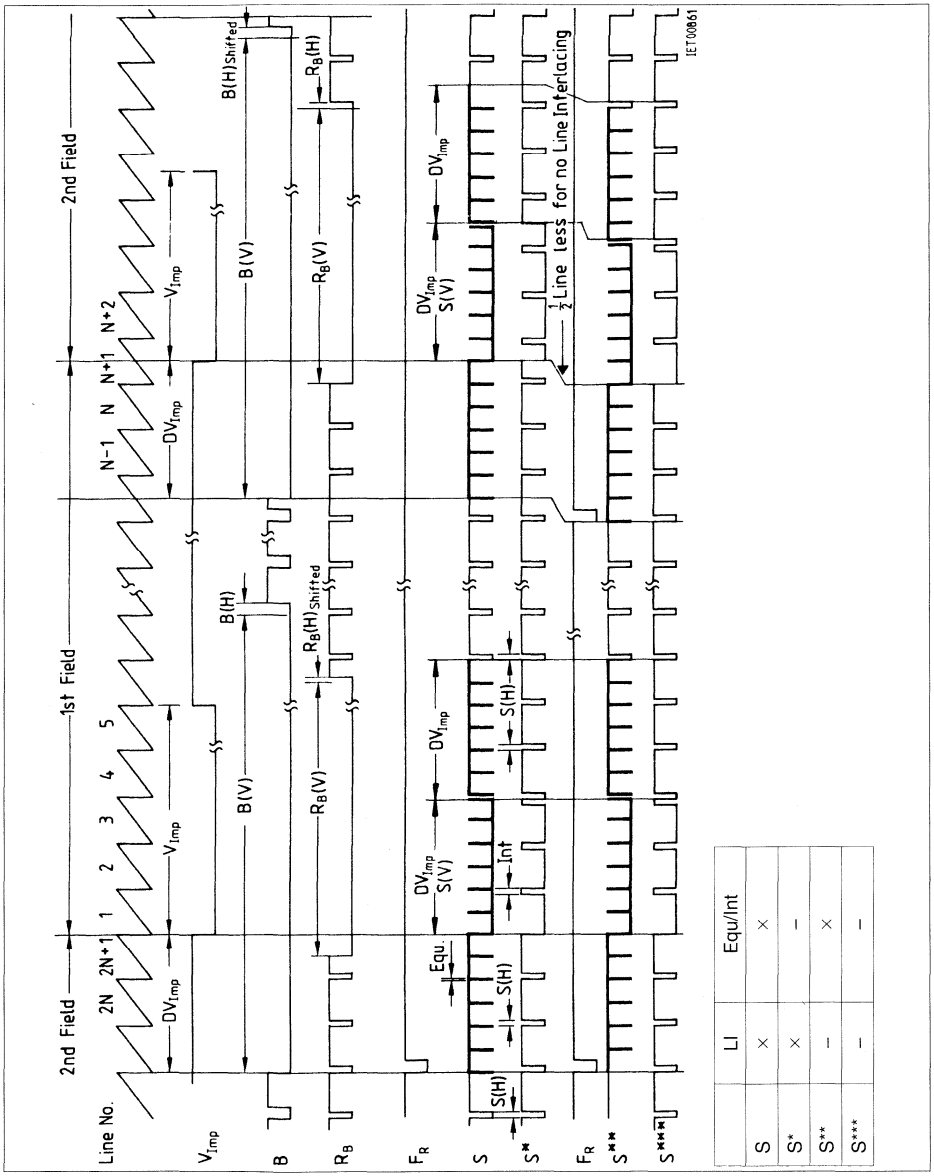

Figure 4
Composite Frame Signals for Even Number of Equalizing Pulses

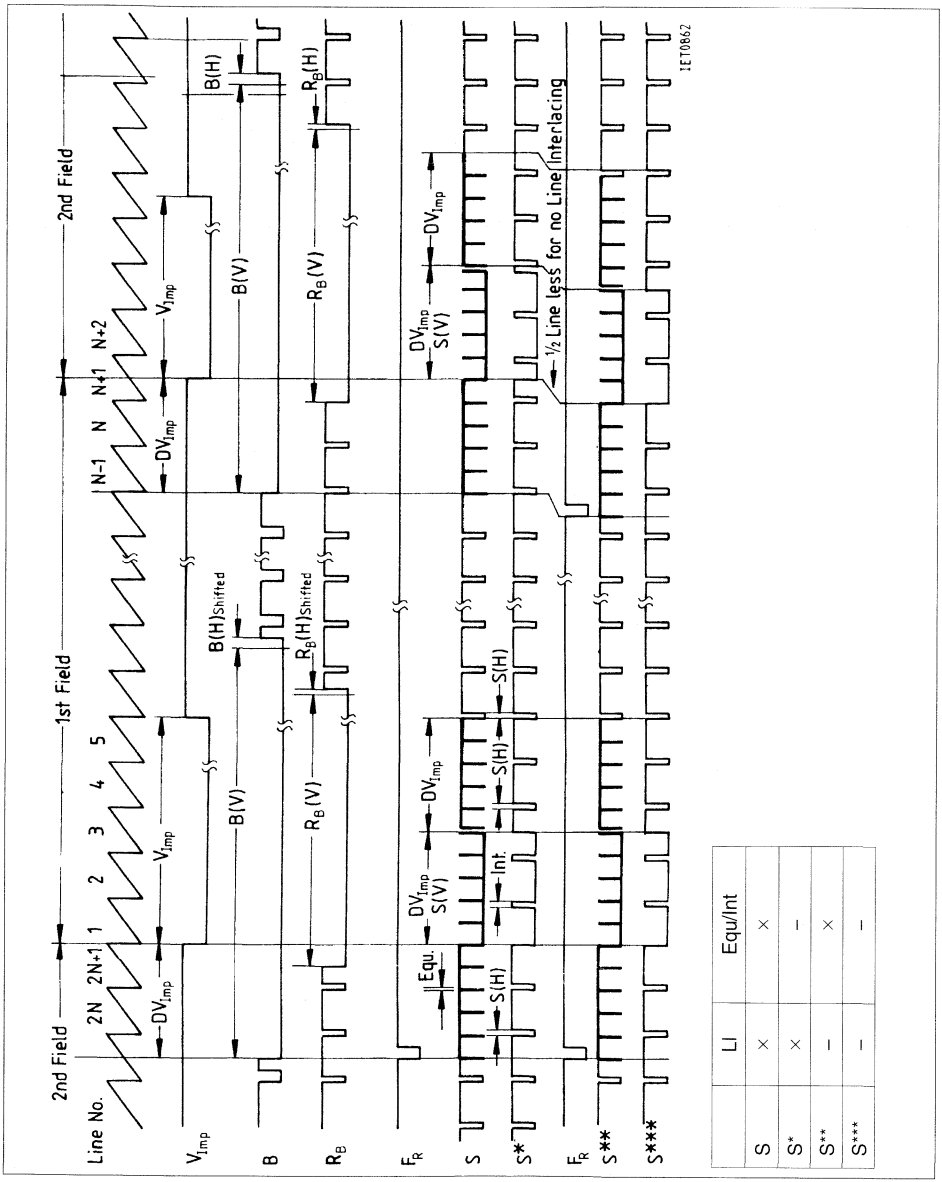

Figure 5
Composite Frame Signals for Odd Number of Equalizing Pulses

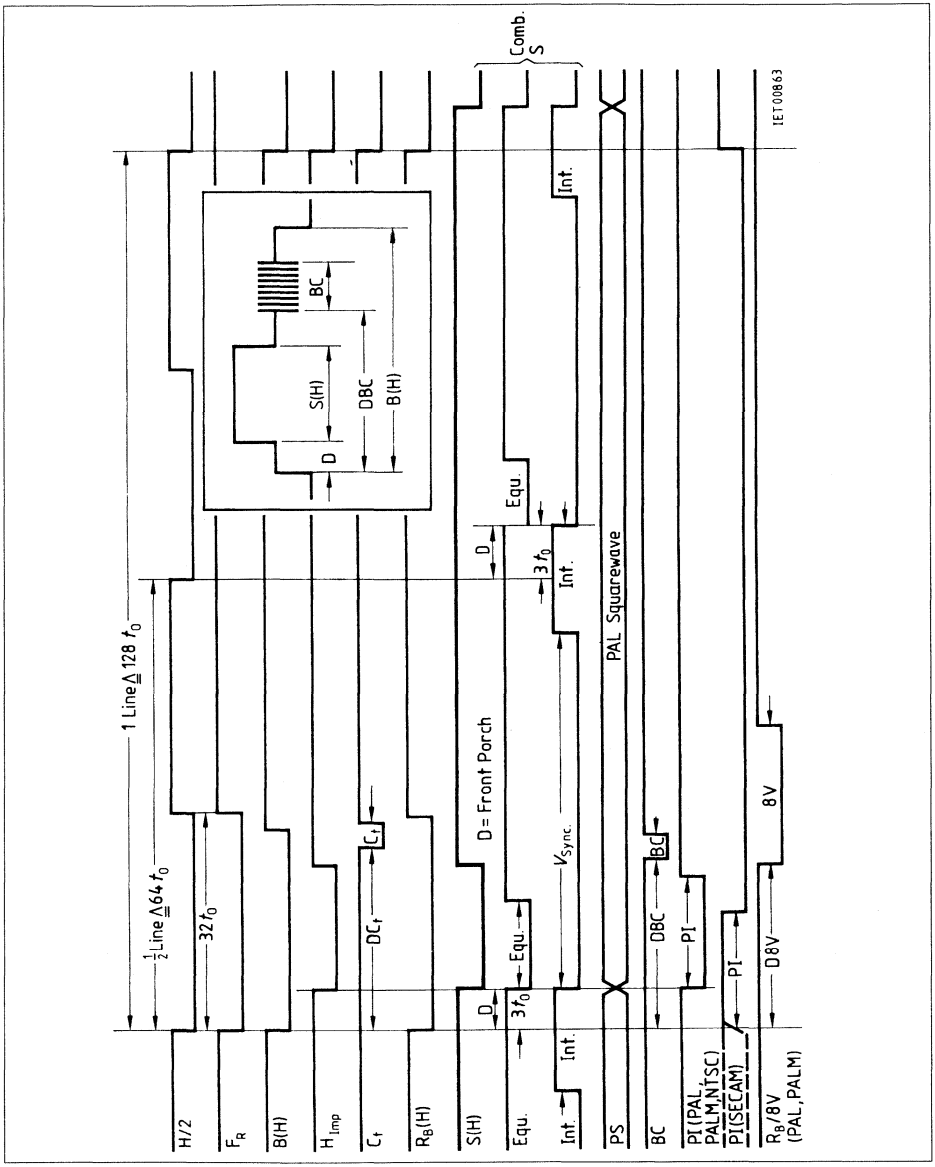

Figure 6
Line-Period Output Signals

Table 4
Pulse Widths for Auxiliary Color Signals

	PAL	SECAM	NTSC	PAL-M
S, H_{Imp}, V_{Imp}, V_R, B, B(H), C_t	refer to parallel system S1		refer to parallel system S2	
to	0.5 µs	0.5 µs	0.4965 µs	0.4965 µs
BC	2.25 µs 4.5 *to*	7.00 µs 14.0 *to*	2.5 µs 5 *to*	2.5 µs 5 *to*
DBC	7.00 µs 14.0 *to*	0	6.75 µs 13.5 *to*	7.25 µs 14.5 *to*
PI	4.75 µs 9.5 *to*	12.00 µs 24 *to*	–	4.75 µs 9.5 *to*
RB/8V	10 µs 20. *to*	–	–	10 µs 20 *to*
D8V	13.5 µs 27.0 *to*	–	–	13.5 µs 27.0 *to*
Field:		BC suppression (line number)*)		
4-1	623 ... 6	622.5 ... 22	523 ... 6	523 ... 8
1-2	310 ... 318	311. ... 335	261 ... 269	260 ... 270
2-3	622 ... 5	622.5 ... 22	523 ... 6	522 ... 7
3-4	311 ... 319	311. ... 335 **)	261 ... 269	259 ... 269

*) Assumption: line # 1 begins in all systems with the first V_{sync} pulse
**) In SECAM 1 BC appears during lines 7-15 and 320-328

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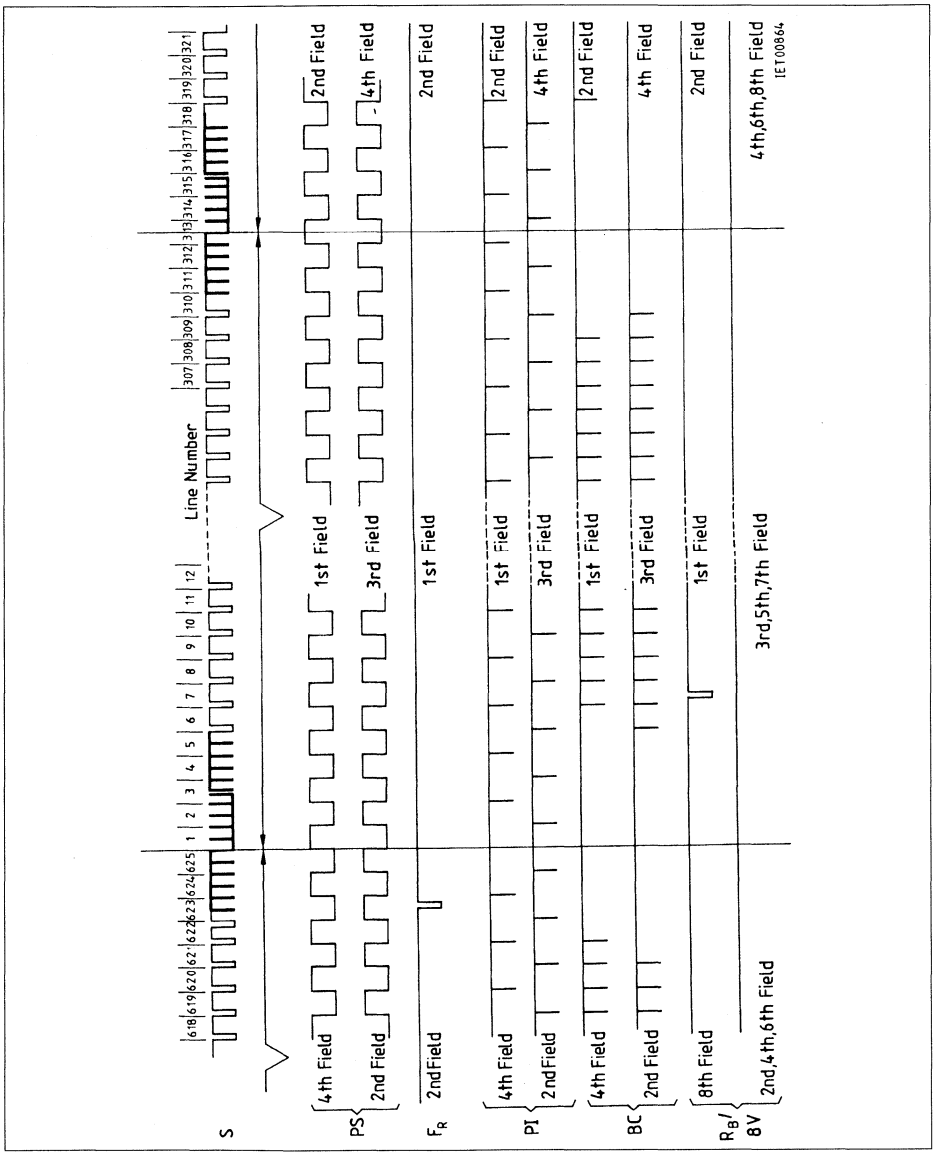


Figure 7
Color Identification Signals in PAL

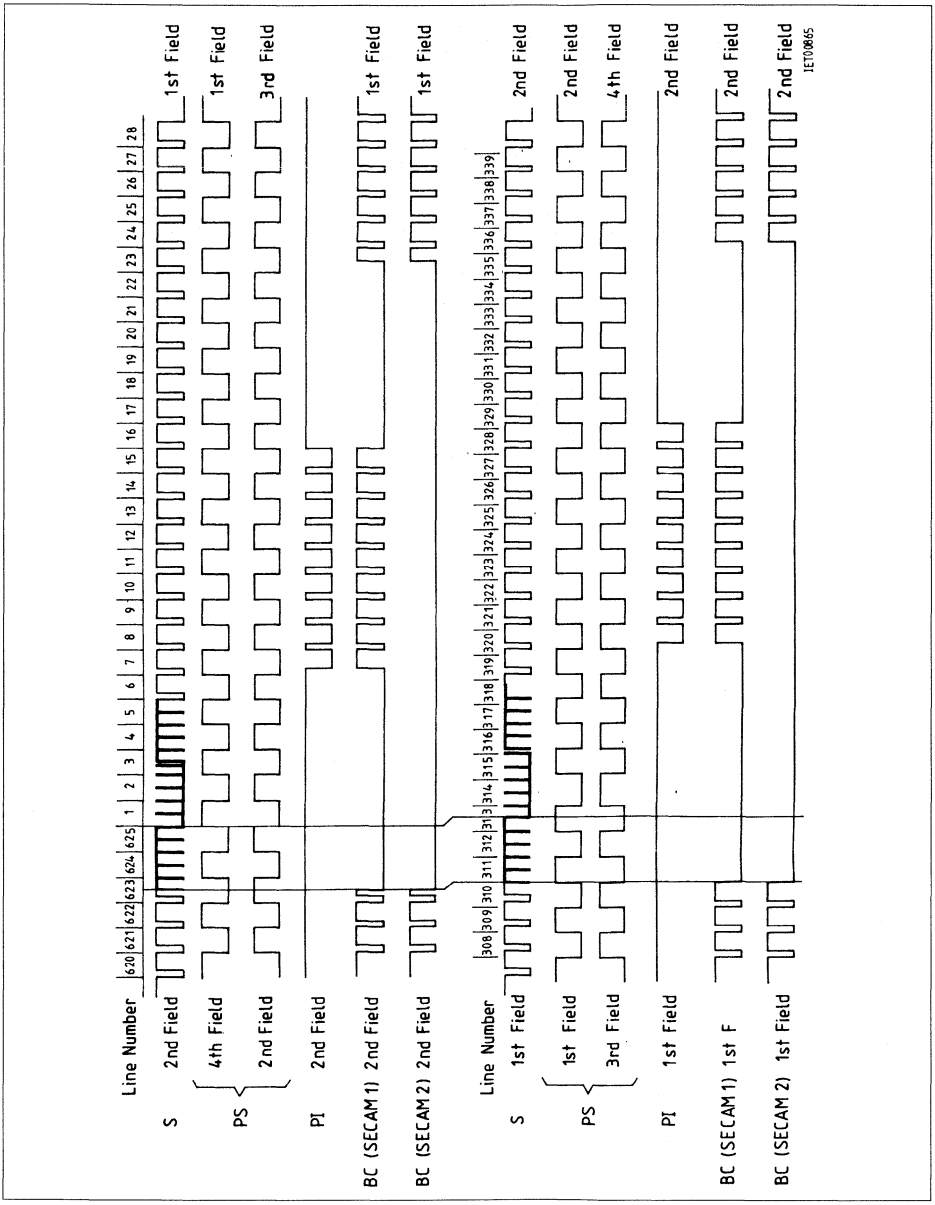


Figure 8
Color Identification Signals in SECAM

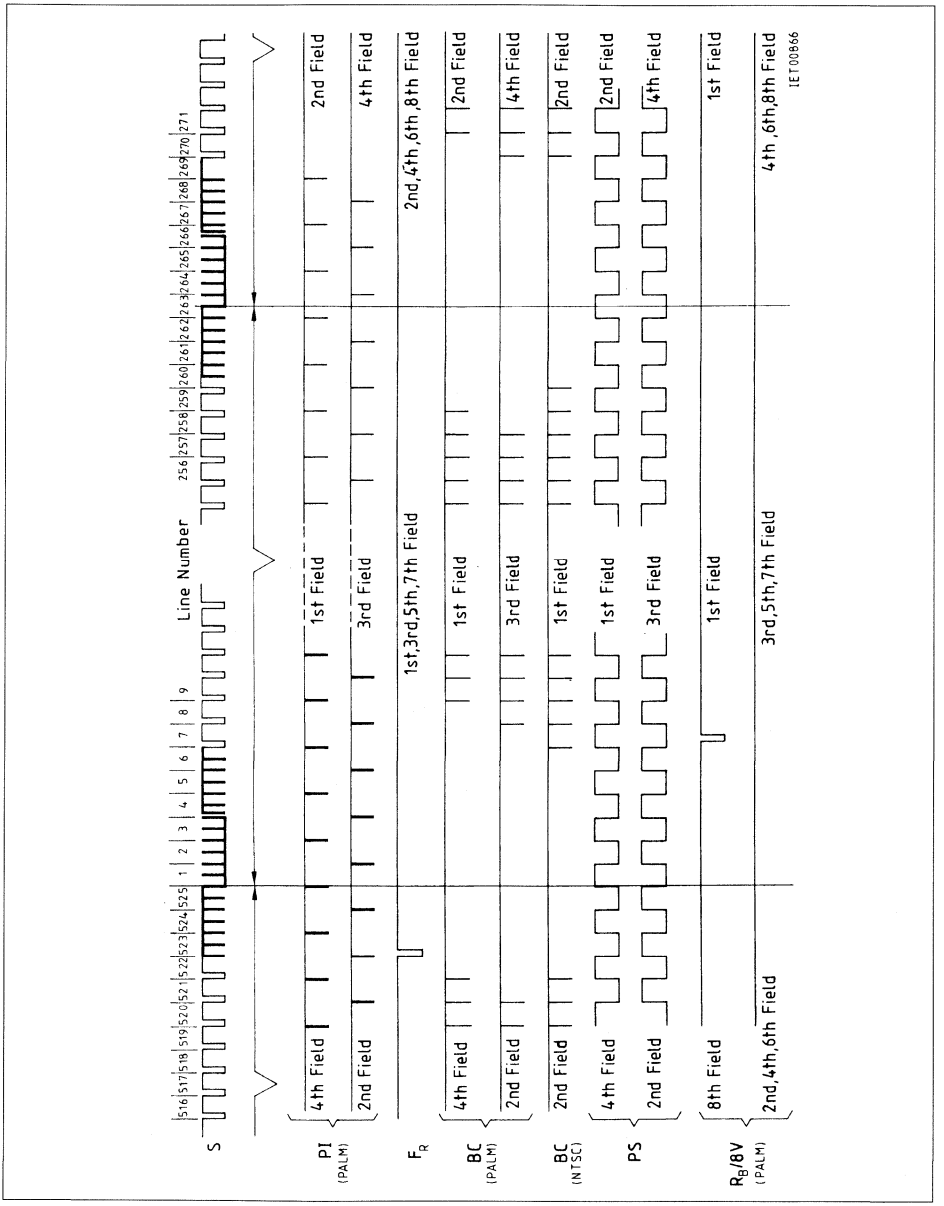


Figure 9
Color Identification Signals in NTSC and PAL-M

Selector Guide

Type	Package	Function	Supply Voltage V_S / V	Temperature Range T_A / °C	Page
Acoustic Signal Generators					
SAE 800	P-DIP-8	Programmable	2.8 to 18	- 25 to 85	517
SAE 800 G	P-DSO-8-1	Single-/Dual-/ Triple-Tone Gong	2.8 to 18	- 25 to 85	517

= SMD

SIEMENS

Programmable Single-/Dual-/Triple- Tone Gong

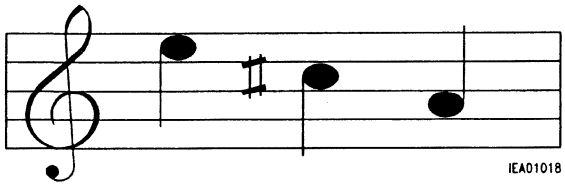
SAE 800

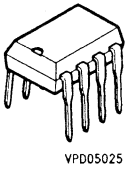
Advance Information

Bipolar IC

Features

- Supply voltage range 2.8 V to 18 V
- Few external components (no electrolytic capacitor)
- 1 tone, 2 tones, 3 tones programmable
- Loudness control
- Typical standby current 1 µA
- Constant current output stage (no oscillation)
- High-efficiency power stage
- Short-circuit protection
- Thermal shutdown





P-DIP-8

P-DSO-8-1

Type	Ordering Code	Package
▼ SAE 800	Q67000-A8339	P-DIP-8
▼ SAE 800 G	Q67000-A8340	P-DSO-8-1 (SMD)

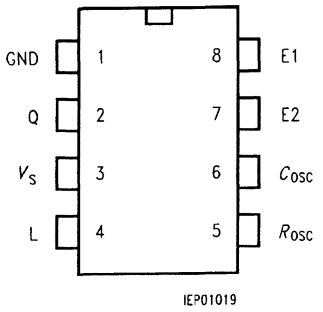
▼ New type

Functional Description

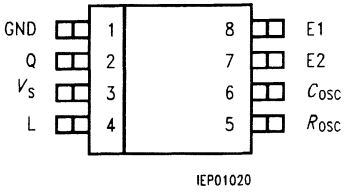
The SAE 800 is a single-tone, dual-tone or triple-tone gong IC designed for a very wide supply voltage range. If the oscillator is set to f_0 = 13.2 kHz for example, the IC will issue in **triple-tone-mode** the minor and major third e^2 – C sharp – a, corresponding to 660 Hz – 550 Hz – 440 Hz, in **dual-tone-mode** the minor third e^2 – C sharp, and in **single-tone-mode** the tone e^2 (derived from the fundamental frequency f_0; $f_1 = f_0 / 20, f_2 = f_0 / 24, f_3 = f_0 / 30$).

When it is not triggered, the IC is in a standby state and only draws a few µA. It comes in a compact P-DIP-8 or P-DSO-8 (SMD) package and only requires a few external components.

SAE 800



SAE 800 G



Pin Configuration
(top view)

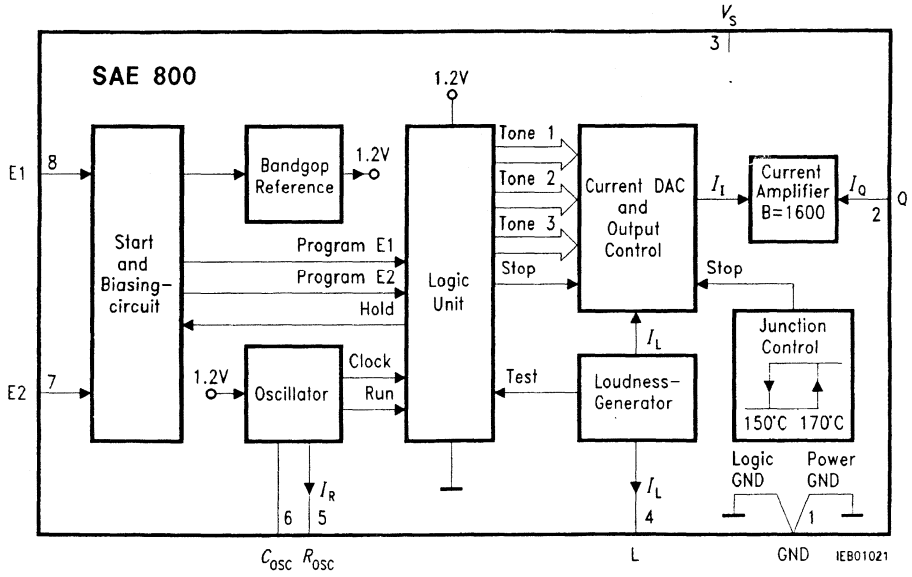
Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	Q	Output
3	V_S	Supply Voltage
4	L	Loudness Control
5	R_{OSC}	Oscillator Resistor
6	C_{OSC}	Oscillator Capacitor
7	E2	Trigger 2 (dual tone)
8	E1	Trigger 1 (single tone)

Functional Description

An RC combination is needed to generate the fundamental frequency (pin R_{OSC}, C_{OSC}). The volume can be adjusted with another resistor (pin L). The loudspeaker must be connected directly between the output Q and the power supply V_S. The current-sink principle combined with an integrated thermal shutdown (with hysteresis) makes the IC overload-protected and shortcircuit-protected.

There are two trigger pins (E1, E2) for setting single-tone, dual-tone or triple-tone mode.



Block Diagram

Circuit Description

Trigger

Positive pulses on inputs E1 and/or E2 trigger the IC. The hold feedback in the logic has a delay of several milliseconds. After this delay has elapsed, the tone sequence is started. This prevents parasitic spikes from producing any effect on the trigger pins.

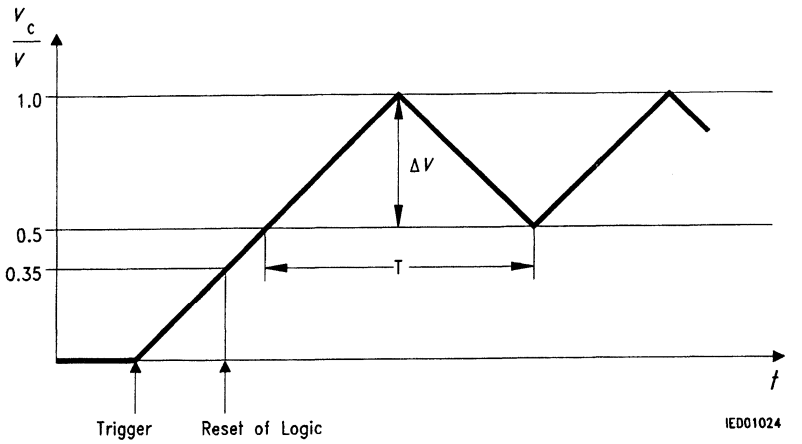
The following **table** shows the trigger options:

E1	E2	Mode	Issued Sequence
Triggered	Triggered	Triple-tone	Minor and major third
Grounded/open	Triggered	Dual-tone	Minor third
Triggered	Grounded/open	Single-tone	1st tone of minor third

Oscillator

This is a precision triangle oscillator with an external time constant (R x C). Capacitor C_C on pin C_{OSC} is charged by constant current to 1 V and then discharged to 0.5 V. The constant current is obtained on pin R_{OSC} with an external resistor R_R to ground.

When the voltage on C_{OSC} is building up, the logic is reset at 350 mV. This always ensures that a complete tone sequence is issued. If the oscillator pin is short-circuited to GND during operation, the sequence is repeated.



The following applies: $\Delta V_C \times C_C = I_C \times T/2$ with $I_C = V_R/2R_R = 1.2\ V/2R_R$

$f_0 = 5/8 \times 1/(R_R \times C_C)$

Voltages on Pin C_{OSC}

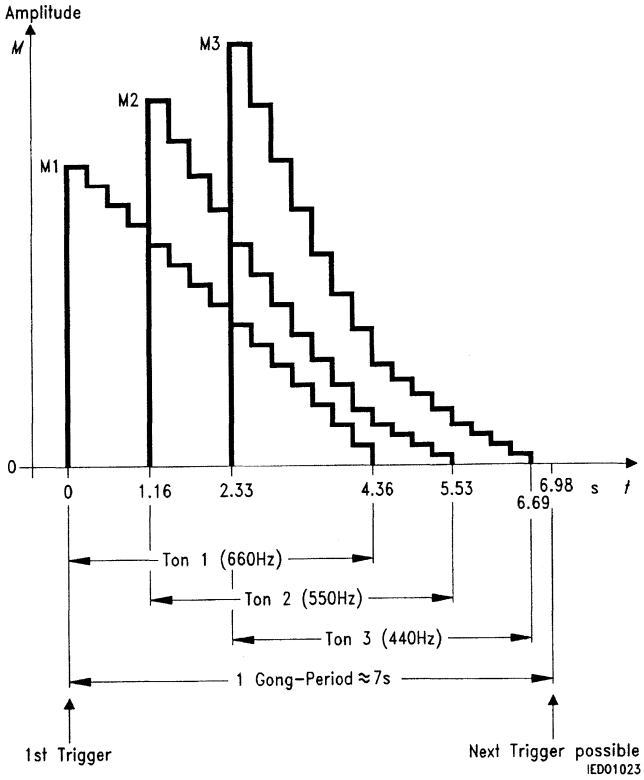
Logic

The logic unit contains the complete sequence control. The oscillator produces the power-on reset and the clock frequency. Single-tone, dual-tone or triple-tone operation is programmed on inputs E1 and E2. The 4-bit digital/analog converters are driven in parallel. In the event of oscillator disturbance, and after the sequence, the dominant stop output is set. By applying current to pin L, the sequence can be shortened by a factor of 30 for test purposes.

The following figure shows the envelope of the triple-tone sequence:

Envelope of maximum amplitudes of three superimposed tones on Q (time scale for f_{OSC} = 13.2 kHz)

Ratio of maximum amplitudes
M3 : M2 : M1 = 1 : 0.89 : 0.67



Envelope of the Triple-Tone Sequence

Digital / Analog Converter, Loudness and Junction Control

The DAC converts the 4-bit words from the logic into the appropriate staircase currents with the particular tone frequency. The sum current I_I drives the following current amplifier. The loudness generator produces the DAC reference current I_L for all three tones. This requires connecting an external resistor to ground. The chip temperature is monitored by the junction control. At temperatures of more then approx. 170 °C the stop input will switch the output current I_I to zero. The output current is enabled again once the chip has cooled down to approx. 150 °C.

Current Amplifier

The current amplifier with a gain of 1600 boosts the current I_I from approx. 470 µA maximum to approx. 750 mA maximum. The output stage consists of an NPN transistor with its emitter on power GND and collector on pin Q.

The current control insures that the output stage only conducts defined currents. In conjunction with the integrated thermal shutdown, this makes the configuration shortcircuit-protected within wide limits. Because of the absence of feedback the circuit is also extremely stable and therefore uncritical in applications. Resistor R_L on pin L sets the output voltage swing. This assumes that the resistive component of the loudspeaker impedance R_Q responds similarly as the resistance R_L.

The output amplitude of the current I_L reaches the maximum $I_{Imax} \cong 3 \times V_L / R_L$ at a time t of 2.33 s* (only 3 tone mode), so R_L has to be scaled for this point.

The following applies:

$I_Q = I_{Imax} \times B = (V_S - V_{sat}) / R_Q = 0.8\ V_S / R_Q$

$3 \times B \times (V_L / R_L) = 0.8\ V_S / R_Q$

the result is:

$R_L = R_Q \times 3 \times B \times (V_L / 0.8\ V_S)$ with: B = 1600

$R_L = R_Q \times K \times (V_L / 0.8\ V_S)$ with: K = 4800

Application Hints and Application Circuit

1) Loudness Resistor (max. Loudness of 3-Tone Signal with Ensured Ratio of Amplitudes)

$0.8\ V_S / R_Q \approx (V_L / R_L) \times K$

$R_L = (V_L / 0.8\ V_S) \times R_Q \times K$; K = 4800

Example: R_Q = 8 Ω; V_S = 5 V; V_L = 1.2 V

R_L = (1.2 / 4) x 8 Ω x 4800 = 12 kΩ

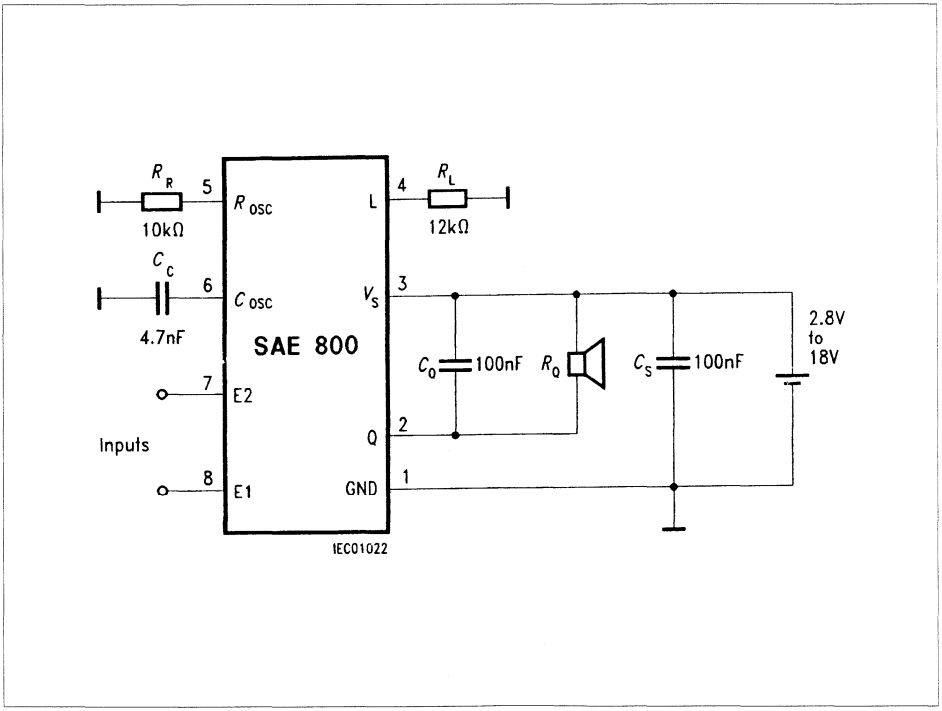
2) Oscillator Elements R_R, C_C

f = 5 / 8 x 1 / (R_R x C_C)

Example: f = 13.2 kHz; C_C = 4.7 nF

R_R = 5 / (8 x 13.2 x 4.7) x 10^6 Ω ≈ 10 kΩ

The following is a typical application circuit



Application Circuit

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	– 0.3	24	V
Input voltage at E1, E2	$V_{E1, E2}$	– 5	24	V
Current at output Q	I_Q	– 50	750	mA
Current at input pins E1, E2	$I_{E1, E2}$	– 2	3	mA
Current at pin R_{OSC}	I_R	– 300	200	µA
Current at pin L	I_L	– 300	0	µA
Current at pin C_{OSC}	I_C	– 200	200	µA
Junction temperature	T_j	– 50	150	°C
Storage temperature	T_{stg}	– 50	150	°C

Operating Range

Supply voltage	V_S	2.8	18	V
Junction temperature	T_j	– 25	125	°C
Oscillator frequency at C_{OSC}	f_C	–	100	kHz
Current at pin R_{OSC}	I_R	– 200	– 10	µA
Current for test mode at pin L	I_R	90	110	µA
Current at pin L	I_L	– 200	– 10	µA
Input voltage at E1, E2	$V_{E1, E2}$	– 4	18	V
Thermal resistance				
junction-air (P-DIP-8)	$R_{th\ JA}$	–	100	K/W
junction-air (P-DSO-8-1)	$R_{th\ JA}$	–	180	K/W

Characteristics

T_j = – 25 to 125°C; V_S = 2.8 to 18 V

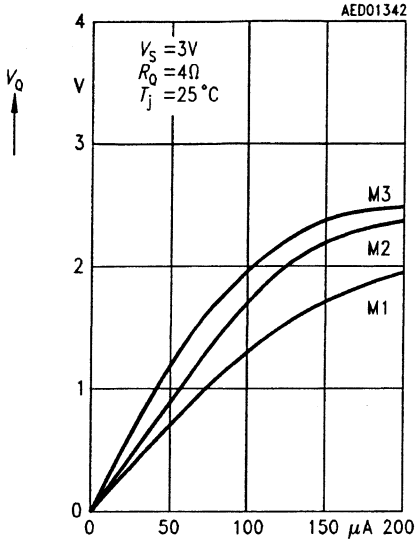
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Section						
Standby current	I_{St}	–	1	10	µA	–
Quiescent current; pin L open	I_{Qu}	–	5	10	mA	–
Output Section						
Peak output power (tone 3)						
V_S = 2.8 V; R_Q = 4 Ω; R_L = 8.2 kΩ	P_Q	–	250	–	mW	A
V_S = 2.8 V; R_Q = 8 Ω; R_L = 18 kΩ	P_Q	–	125	–	mW	B
V_S = 5.0 V; R_Q = 8 Ω; R_L = 10 kΩ	P_Q	–	450	–	mW	C
V_S = 5.0 V; R_Q = 16 Ω; R_L = 18 kΩ	P_Q	–	225	–	mW	D
V_S = 12 V; R_Q = 50 Ω; R_L = 33 kΩ	P_Q	–	450	–	mW	E
Output level differences:						
tone 1 to 3	a_{13}	– 1	–	1	dB	C [1]
tone 2 to 3	a_{23}	– 1	–	1	dB	C [2]
Biasing Section						
Voltage at pin R_{OSC}; R_R = 10 kΩ	V_R	–	1.2	–	V	–
Voltage at pin L; R_L = 10 kΩ	V_L	–	1.2	–	V	–
Oscillator Section						
Amplitude	ΔV_C	–	0.5	–	V	–
Frequency R_R = 10 kΩ; C_C = 4.7 nF	f_0	–	13.2	–	kHz	–
Oscill. drift vs. temperature	D_T	– 3	–	+ 3	10-4/K	–
Oscill. drift vs. supply voltage	D_V	–	1	–	10-3/V	–
Input Section						
Triggering voltage at E1, E2	$V_{E1,E2}$	1.6	–	–	V	–
Triggering current at E1, E2	$I_{E1,E2}$	100	–	–	µA	–
Noise voltage immunity at E1, E2	$V_{E1,E2}$	–	–	0.3	V	–
Triggering delay at f_0 = 13.2 kHz	t_{dT}	2	–	5	ms	–

1) $a_{13} = 20 \times \log (M_1 / (0.67 \times M_3))$

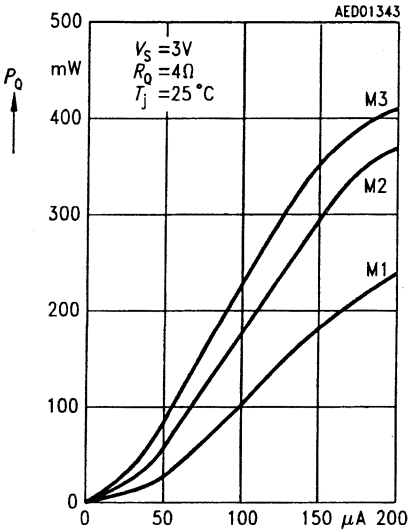
2) $a_{23} = 20 \times \log (M_2 / (0.89 \times M_3))$

9

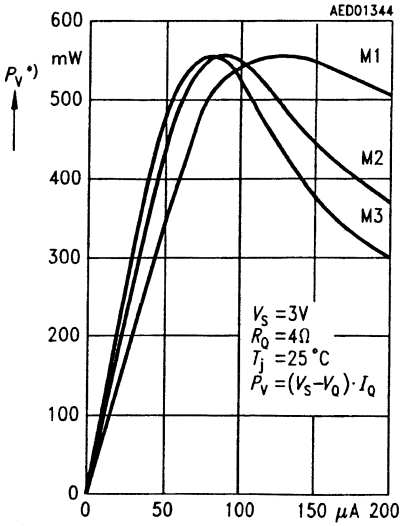
Output Peak Voltage V_Q versus Loadness-Current I_L



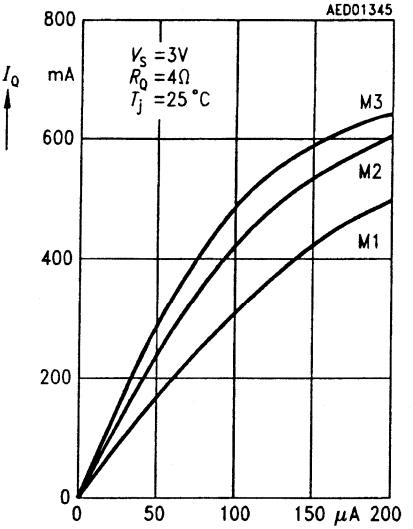
Max. Output Power P_Q versus Loadness-Current I_L



Power Dissipation P_v of Output Stage versus Loudness-Current I_L

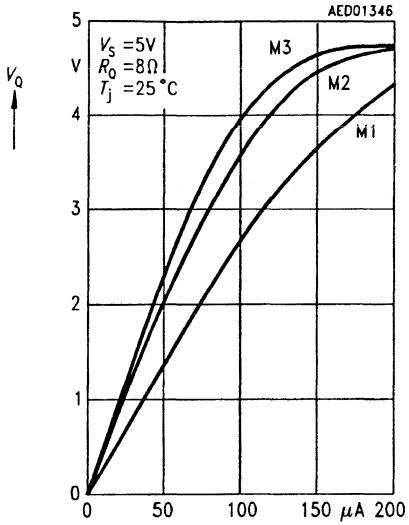


Peak Current I_Q versus Loadness-Current I_L

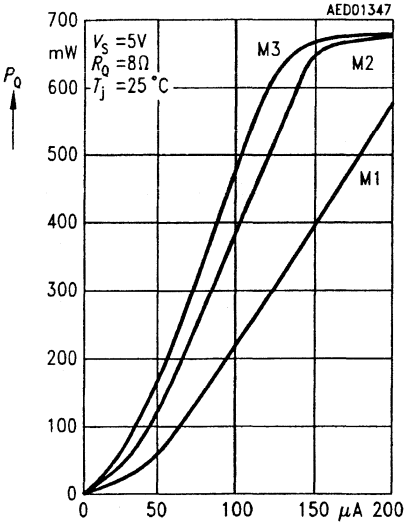


*) Note that $I_Q = f(I_L)$ varies between 0 and K · I_L during tone sequence. Thereby the maximum of the power dissipation during the tone sequence is the maximum of P_v (in diagram) between $I_L = 0$ and chosen $I_L = V_L/R_L$.

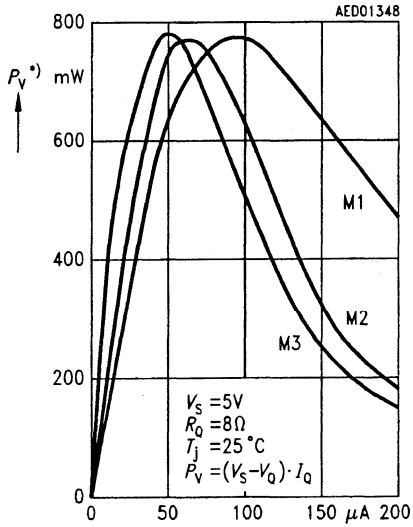
Output Peak Voltage V_Q versus Loadness-Current I_L



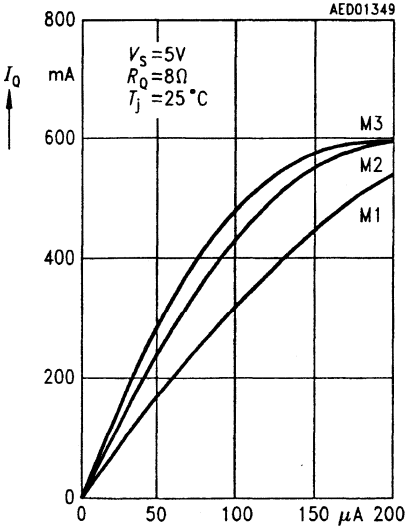
Max. Output Power P_Q versus Loadness-Current I_L



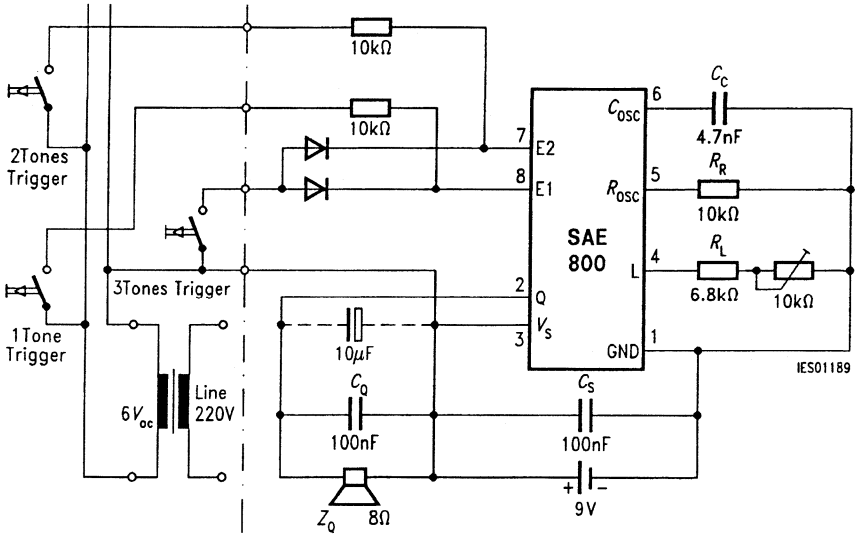
Power Dissipation P_v of Output Stage versus Loudness-Current I_L



Peak Current I_Q versus Loadness-Current I_L

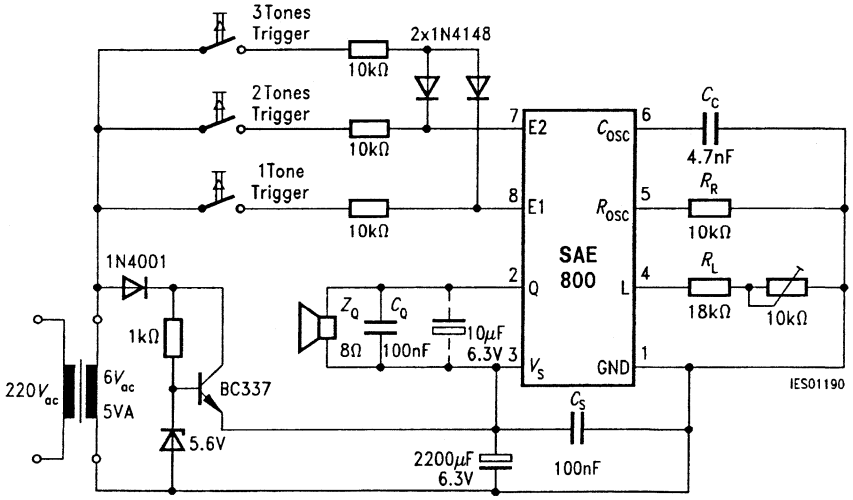


*) Note that $I_Q = f(I_L)$ varies between 0 and K · I_L during tone sequence. Thereby the maximum of the power dissipation during the tone sequence is the maximum of P_v (in diagram) between I_L = 0 and chosen $I_L = V_L/R_L$.



Circuit for SAE 800 Application in Home Chime Installation Utilizing AC and DC Triggering for 1, 2 or 3 Tone Chime; Adjustable Volume

PCB layout information: Because of the peak currents at V_S, Q and GND the lines should be designed in a flatspread way or as star pattern.



Circuit for SAE 800 Application in Home Chime Installation for Operation without Battery

Leistungs-OP, Leistungsbrücken, Spezielle Motoransteuerungen

Power Op Amps, Power Bridges, Special Motor Control ICs

Selector Guide

Type			Features								Page
			Peak Output Current	Operating Range	Max. Supply Voltage	Short-Circuit Proof to $+V_S$	Short-Circuit Proof to $-V_S$	Clamp Diodes	Inhibit	Package	
Dual Power Operational Amplifiers		TCA 2465	2.5 A	40 V	42 V	●	●	●	●	P-SIP-9	533
		TCA 2465 A	2.5 A	40 V	42 V	●	●	●	●	P-DIP-16	533
		TCA 2465 G	2.0 A	40 V	42 V	●	●	●	●	P-DSO-20-1	533
Full Bridge DC Motor Drivers	DC Motor ICs	TLE 4201 A1	1 A	17 V	36 V		●			P-DIP-18-1	551
		TLE 4201 S1	1 A	17 V	36 V		●			P-SIP-9	551
		TLE 4205	1 A	32 V	45 V		●	●	●	P-DIP-18-1	560
		TLE 4205 G	1 A	32 V	45 V		●	●	●	P-DSO-20-1	560
		TLE 4202	1.5 A	17 V	36 V		●			P-TO220-7-1	570
		TLE 4202 B	2 A	17 V	36 V		●	●		P-TO220-7-1	579
		TLE 4204	3 A	24 V	45 V	●	●	●		P-TO220-7-1	589
		TLE 5203	3 A	24 V	40 V	●	●	●		P-TO220-7-1	598
		TLE 4203	4 A	26 V	45 V	●	●	●		P-TO220-7-1	608
		TLE 4203 S	4 A	26 V	45 V	●	●	●		P-TO220-7-2	608
	Stepper M. ICs	TCA 3727	1 A	50 V	52 V	●		●	●	P-DIP-20-1	616
		TCA 3727 G	1 A	50 V	52 V	●		●	●	P-DSO-24-1	616
		TLE 4727	1 A	25 V	45 V	●	●	●	●	P-DIP-20-1	634
		TLE 4728 G	1 A	25 V	45 V	●	●	●	●	P-DSO-24-1	652
Control ICs		SLE 4520	20 mA	5 V	6 V					P-DIP-28	671

= SMD

SIEMENS

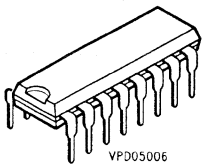
Dual Power Operational Amplifier

TCA 2465

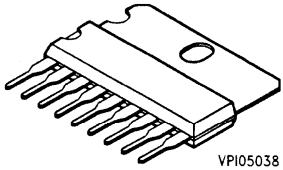
Bipolar IC

Features

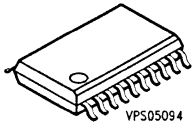
- High output peak current of twice 2.5 A
- Twice 2.0 A output peak current for TCA 2465 G
- Large supply voltage range up to 42 V
- High slew rate of 2 V/µs
- Outputs fully protected (DC short-circuit proof)
- Thermal overload protection
- Inhibit input enables "tristate" outputs
- Integrated clamp diodes



P-DIP-16



P-SIP-9



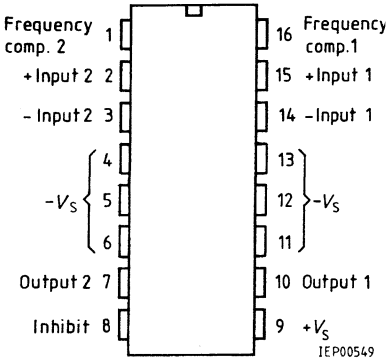
P-DSO-20-1

	Type	Ordering Code	Package
S	TCA 2465	Q67000-A8109	P-SIP-9
S	TCA 2465 A	Q67000-A8110	P-DIP-16
S ▼	TCA 2465 G	Q67000-A8334	P-DSO-20-1 (SMD)

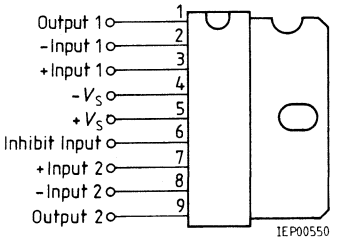
▼ New type

The IC contains two identical op amps, each supplying a high output current of 2.5 A at supply voltages between ± 3 V and ± 20 V. Internal compensation permits negative feedback of the amplifiers up to a min. of 20 dB. If a voltage gain of 0 to 20 dB is required, the TCA 2465 A can be compensated with external capacitors from pin 7 to 1 or pin 10 to 16. Both amplifiers can be disconnected at $V_8 \geq 2$ V via an inhibit input. Integrated protective circuits protect the outputs against short-circuit to + V_S and − V_S and prevent thermal overloading of the IC. TCA 2465 G comes in a special surface-mounted power package similar to P-DSO-20 and delivers twice 2.0 A output peak current.

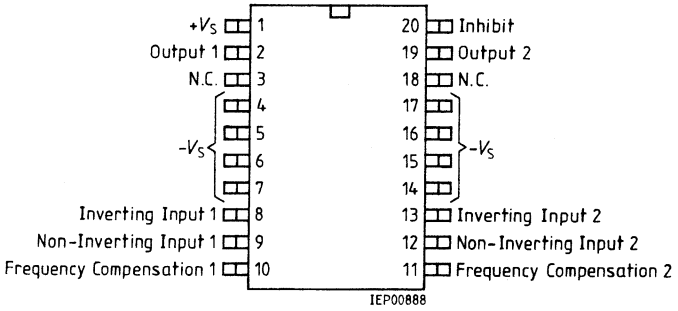
TCA 2465 A



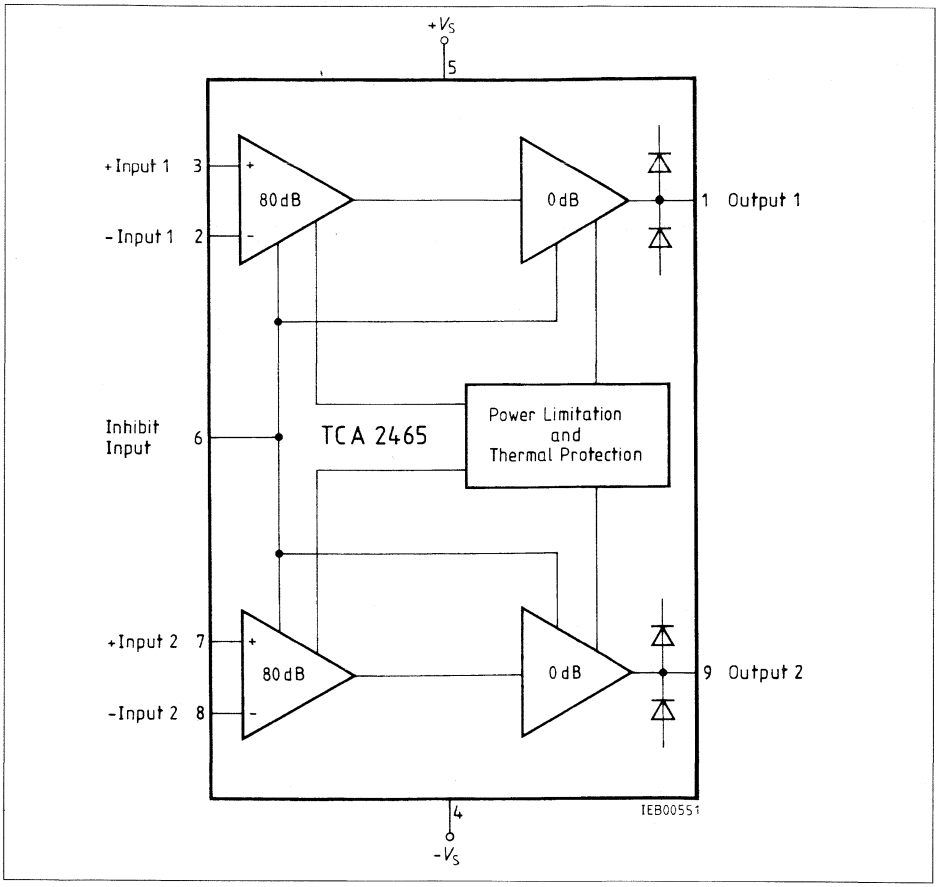
TCA 2465



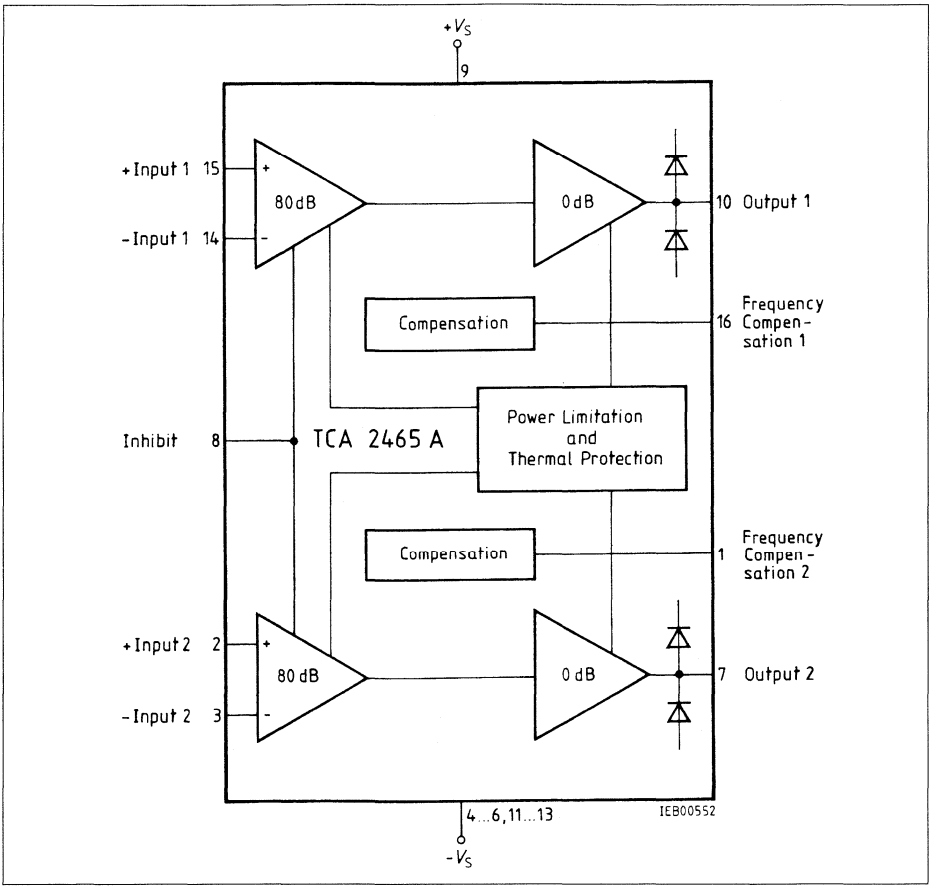
TCA 2465 G



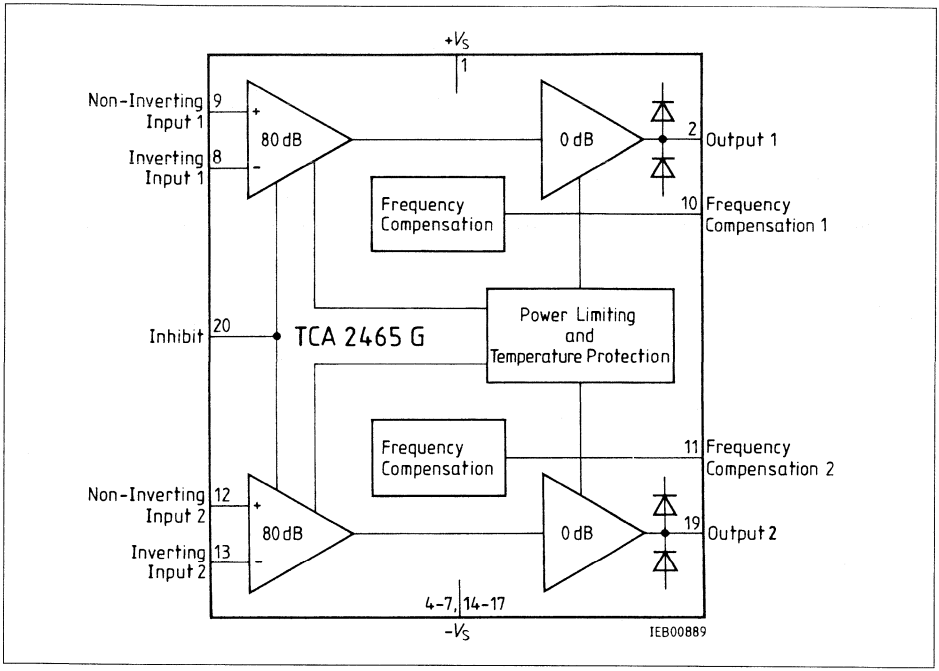
Pin Configuration
(top view)



Block Diagram
TCA 2465



Block Diagram
TCA 2465 A



Block Diagram
TCA 2465 G

10

Absolute Maximum Ratings
T_C = – 40 to 85 °C

Note: Values in brackets refer to TCA 2465 G

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S		± 21	V	$\Delta V_{2\text{-}3}$ or $\Delta V_{8\text{-}7}$
Differential input voltage	V_{ID}		$(-V_S)+(+V_S)$	V	
Output current	I_Q	–2.5 (– 2.0)	2.5 (2.0)	A	I_1 or I_9
Output current	I_Q	–1.5		A	$V_S \geq \pm$ 15 V; $V_Q < -V_S$
Supply current	I_S	– 5 (– 2.0)	5.5 (2.0)	A	I_S
Ground current	I_{GND}	– 5.5 (– 2.0)	5 (2.0)	A	I_4
Input voltage	V_I	$-V_S$	$+V_S$	V	V_2, V_3, V_7, V_8
Inhibit input	V_6	$-V_S$	$+V_S$	V	
Junction temperature	T_j		150	°C	
Storage temperature range	T_{stg}	– 50	125	°C	

Operating Range

Supply voltage	V_S	± 3	± 20	V	
Case temperature	T_C	– 40	85	°C	P_D = 12 W
Voltage gain	$G_{V\,min}$	20		dB	
Thermal resistance junction - ambient junction - case	 $R_{th\,jA}$ $R_{th\,jC}$		 60 (70) 5 (22)	 K/W K/W	 (soldered)

Characteristics
$V_S = \pm 10$ V; $T_j = 25$ °C

Note: Values in brackets refer to TCA 2465 A; G

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Open-loop supply current consumption S1 in position 1 and 2	I_S		30	50	mA	1
Input offset voltage	V_{IO}	– 10		10	mV	2
Input offset current Input current	I_{IO} I_I	– 100	 0.25	100 1	nA µA	3 3
Output voltage $R_L = 12\,\Omega$; $f = 1$ kHz $R_L = 4\,\Omega$; $f = 1$ kHz $R_L = 470\,\Omega$; $f = 40$ kHz	 $V_{Q\,pp}$ $V_{Q\,pp}$ $V_{Q\,pp}$	 ± 8.5 ± 8.0	 ± 9.0 ± 8.5 (± 9.0) ± 8.0		 V V V	 4 4 4
Input resistance $f = 1$ kHz	R_I	1	5		MΩ	4
Open-loop voltage gain $f = 100$ kHz	G_{VO}	70	80		dB	5
Common-mode input voltage range	V_{IC}	+ 7/–10	± 7.5/– 10.5		V	6
Common-mode rejection Supply voltage rejection	k_{CMR} k_{SVR}	70 – 70	80 – 80		dB dB	6 7
Temperature coefficient of V_{IO} – 40 °C ≤ T_j ≤ + 85 °C Temperature coefficient of I_{IO} – 40 °C ≤ T_j ≤ + 85 °C	α_{VIO} α_{IIO}		50 0.4		µV/K nA/K	2 3
Slew rate of V_Q for non-inverting operation Slew rate of V_Q for inverting operation	SR SR		2 (0.5) 2 (0.5)		V/µs V/µs	8 9
Noise voltage (DIN 45405, referred to input)	V_n		3		µV	1
Inhibit input (referred to – V_S) V_6 for IC turned OFF V_6 for IC turned ON	 $V_{6\,OFF}$ $V_{6\,ON}$	 2.0		 0.8	 V V	 1 1

10

Characteristics (cont'd)
$V_S = \pm 10$ V; $T_j = 25$ °C

Note: Values in brackets refer to TCA 2465 A; G

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
H-input current, $V_6 = 5$ V[1]	I_{6H}		0.1	0.5	µA	1
L-input current, $V_6 = 0$ V[1]	I_{6L}		0.5	3.0	µA	1
Turn-ON dead time $\lvert I_{1;9} \rvert > A$[2] (referred to $V_{6\,OFF/ON}$)	$t_{D\,ON}$		10	20	µs	1
Turn-OFF dead time $\lvert I_{1;9} \rvert < 1$ A[2] (referred to $V_{6\,OFF/ON}$)	$t_{D\,OFF}$		10	20	µs	1
Short-circuit current (switch S3 closed)	I_{SC}		1		A	1
Short-circuit current (switch S4 closed)	I_{SC}		1		A	1

[1] referred to $-V_S$
[2] Switch S2 closed

Test Circuits

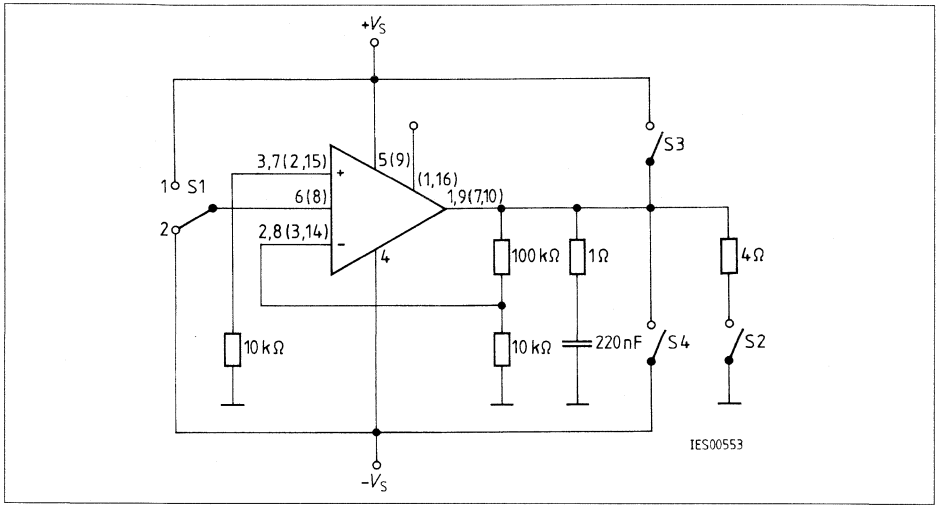


Figure 1
Open-Loop Supply Current Consumption; Noise Voltage

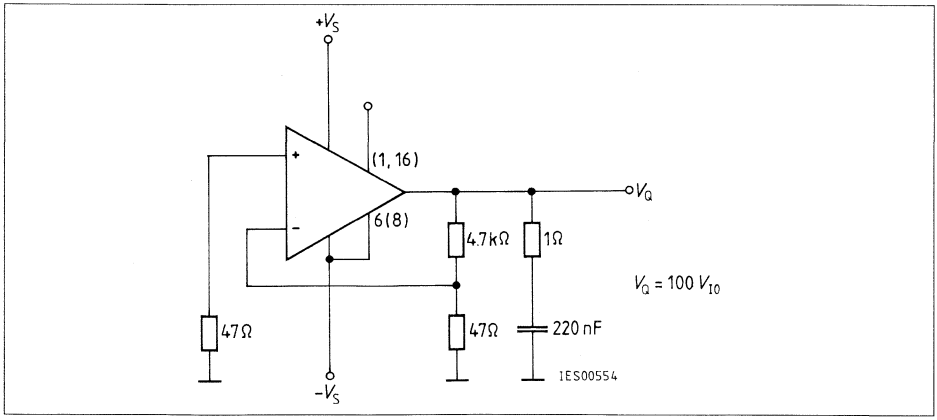


Figure 2
Input Offset Voltage; Temperature Coefficient of V_{IO}

10

Note: Values in brackets refer to TCA 2465 A

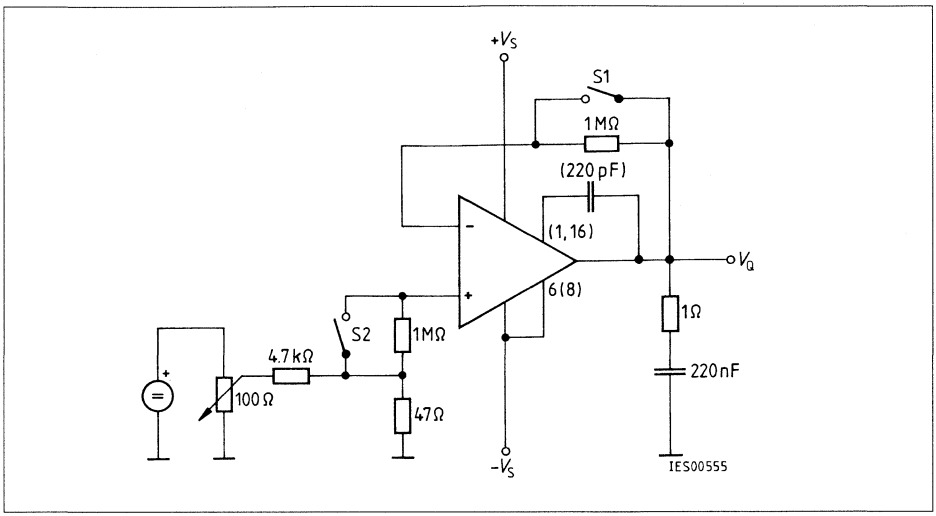


Figure 3
Input Offset Current; Input Current; Temperature Coefficient of I_{IO}

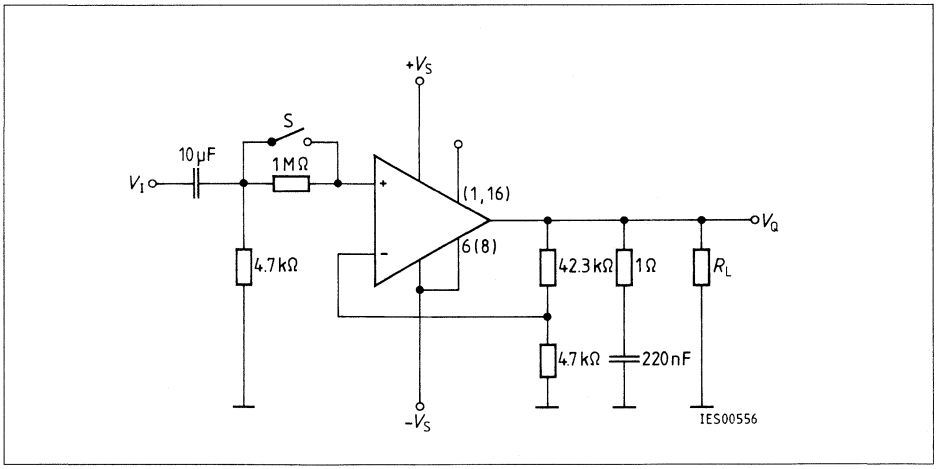


Figure 4
Output Voltage; Input Resistance

Note: Values in brackets refer to TCA 2465 A

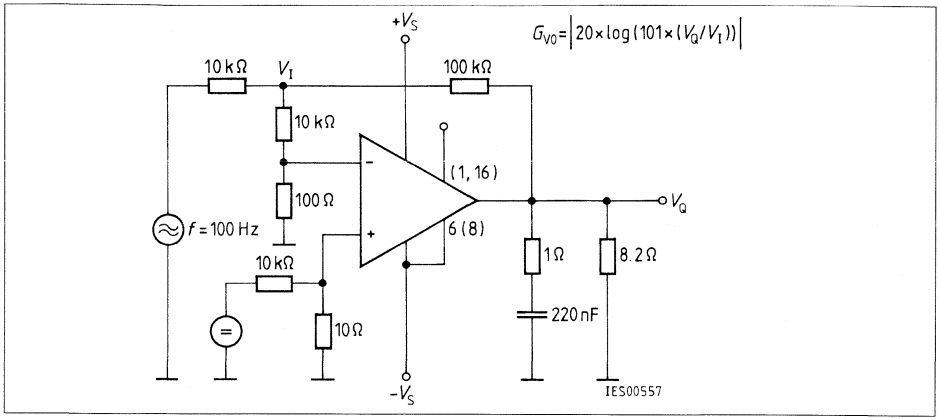


Figure 5
Open-Loop Voltage Gain G_{VO}

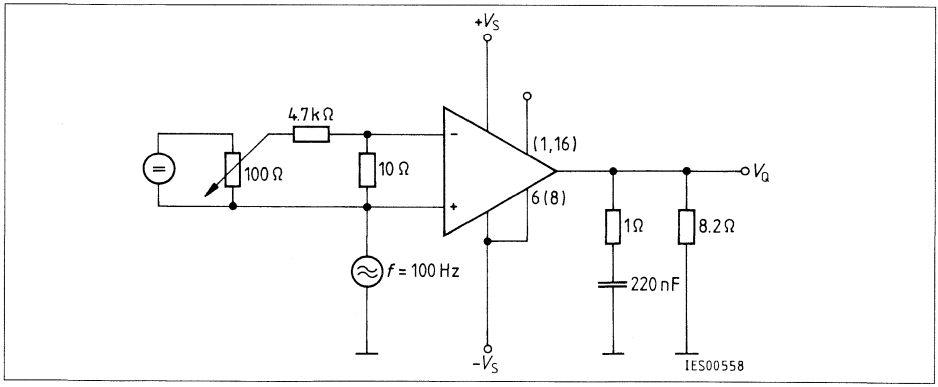


Figure 6
Open-Loop Voltage Gain G_{VC}
Common-Mode Rejection k_{CMR} (dB) = G_{VO} (dB) − G_{VC} (dB)

10

Note: Values in brackets refer to TCA 2465 A

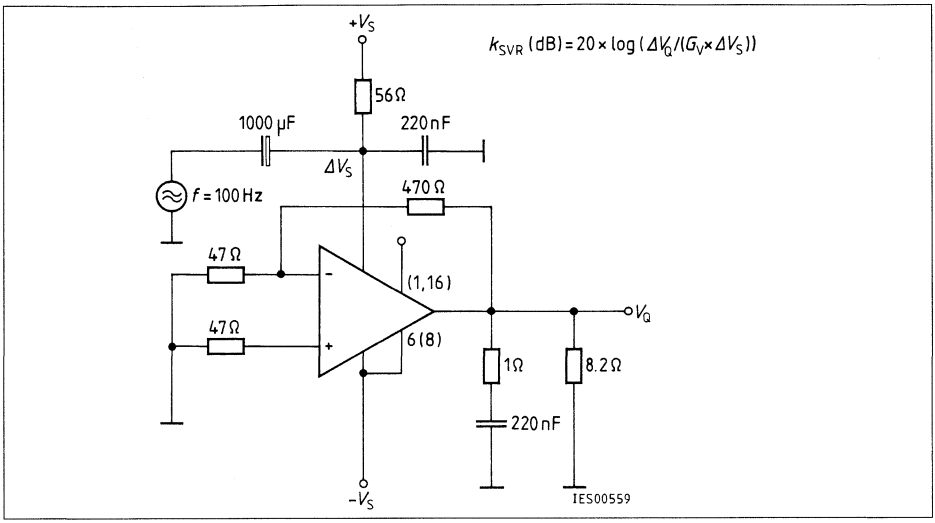


Figure 7
Supply Voltage Rejection k_{SVR}

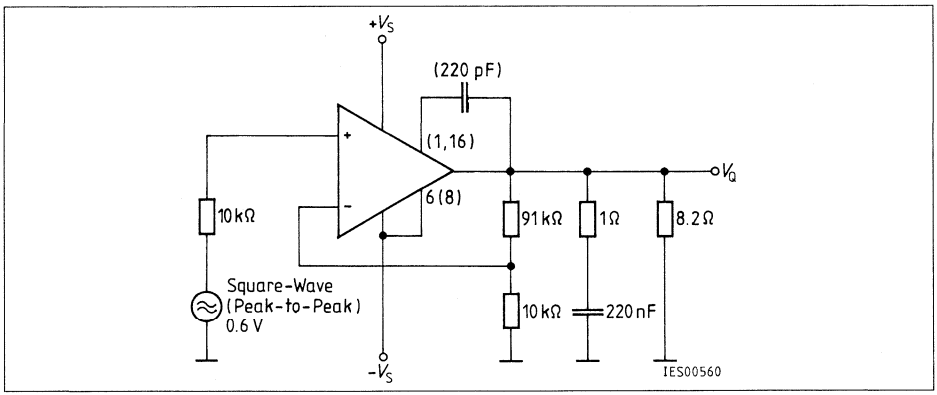


Figure 8
Slew Rate for Non-Inverting Operation

Note: Values in brackets refer to TCA 2465 A

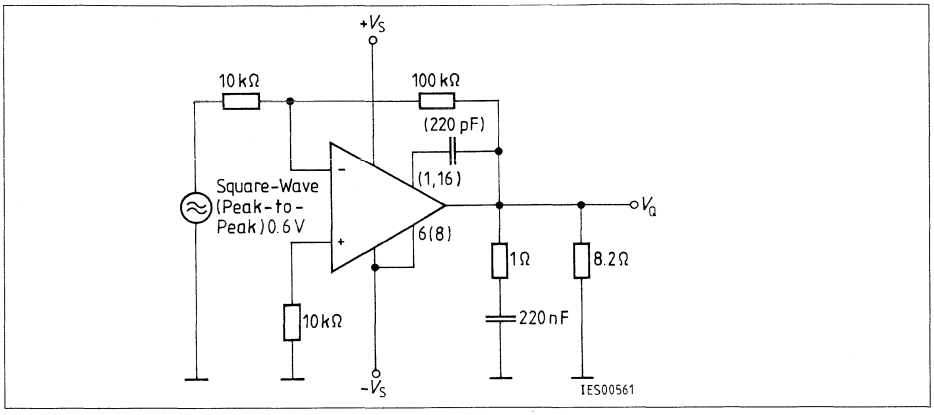
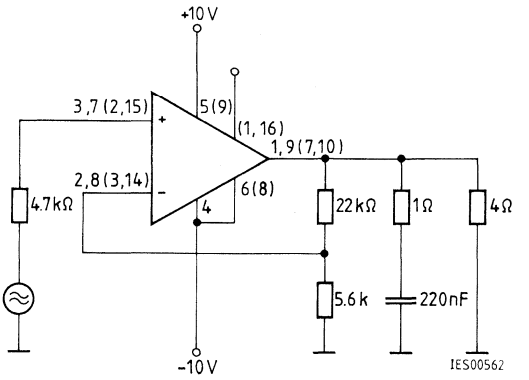


Figure 9
Slew Rate for Inverting Operation

10

Note: Values in brackets refer to TCA 2465 A.

a) Amplifier; $G_V = 5$



b) Voltage follower TCA 2465 A

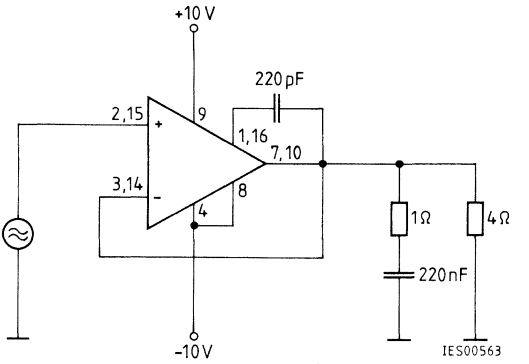
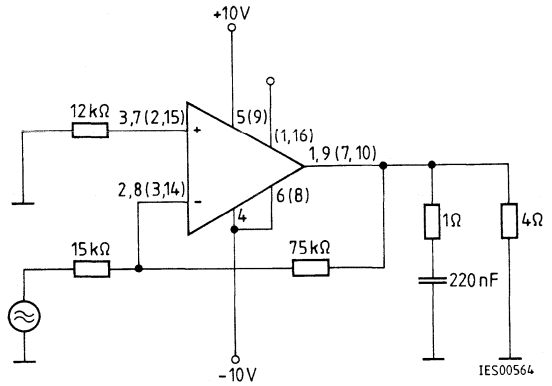


Figure 10
Non-Inverting Operation

Note: Values in brackets refer to TCA 2465 A.

a) Amplifier; $G_V = -5$



b) Inverter TCA 2465 A

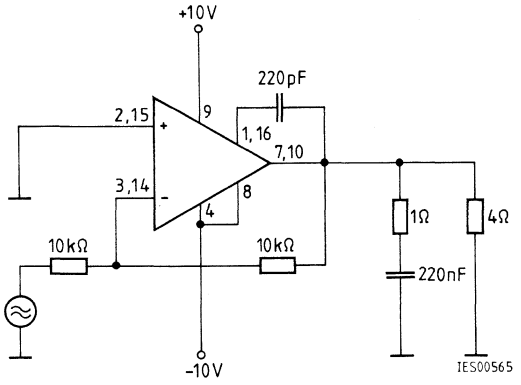
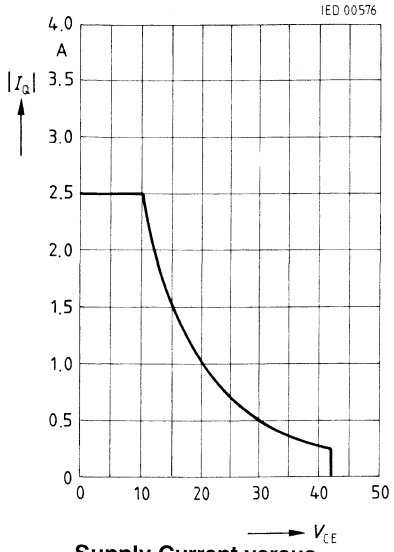


Figure 11
Inverting Operation

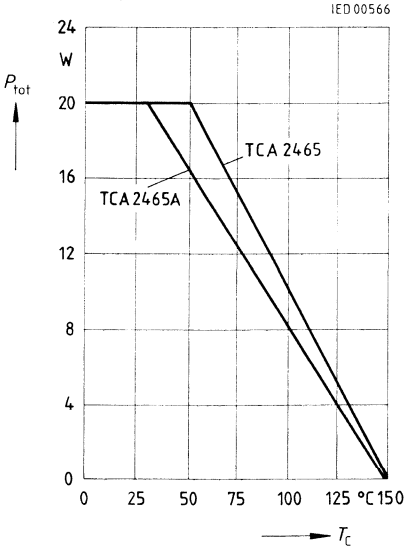
Note: Values in brackets refer to TCA 2465 A.

10

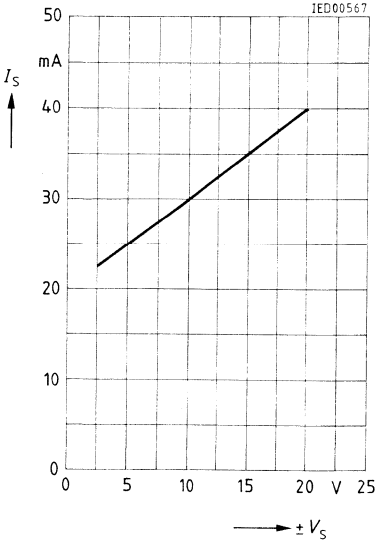
Safe Operating Area (SOA)
Peak Output Current versus Collector-Emitter Voltage
$T_j = 25\,^{\circ}C$, $V_{CE} = +V_S - V_Q$ or $V_{CE} = -V_S - V_Q$



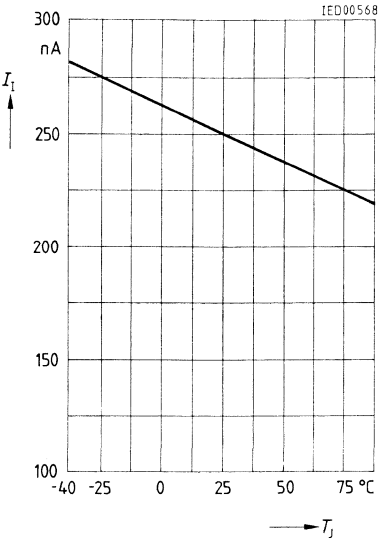
Max. Permissible Power Dissipation versus Case Temperature



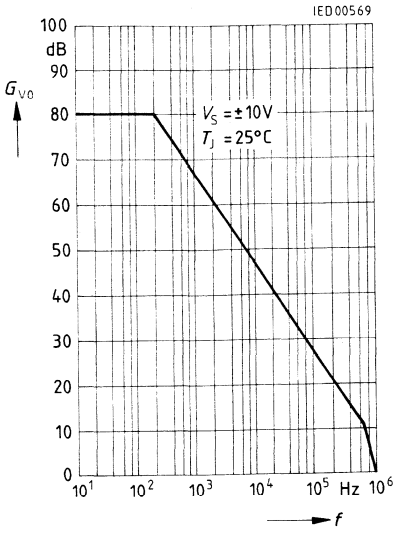
Supply Current versus Supply Voltage
$T_j = 25\,^{\circ}C$



Input Current versus Junction Temperature
$V_S = \pm 10$ V

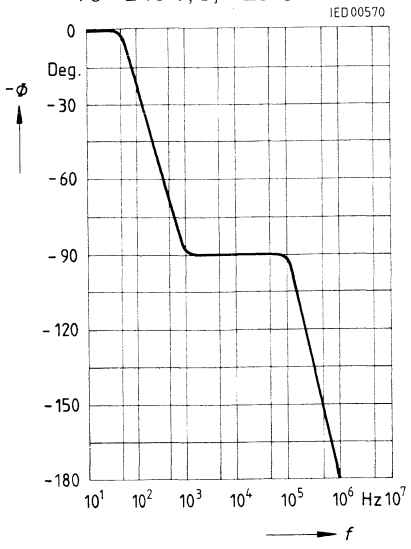


Open-Loop Voltage Gain versus Frequency



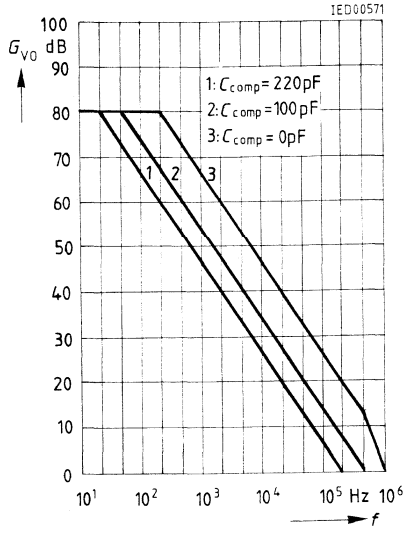
Phase Response versus Frequency

$V_S = \pm 10$ V, $T_j = 25$ °C



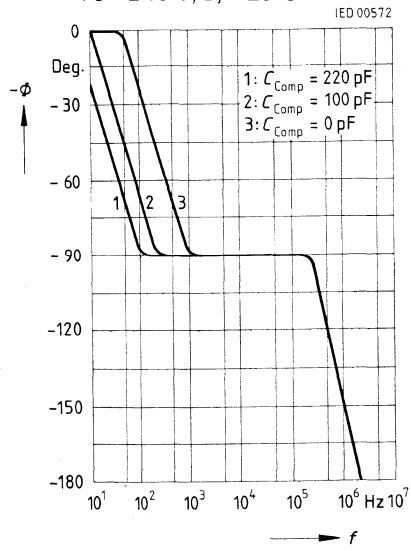
TCA 2465 A, G Open-Loop Voltage Gain versus Frequency

$V_S = \pm 10$ V, $T_j = 25$ °C



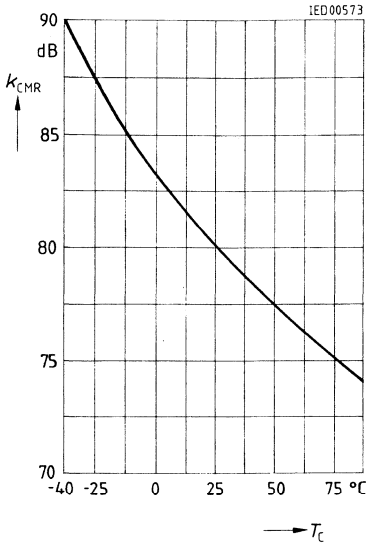
TCA 2465 A, G Phase Response versus Frequency

$V_S = \pm 10$ V, $T_j = 25$ °C

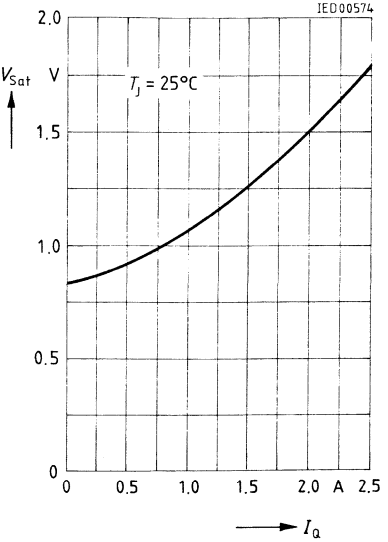


10

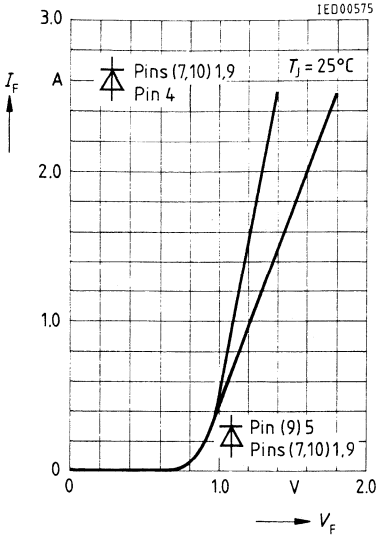
Common-Mode Rejection versus Case Temperature
$V_S = \pm 10$ V



Saturation Voltage versus Peak Output Current
$T_j = 25$ °C



Forward Current versus Forward Voltage



Note: Numbers in brackets refer to TCA 2465 A.

SIEMENS

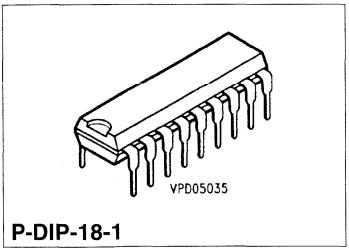
DC Motor Driver

TLE 4201

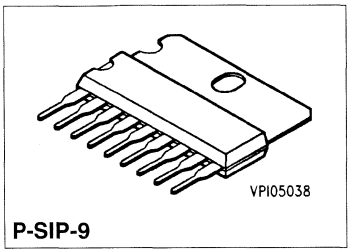
Bipolar IC

Features

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection



P-DIP-18-1



P-SIP-9

Type	Ordering Code	Package
■ S TLE 4201 A1	Q67000-A8080	P-DIP-18-1
■ S TLE 4201 S1	Q67000-A2285	P-SIP-9

■ Not for new design

10

The TLE 4201 IC is a dual comparator that is particularly suitable for driving reversible DC motors and may also be used as a versatile power driver.

The push-pull power-output stages work in switch mode and can be combined into a full-bridge configuration.

Driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

The TLE 4201 IC comes in two different packages: with the P-SIP-9 package it is possible to remove the heat by way of a cooling fin to a suitable heat sink, whereas with the P-DIP-18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

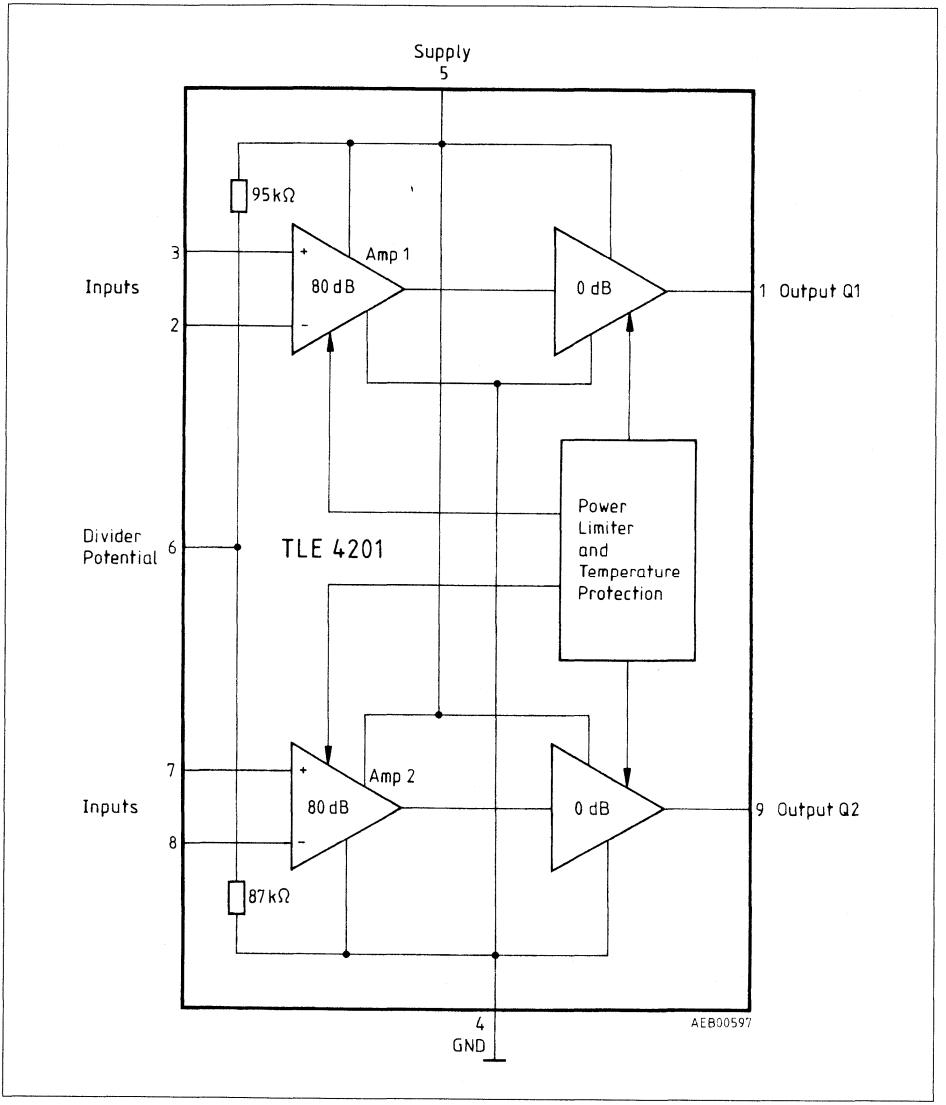


Figure 1
Block Diagram

Pin Definitions and Functions

TLE 4201 A1 Pin	TLE 4201 S1 Pin	Function
1	1	Output of 1st amplifier
2	2	Inverting input of 1st amplifier
3	3	Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7	7	Non-inverting input of 2nd amplifier
8	8	Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18		Ground; to be connected to pin 4

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of ± V_S ±. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SOA protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_S/2$ is available at pin 6 (**see application circuit 2**). This makes the IC particularly suitable as power driver for digital circuits.

10

Application

Figure 2 shows a window discriminator operation with the control voltage V_1.

The window within which the motor is to stop is set by R_2.

Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application Circuits

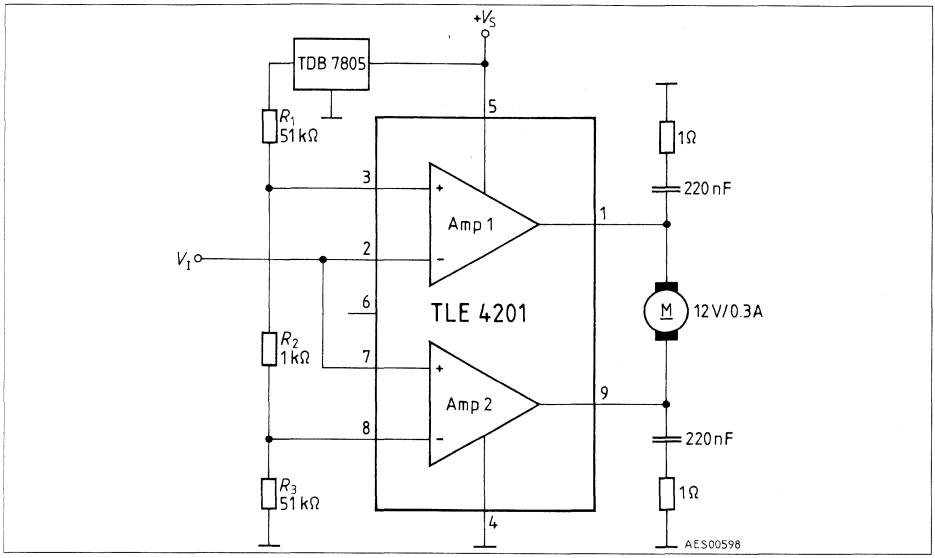


Figure 2
Operated as Window Discriminator
for Input Signals Applies: H ≥ 0.6 V_S, L ≤ 0.3 V_S

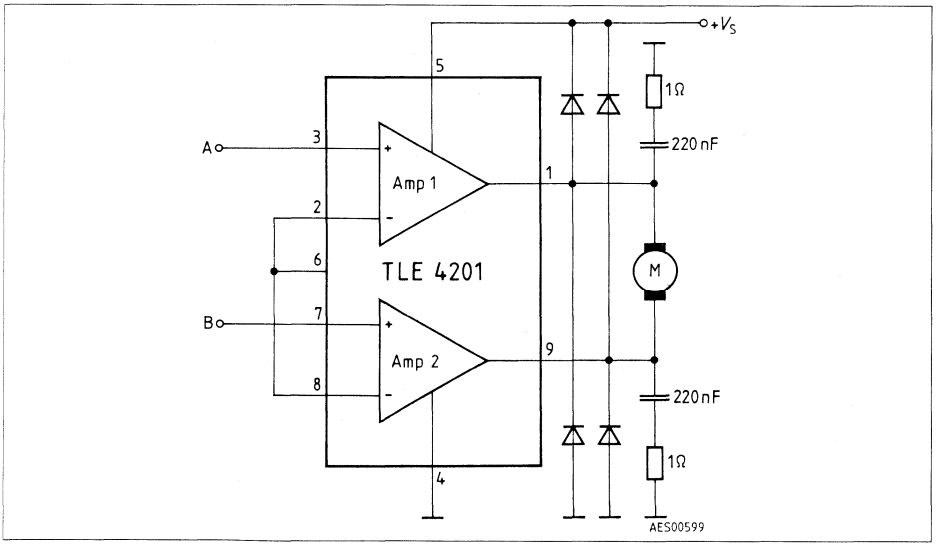


Figure 3
Digital Control

Absolute Maximum Ratings

T_C = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	–	25	V
Supply voltage ($t \leq 50$ ms)	V_S	–	36	V
Output current	I_Q	–	2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	– 0.3	V_S	V
Voltage of pins 1, 9	V	– 0.3	–	V
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 55	125	°C
Thermal resistance				
TLE 4201 S1 system - air	$R_{th\,JA}$	–	65	K/W
system - case	$R_{th\,JC}$	–	8	K/W
TLE 4201 A1 system - air[1)]	$R_{th\,JA}$	–	60	K/W
system - PC board[1)]	$R_{th\,JA1}$	–	44[1)]	K/W

Operating Range

Supply voltage	V_S	3.5	17	V
Case temperature	T_C	– 40	85	°C
Voltage gain (at negative feedback with external components)	G_V	25	–	dB

Characteristics

V_S = 13 V, T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	
		min.	typ.	max.			
Supply current	I_S	–	20	30	mA	**figure 4:** S =1	
Open-loop voltage gain	G_{V0}	–	80	–	dB	f = 500 Hz	
Input resistance	R_I	1	5	–	MΩ	f = 1 kHz	
Saturation voltages						**figure 5:**	S =1
Source operation	$V_{Q\,10}$	–	1.0	1.1	V	I_Q = 0.3 A	1
			1.2	1.6	V	I_Q = 1.0 A	1
Sink operation	$V_{Q\,20}$	–	0.35	0.5	V	I_Q = – 0.3 A	2
			0.7	1.0	V	I_Q = – 1.0 A	2
Rise time of V_Q	t_r	–	1.5	–	µs	**figure 4 and 6**	
Fall time of V_Q	t_f	–	1.5	–	µs	**figure 4 and 6**	
Turn-ON delay time	t_{ON}	–	3.0	–	µs	**figure 4 and 6**	
Turn-OFF delay time	t_{OFF}	–	1.5	–	µs	**figure 4 and 6**	
Input current (pins 2, 3, 7, 8)	I_I	–	1.5	3.0	µA	**figure 5,** $V_{2,3,7,8,}$ = 0	
Input offset voltage	V_{I0}	– 5	–	5	mV	**figure 7**	

[1)] **see figure 8**

10

Test and Measurement Circuits

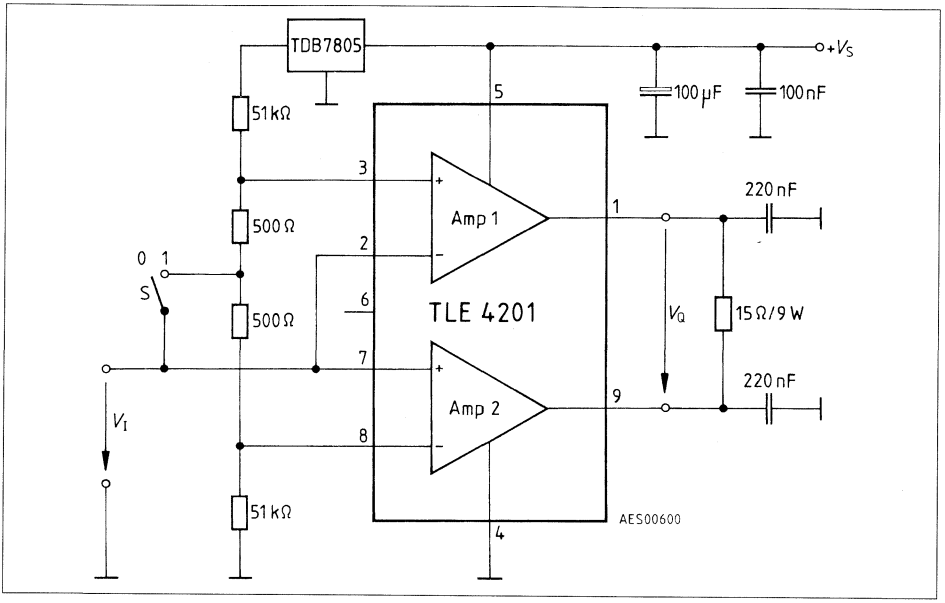


Figure 4

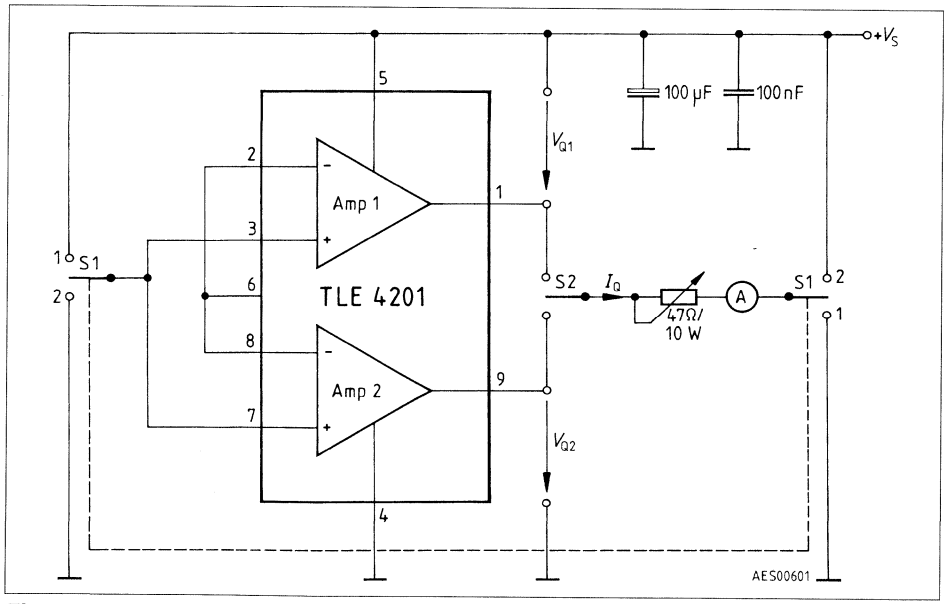


Figure 5

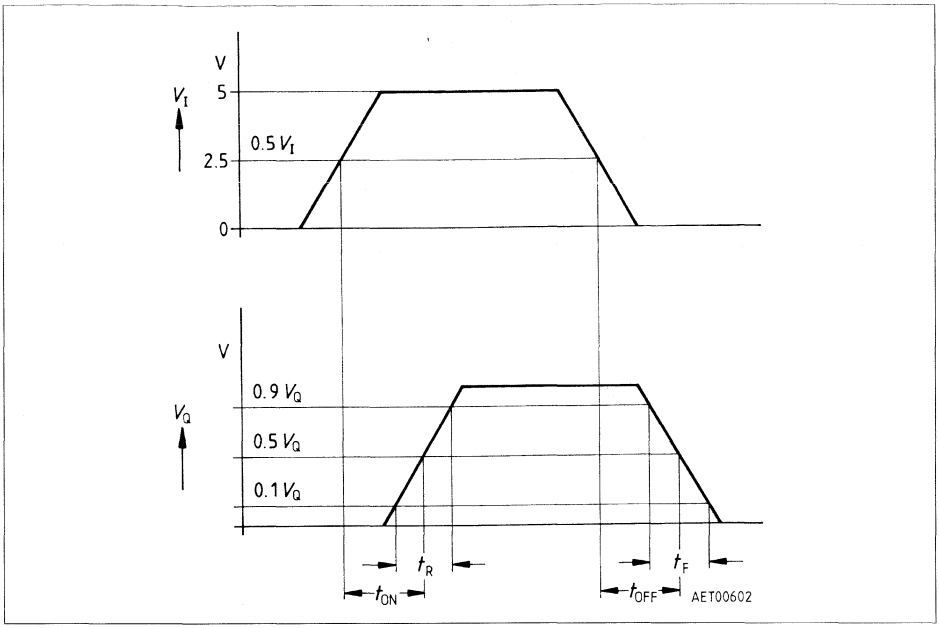


Figure 6
Pulse Diagram

10

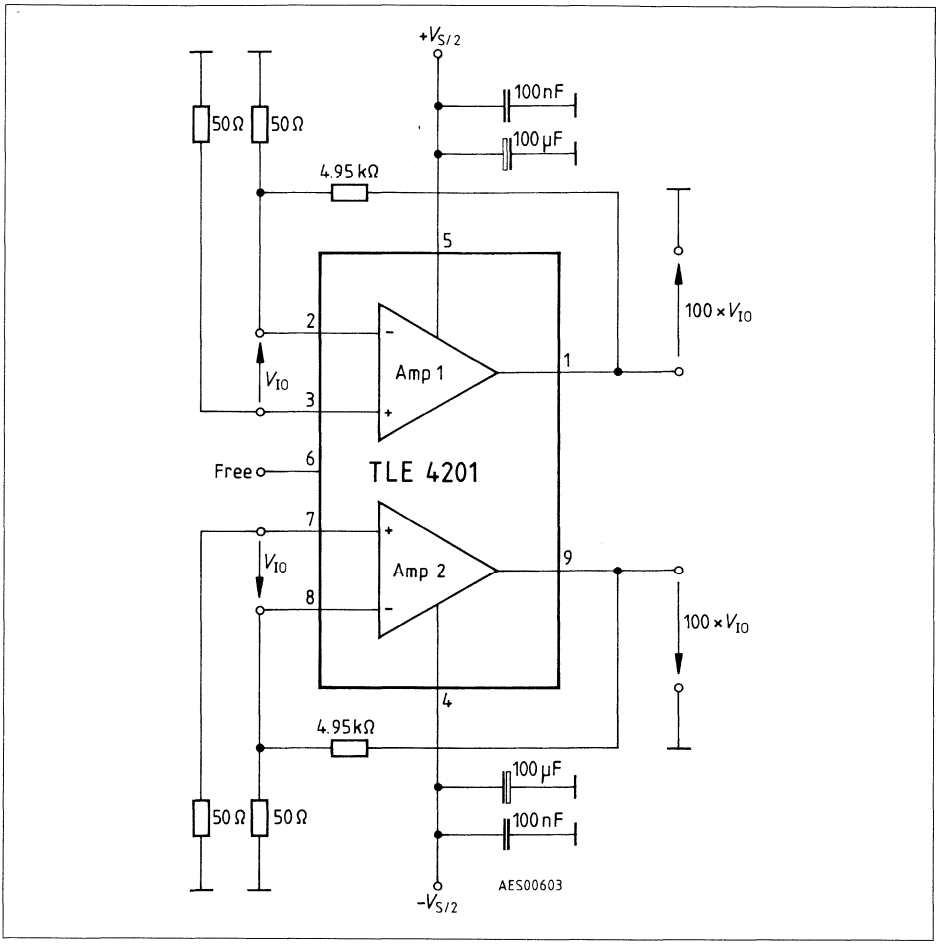


Figure 7
Test and Measurement Circuit

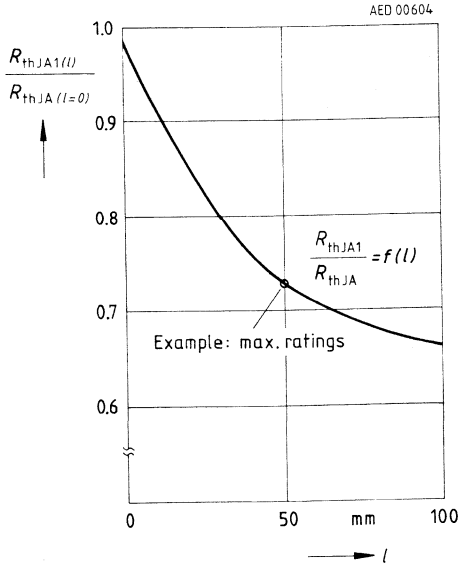
Input Offset Voltages

Thermal Resistance of TLE 4201 A1

Thermal resistance, junction-air, $R_{th\,JA\,1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\,JA}$ $(l = 0)$ = 60 K/W
$T_A \leq 70$ °C
P_V = 1 W
substrate vertical
circuit vertical
still air

Figure 8



10

SIEMENS

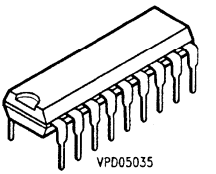
Motor Driver

TLE 4205

Bipolar IC

Features

- Max. driver current 1 A
- Integrated free-wheeling diodes
- Shortcircuit-proof to ground
- Inhibit
- ESD-protected inputs
- Temperature range – 40 °C ≤ T_j ≤ 150 °C



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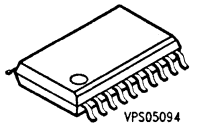
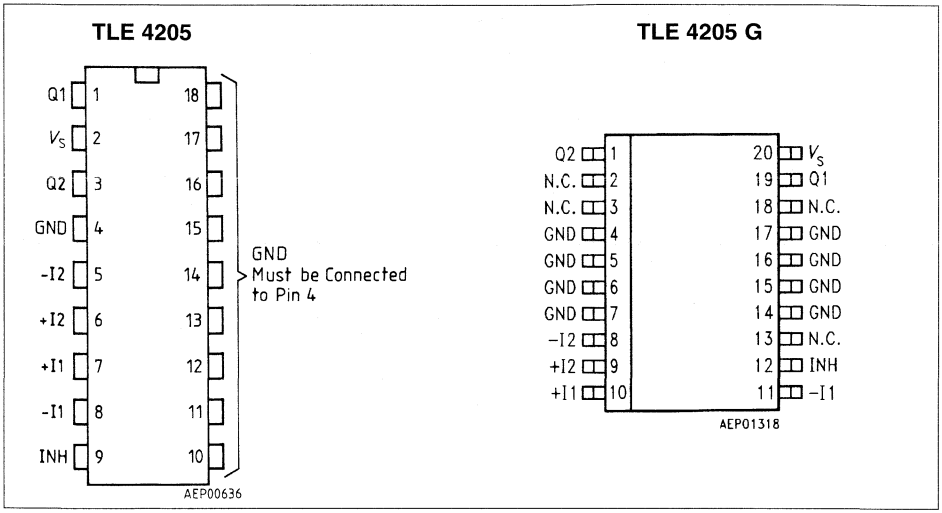


P-DSO-20-1

Type	Ordering Code	Package
S TLE 4205	Q67000-A9025	P-DIP-18-1
S ▼ TLE 4205 G	Q67000-A9114	P-DSO-20-1 (SMD)

▼ New type

TLE 4205 is an integrated power full-bridge DC motor driver for a wide temperature range, as required in automotive applications for example. The circuit contains two power comparators that can be combined to a full-bridge circuit. For inductive loads there are integrated free-wheeling diodes to + V_S and ground. The outputs are shortcircuit-proof from 18 V to ground and turn off when overtemperature occurs. This IC is especially suitable for headlight-beam adjustment in automobiles.



Pin Configuration
(top view)

Pin Definitions and Functions (TLE 4205)

Pin	Symbol	Function
1	Q1	**Output Q1 of channel 1;** push-pull B output with DC short-circuit protection to ground. Integrated free-wheeling diodes to ground and the supply voltage.
2	V_S	**Supply voltage V_S;** must be blocked to ground with a ceramic capacitor of at least 100 nF directly on the pins of the IC.
3	Q2	**Output Q2 of channel 2;** see pin 1.
4	GND	**Ground**
5	– I2	**Inverting input channel 2;** to be wired according to general rules.
6	+ I2	**Non-inverting input channel 2;** to be wired according to general rules.
7	+ I1	**Non-inverting input channel 1;** see pin 6.
8	– I1	**Inverting input channel 1;** see pin 5.
9	INH	**Inhibit;** the IC is passive when this pin is open or connected to ground.
10-18	GND	**Ground;** must be connected to pin 4.

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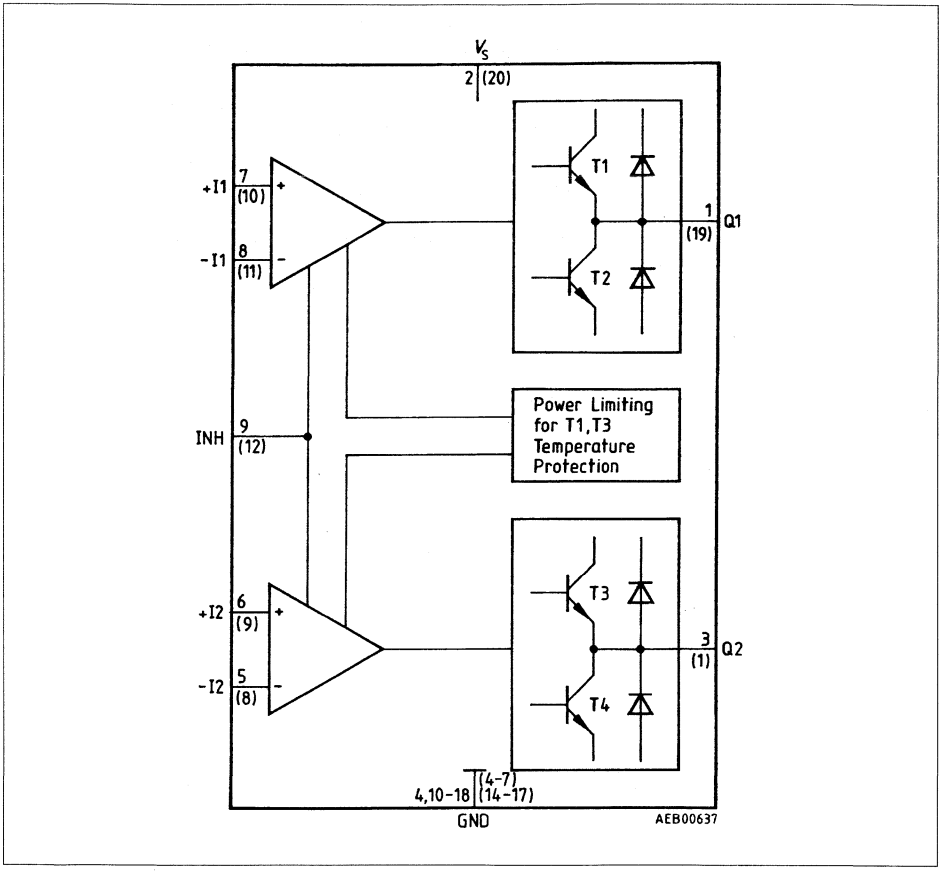
Pin Definitions and Functions (TLE 4205 G)

Pin	Symbol	Function
1	Q1	**Output 1 of channel 1;** push-pull B output with DC short-circuit protection to ground. Integrated free-wheeling diodes to ground and the supply voltage.
2	N.C.	Not connected
3	N.C.	Not connected
4-7	GND	**Ground**
8	– I2	**Inverting input channel 2;** to be wired according to general rules.
9	+ I2	**Non-inverting input channel 2;** to be wired according to general rules.
10	+ I1	**Non-inverting input channel 1;** see pin 6.
11	– I1	**Inverting input channel 1;** see pin 5.
12	INH	**Inhibit;** the IC is passive when this pin is open or connected to ground.
13	N.C.	Not connected
14-17	GND	**Ground**
18	N.C.	Not connected
19	Q2	**Output Q2;** must be connected to pin 4.
20	V_S	**Supply voltage;** must be connected to pin 4.

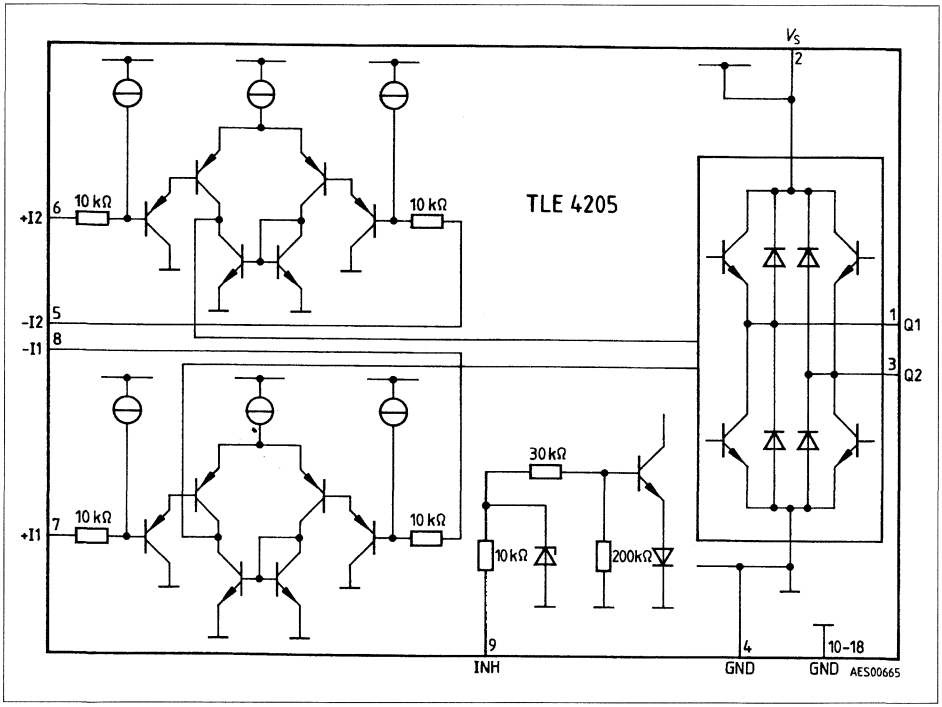


Block Diagram

Circuit Description

The IC contains two amplifiers with typical open-loop gain of 80 dB at 500 Hz.

The input stages consist of PNP differential amplifiers. This produces a common-mode input range of 0 V to nearly V_S and a maximum differential input voltage of V_S. The IC is guarded against ground shorts by an SOA protective circuit. The output transistors are turned off if the chip temperature exceeds approx. 160 °C. The IC can be turned off by an inhibit input, which very much reduces current consumption.



Circuit Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 0.3	45	V	
Differential input voltage	V_{ID}	–	± V_S	V	$\Delta V_{6\text{-}5}$ or $\Delta V_{7\text{-}8}$ TLE 4205 $\Delta V_{8\text{-}9}$ or $\Delta V_{10\text{-}11}$ TLE 4205G
Output current	I_Q	– 1	1	A	–
Supply current	I_S	2.5	3	A	–
Ground current	I_{GND}	– 3	2.5	A	I2
Input voltage	V_I	– 15	+ V_S	V	V_5; V_6; V_7; V_8 TLE 4205 V_8; V_9; V_{10}; V_{11} TLE 4205G
Inhibit input	V_9	– 15	+ V_S	V	–
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Operating Range

Supply voltage	V_S	6	32	V	–
Case temperature	T_C	– 40	105	°C	P_{Dmax} = 3 W
Thermal resistance					
junction - ambient	$R_{th\ JA}$	–	60	KW	TLE 4205
junction - case	$R_{th\ JC}$	–	15	KW	TLE 4205
Thermal resistance					
junction - ambient	$R_{th\ JA}$	–	65	KW	TLE 4205 G
junction - case	$R_{th\ JC}$	–	3	KW	TLE 4205 G

Outputs pin 1 and pin 3 shortcircuit-proof to GND at $V_S \leq$ 18 V

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Characteristics

V_S = 13.5 V; T_j = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Open-circuit current consumption	I_S	–	10	30	mA	active
Open-circuit current consumption	I_S	–	10	100	µA	inhibit
Turn-ON dead time ref. to $V_{9\ OFF/ON}$	t_{dON}	–	10	20	µs	$\lvert I_{1,3} \rvert < 1$ A TLE 4205 $\lvert I_{1,19} \rvert < 1$ A TLE 4205 G
Turn-OFF dead time ref. to $V_{9\ OFF/ON}$	t_{dOFF}	–	10	20	µs	$\lvert I_{1,3} \rvert < 1$ A TLE 4205 $\lvert I_{1,19} \rvert < 1$ A TLE 4205G
Open-loop gain	G_{VO}	50	80	–	dB	f = 500 Hz
Inputs						
Input zero voltage	V_{IO}	– 7.5	–	7.5	mV	R_S = 10 kΩ; – 40 °C ≤ T_j ≤ 85 °C
Input-voltage drift	$\Delta V_{IO}/\Delta T$	–	20	30	µV/K	– 40 °C ≤ T_j ≤ 85 °C
Input zero current	I_{IO}	– 75	–	75	mA	– 40 °C ≤ T_j ≤ 85 °C
Input current	I_I	– 300	–	300	nA	– 40 °C ≤ T_j ≤ 85 °C
Input-current drift	$\Delta I/\Delta T$	–	–	5	nA/K	– 40 °C ≤ T_j ≤ 85 °C
Input common-mode range, positive	V_{IC}	–	–	V_S – 2	V	–
Input common-mode range, negative	V_{IC}	–	–	– 0.5	V	–
Power-supply rejection ratio	$PSRR$	–	–	200	µV/V	R_S = 10 kΩ; – 40 °C ≤ T_j ≤ 85 °C
Common-mode rejection ratio	$CMRR$	70	80	–	dB	–

Characteristics (cont'd)
V_S = 13.5 V; T_j = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs						
Saturation voltage	V_{Satu}	–	1.0	1.5	V	I_Q = 0.6 A; – 40 °C ≤ T_j ≤ 85 °C
Saturation voltage	V_{Sat1}	–	1.0	1.5	V	I_Q = 0.6 A; – 40 °C ≤ T_j ≤ 85 °C
Forward voltage of free-wheeling diode	V_{Fu}	–	1.0	1.5	V	I_Q = 0.6 A; – 40 °C ≤ T_j ≤ 85 °C
Forward voltage of free-wheeling diode	V_{F1}	–	1.0	1.5	V	I_Q = 0.6 A; – 40 °C ≤ T_j ≤ 85 °C
Slew rate of V_Q	dV_Q/dt_r	–	0.5	–	V/µs	–
Inhibit Input						
Switching threshold high	V_{IH}	2	–	–	V	–
Switching threshold high	V_{IL}	–	–	0.8	V	–
H-input current	I_{IH}	–	100	–	µA	V_9 = 5 V
L-input current	I_{IL}	–	0	–	µA	V_9 = 0 V

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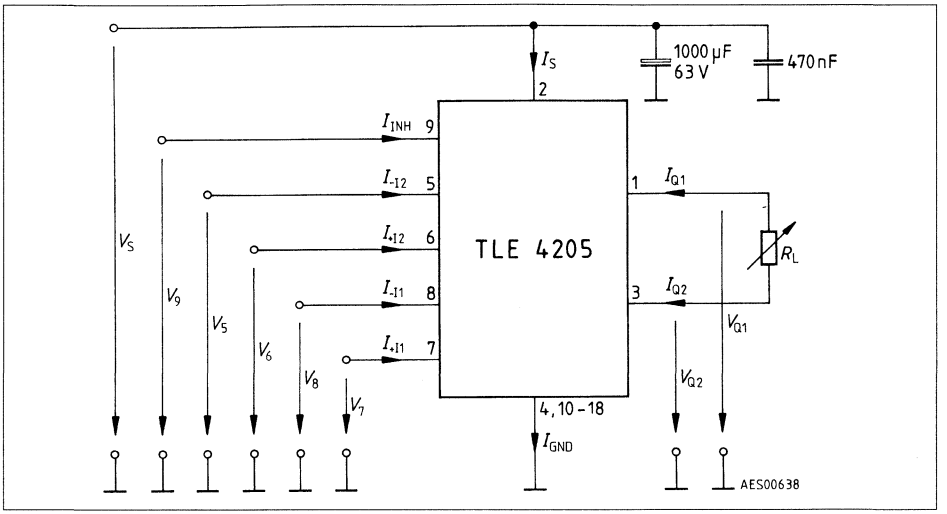
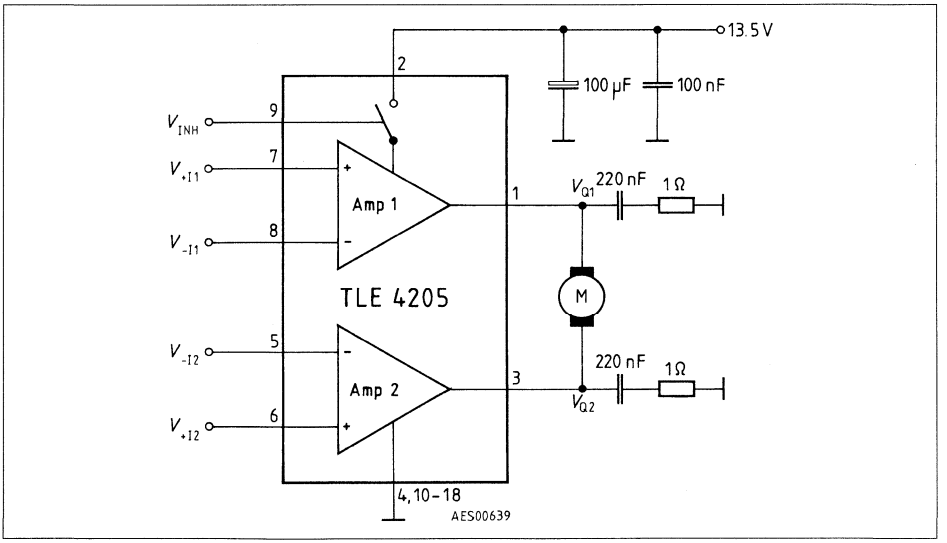
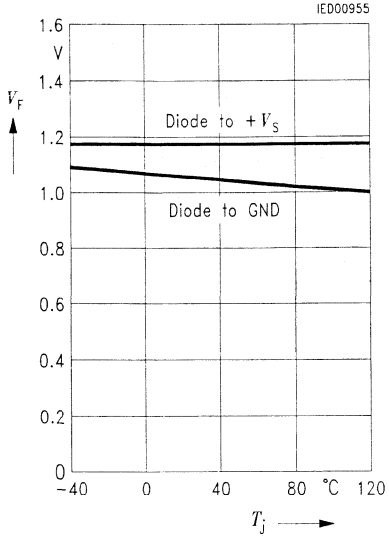


Test Circuit

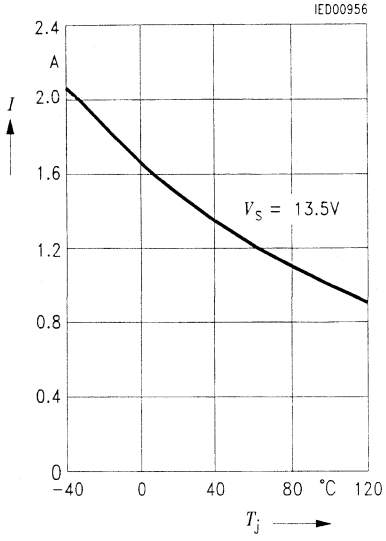


Application Circuit

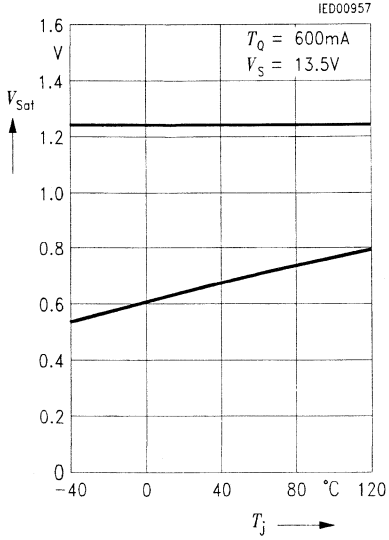
Forward Voltage of the Free-Wheeling Diodes versus Junction Temperature



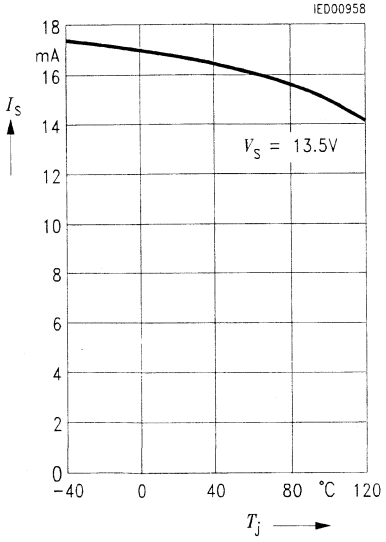
Start Point of the SOA Protection Circuit versus Junction Temperature



Saturation Voltage versus Junction Temperature



Current Consumption versus Junction Temperature



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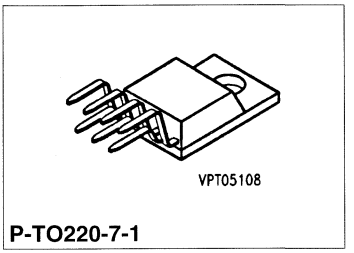
SIEMENS

DC Motor Driver

TLE 4202

Bipolar IC



P-TO220-7-1

Features

- Max. output current 3.0 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA circuit
- Temperature protection
- Short-circuit proof to ground
- Suitable for applications in automotive engineering

Type	Ordering Code	Package
S ■ TLE 4202	Q67000-A8007	P-TO220-7-1

■ Not for new design

The TLE 4202 IC is a dual comparator that is particularly suitable as a driver for reversible DC motors and may also be used as a versatile power driver.

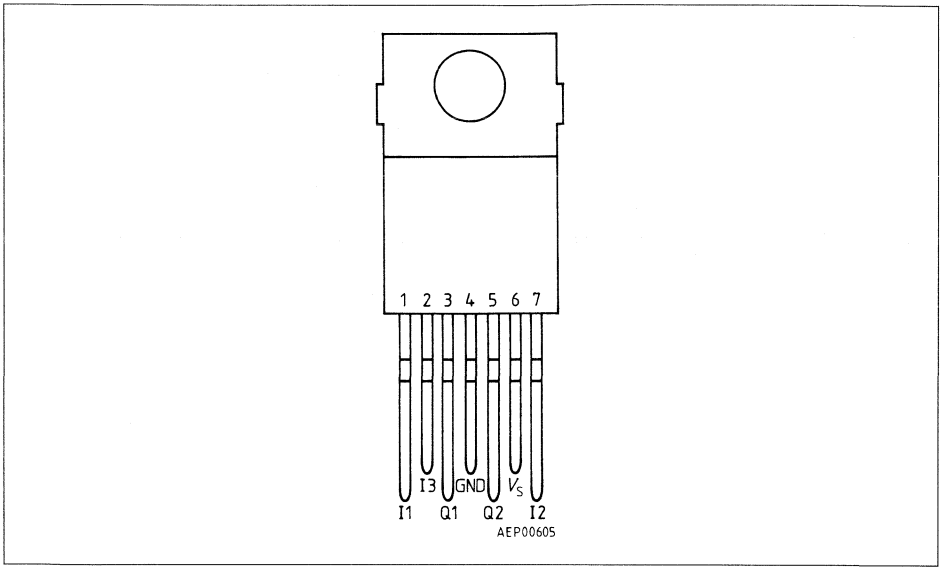
The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for applications in motor vehicles. It can be applied at package temperatures between – 40 °C and 130 °C.

The comparators can be driven analogically in form of a window discriminator or simply by digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanism, etc.

Circuit Description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low residual voltages at the sink transistor, the drive circuit of the sink transistor is connected to the supply voltage. An SOA circuit protects the IC against ground short- circuits.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	I1	**Input** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input** Inverting input of the two comparators, to be connected according to general rules
3	Q1	**Output Q1** Push-pull B output DC-short-circuit proof to ground
4	GND	**Ground**
5	Q 2	**Output Q2** see pin 3
6	V_S	**Supply voltage** V_S Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	**Input** Non-inverting input I2, see pin 1

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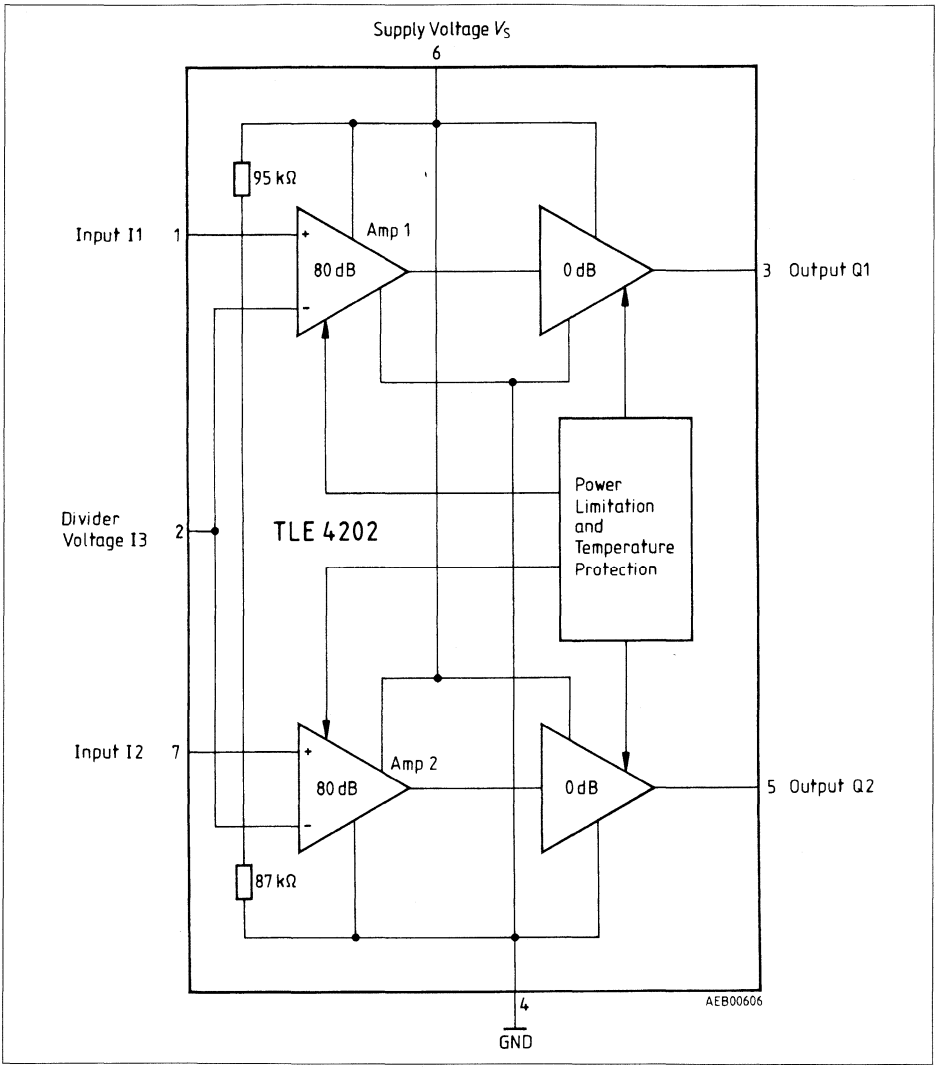


Block Diagram

Absolute Maximum Ratings

T_C = – 40 to 130 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	–	25	V
Supply voltage ($t \leq 50$ ms)	V_S	–	36	V
Output current $T_C \leq 85$ °C	I_Q	– 3.0	3.0	A
Voltage at pins 1, 2, I3	$V_{1,2,7}$	– 0.3	V_S	V
Voltage at the pins Q1, Q2	$V_{3,5}$	– 0.7	V_S + 0.7	V
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 55	125	°C

Operating Range

Package temperature during operation	T_C	–	–	–
$R_L \geq 11\ \Omega$, V_S = 7 ... 16 V		– 40	–	°C
$R_L \geq 18\ \Omega$, V_S = 16 V		–	130	°C
Voltage gain (at negative feedback with external connection)	G_V	30	–	dB
Thermal resistance system - case	$R_{th\,SC}$	–	4.8	K/W

Outputs Q1 and Q2 short-circuit proof to ground
R_L: Resistance between output 1 and output 2

10

Characteristics

V_S = 13 V, T_C = 25 °C

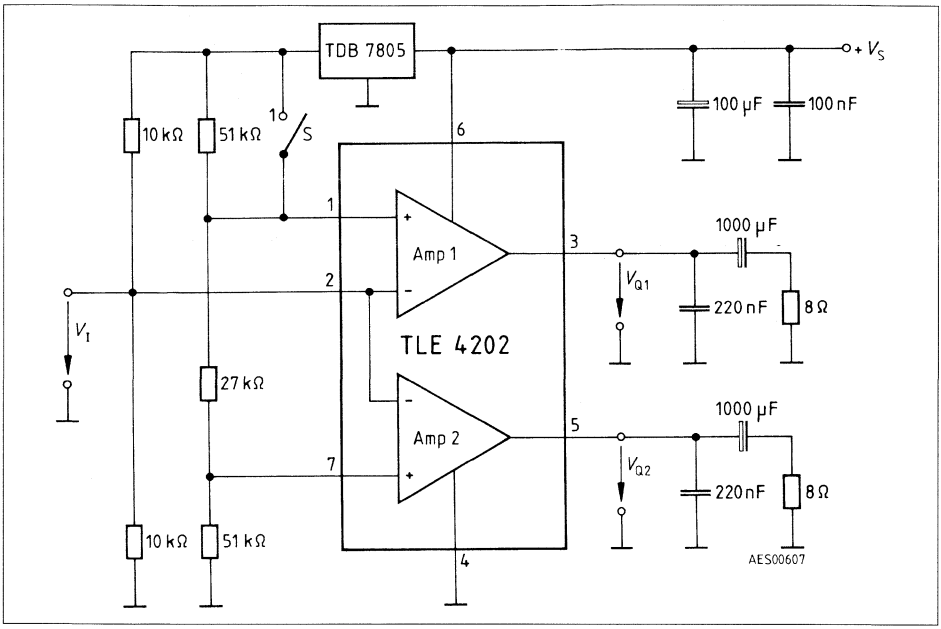
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
General Characteristics							
Quiescent current	I_q	–	15	25	mA	S = 1	1
Open-loop voltage gain	G_{VO}	50	80	–	dB	f = 500 Hz[1)]	1
Input Characteristics							
Input current (pins I1, I2)	$I_{I1,7}$	–	1.5	3.0	µA	$V_{I1,12}$ = 0	2
Input resistance	$R_{I1,7}$	1	5	–	MΩ	f = 1 kHz	1
Input offset voltage	V_{I0}	– 20	–	20	mV	–	3

[1)] – 40 °C ≤ T_C ≤ 110 °C
7 V ≤ V_S ≤ 16 V

Characteristics (cont'd)
V_S = 13 V, T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Output Characteristics							
Source operation	V_{Sato}	–	1.0	1.1	V	I_Q = – 0.3 A S1 = 1	2
		–	1.2	1.6	V	I_Q = – 1.0 A S1 = 1	2
		–	1.3	2.0	V	I_Q = – 1.5 A S1 = 1[1]	2
Sink operation	V_{Satu}	–	0.35	0.5	V	I_Q = + 0.3 A S1 = 2	2
		–	0.7	1.0	V	I_Q = + 1.0 A S1 = 2	2
		–	0.8	1.5	V	I_Q = + 1.5 A S1 = 2[1]	2
Short-circuit current	$I_{Q\,max}$	–	1.25	1.60	A	Source operation[1]	2
Slew-rate (falling edge)	SR	6	–	–	V/µs	–	1
Slew-rate (rising edge)	SR	6	–	–	V/µs	–	1
Switching Times							
Rise time of V_Q	t_r	–	1.5	–	µs	–	1
Falling time of V_Q	t_f	–	1.5	–	µs	–	1
Turn-ON delay	t_{ON}	–	3.0	–	µs	–	1
Turn-OFF delay	t_{OFF}	–	1.5	–	µs	–	1

[1] – 40 °C ≤ T_C ≤ 110 °C
7 V ≤ V_S ≤ 16 V



Test Circuit 1

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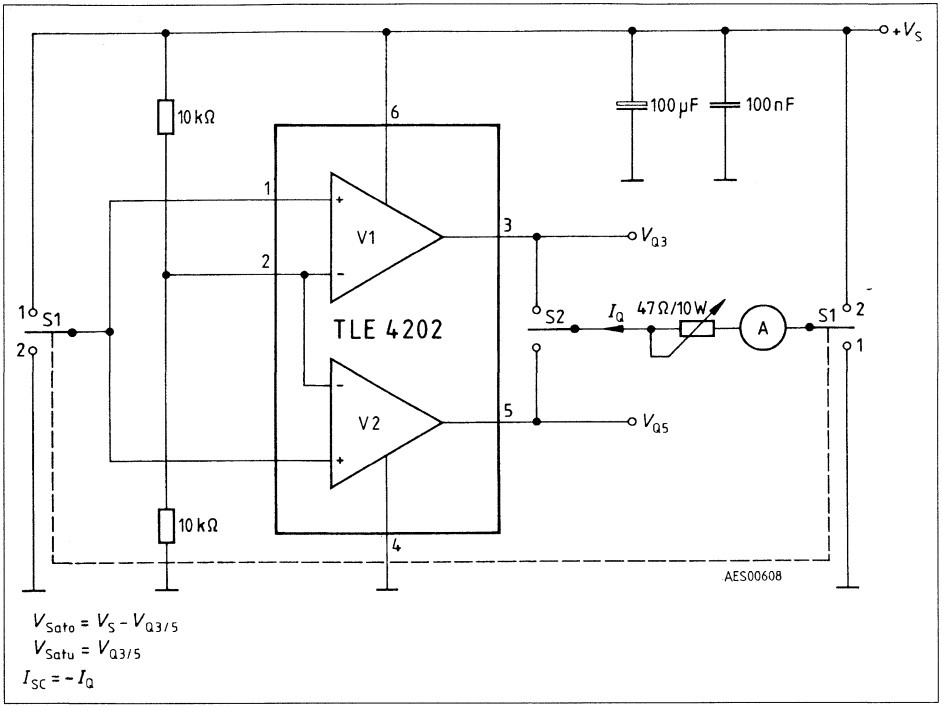
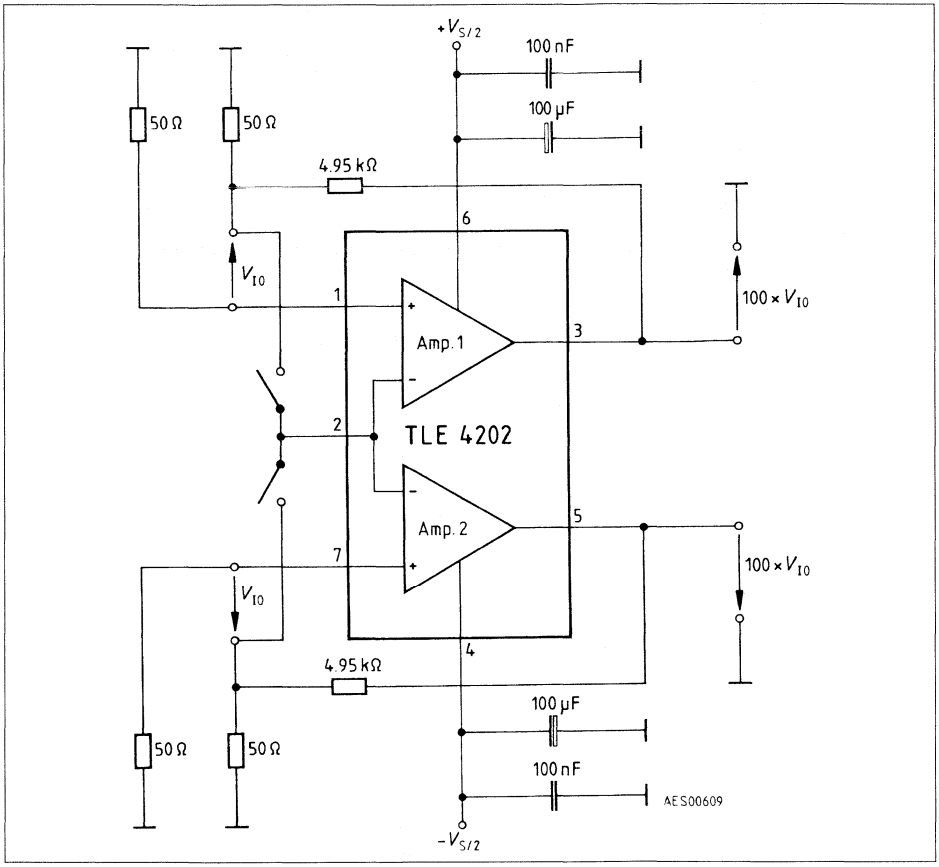


Test Circuit 2



Test Circuit 3

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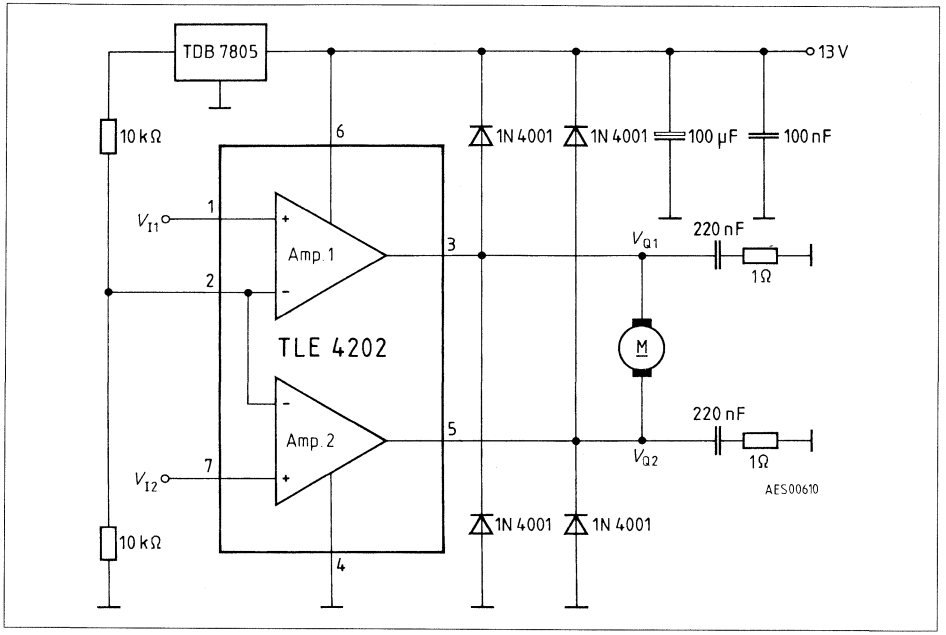
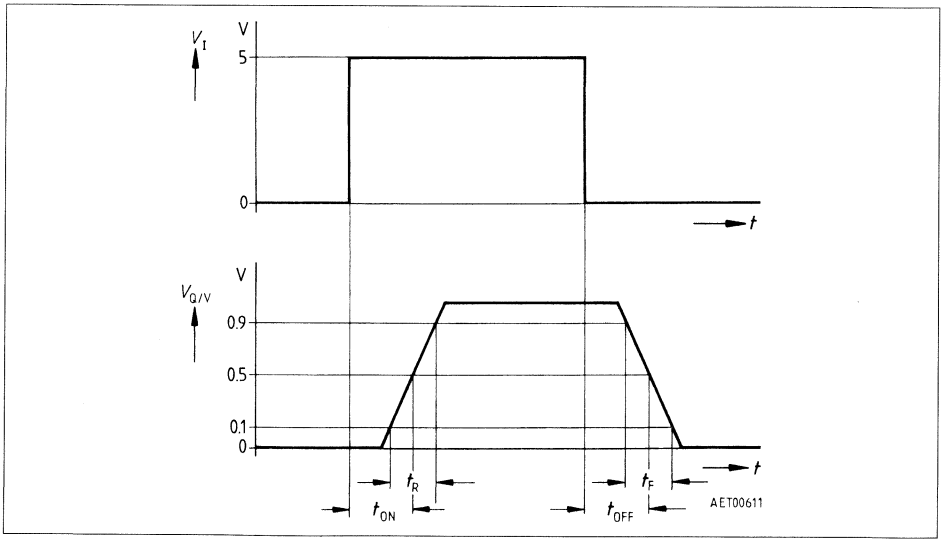


Application Circuit



Diagram

2-A DC Motor Driver

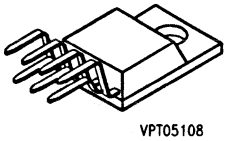
TLE 4202 B

Preliminary Data

Bipolar IC

Features

- Drives motors up to 2 A
- Integrated free-wheeling diodes 2.5 A
- Short-circuit proof to ground
- Overtemperature protection
- Low saturation voltages through bootstrap
- Wide temperature range
- Suitable for applications in automotive engineering



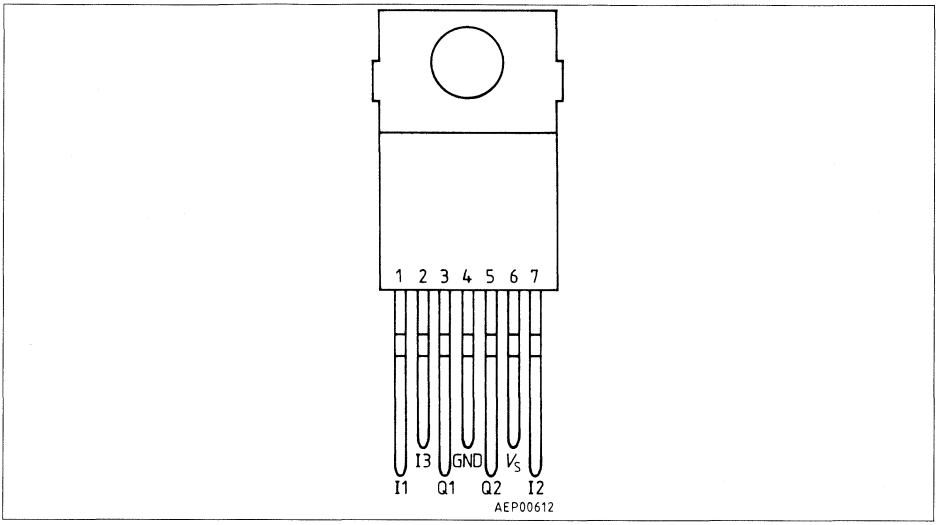
P-TO220-7-1

Type	Ordering Code	Package
S TLE 4202 B	Q67000-A8225	P-TO220-7-1

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for application in motor vehicles. It can be applied at package temperatures between – 40 °C and 130 °C.

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz.

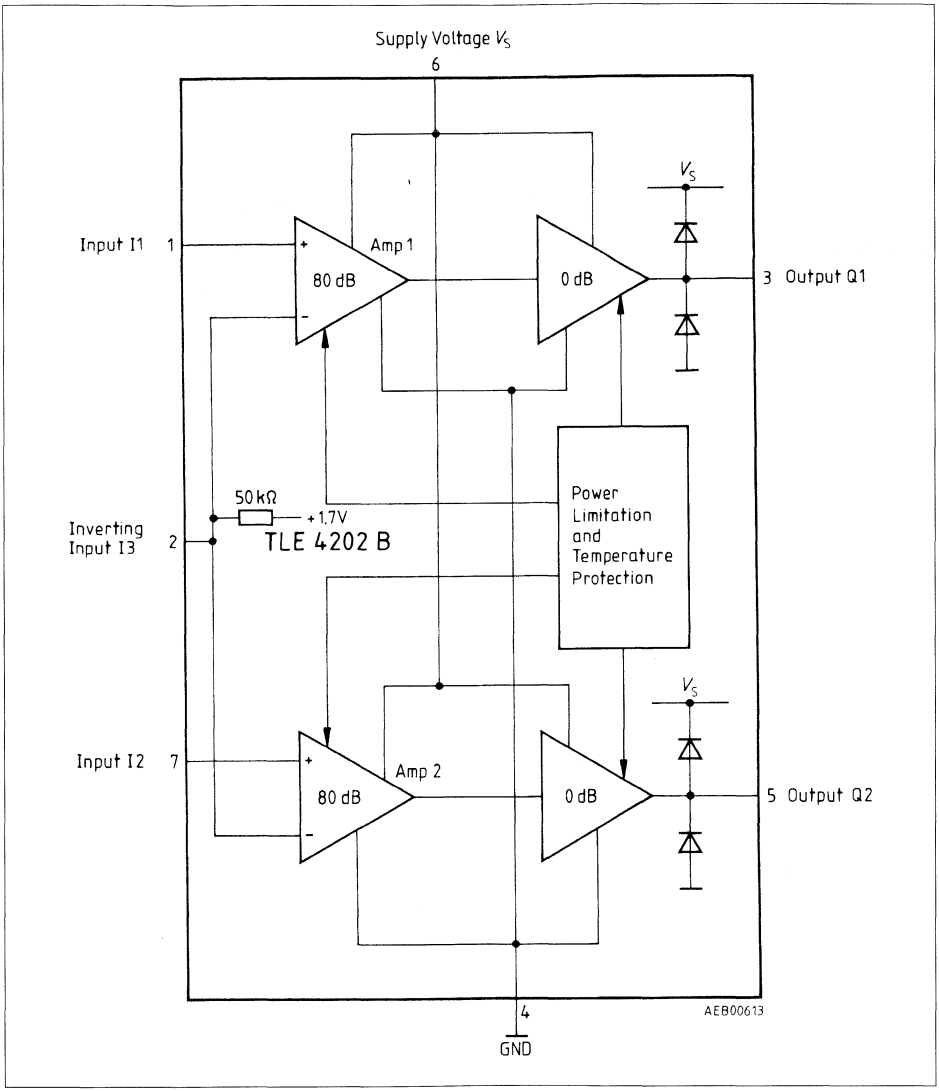
The input stages are PNP differential amplifiers thus resulting in a common-mode input voltage range from 0 V to approx. the value of V_S and in a maximum input differential voltage of V_S. To obtain low saturation voltages at the sink circuit, the drive circuit of the sink transistor is connected to the supply voltage. An SOA protective circuit protects the IC against ground short-circuits. At chip temperatures above approx. 160 °C the source transistors are turned off.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	I1	**Input 1** Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	**Inverting input 3** Inverting inputs of the two comparators; internally connected to reference voltage across 50 kΩ (typ. 1.7 V)
3	Q1	**Output Q1** Push-pull output B DC-short-circuit proof to ground. Integrated free-wheel diodes to ground and to supply voltage
4	GND	**Ground**
5	Q2	**Output Q2,** see pin 3
6	V_S	**Supply voltage** Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	**Input 2** Non-inverting input 2; see pin 1



Block Diagram

Absolute Maximum Ratings
T_C = – 40 to 130 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	–	40	V
Output current of sink transistors $T_C \leq 85$ °C	I_Q	–	2.5	A
Output current of source transistors internally limited	I_Q	–	–	–
Diode peak currents				
to + V_S	I_{F+}	–	2.5	A
to ground	I_{F-}	–	2.5	A
Voltage at pins I1, I2, I3	$V_{1,2,7}$	– 0.3	V_S	V
Voltage at pins Q1, Q2 [1]	$V_{3,5}$	–	–	V
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 55	125	°C

Operating Range

Supply voltage	V_S	3.5	17	V
Case temperature during operation	T_C			
$R_L \geq 6\ \Omega$, V_S = 7 ... 16 V		– 40	–	°C
$R_L \geq 9\ \Omega$, V_S = 16 V		–	130	°C
Voltage amplification (at negative feedback with external connection)	V_V	30	–	dB
Thermal resistance system - case	$R_{th\,SC}$	–	4	K/W

Outputs Q1 and Q2 short-circuit proof to ground
R_L: Resistance between output 1 and output 2

[1] The output voltages are kept within a permissible range by free-wheel diodes

Characteristics

V_S = 13 V, T_j = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
General Data							
Quiescent current	I_S	–	15	25	mA	S = 1	1
Open-loop gain	G_{VO}	50	80	–	dB	f = 500 Hz $V_S \leq 7$ V ≤ 16 V T_C = – 40 °C to + 110 °C	1
Input Characteristics							
Input current (pins I1, I2)	$I_{I1,7}$	–	1.0	3.0	mA	$V_{I1,12}$ = 0	2
Input current	I_{I2}	–	35	70	mA	V_{I2} = 0; $V_{I1,7} = V_S$	1
	$-I_{I2}$	–	230	300	mA	$V_{I2} \leq V_S$; $V_{I1,7}$ = 0 V	–
Input resistance	$R_{I1,7}$	1	5	–	MΩ	f = 1 kHz	1
Input reference voltage	V_{I2}	1.4	1.7	2.0	V	I_2 = 0; $V_{I1,7}$ = 0 V	1
Input offset voltage	V_{I0}	– 20	–	20	mV	–	3
Output Characteristics							
Saturation voltages							
Source operation	V_{Sato}	–	0.9	1.0	V	I_Q = – 0.3 A S1 = 1	2
measured to V_S	V_{Sato}	–	1.2	1.6	V	I_Q = – 1.0 A S1 = 1	2
	V_{Sato}	–	1.5	2.1	V	I_Q = – 2 A S1 = 1	2
Sink operation	V_{Satu}	–	0.25	0.4	V	I_Q = + 0.3 A S1 = 2	2
			0.5	0.75	V	I_Q = + 1.0 A S1 = 2	2
	V_{Satu}	–	1.0	1.3	V	I_Q = + 2 A S1 = 2	2
Short-circuit current	I_{SC}	–	1.25	1.60	A	V_Q = 0 V	2
Diode forward voltage							
to + V_S	V_{F+}	–	1.0	1.3	V	$I_F = I_Q$ = + 1 A	2
to ground	V_{F-}	–	0.9	1.2	V	$I_F = I_Q$ = – 1 A	2
Slew rate falling edge	SR	–	6	–	V/µs	–	1
Slew rate rising edge	SR	–	6	–	V/µs	–	1
Switching Times							
Rise time of V_Q	t_r	–	1.5	–	µs	–	1
Fall time of V_Q	t_f	–	1.5	–	µs	–	1
Switch-ON delay	t_{ON}	–	3.0	–	µs	–	1
Switch-OFF delay	t_{OFF}	–	1.5	–	µs	–	1

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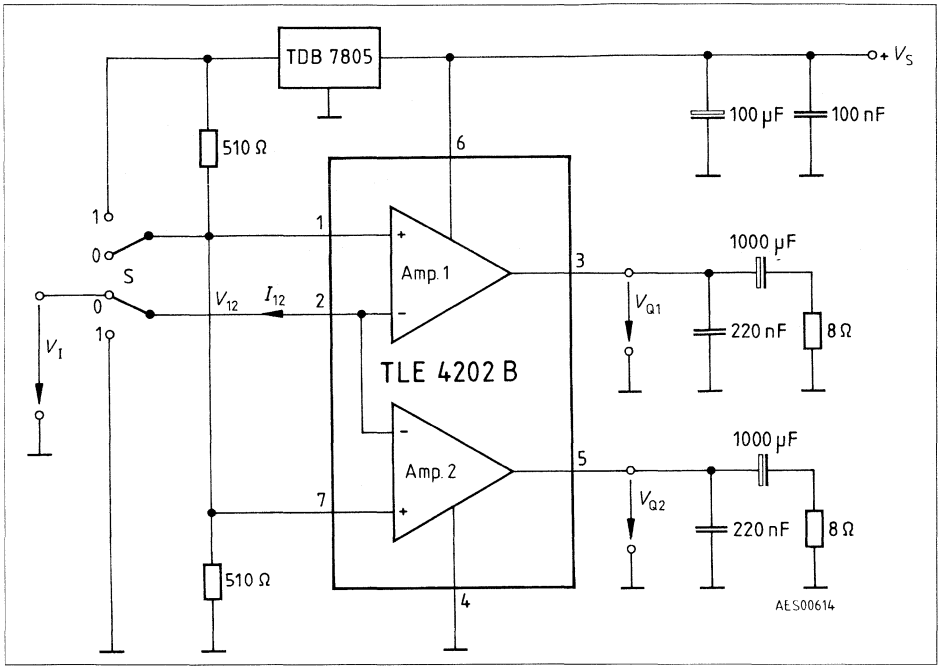
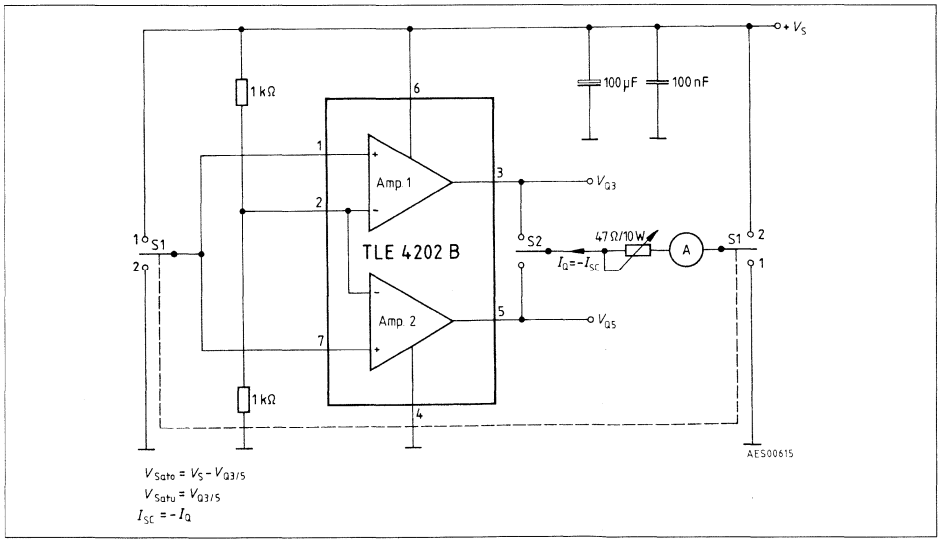
Characteristics (cont'd)
$V_S \leq 7$ V to 17 V; $T_C = -40$ to 110 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Quiescent current	I_S	–	15	30	mA	S = 1	1
Saturation Voltage							
Source operation measured to V_S	V_{Sato}	–	0.9	1.2	V	$I_Q = -0.3$ A; S = 1	2
	V_{Sato}	–	1.2	1.8	V	$I_Q = -1$ A; S = 1	2
	V_{Sato}	–	1.5	2.4	V	$I_Q = -2$ A; S = 1	2
Sink operation	V_{Satu}	–	0.25	0.60	V	$I_Q = 0.3$ A; S1 = 2	2
	V_{Satu}	–	0.5	1.1	V	$I_Q = 1$ A; S1 = 2	2
	V_{Satu}	–	1.2	2.0	V	$I_Q = 2$ A; S1 = 2	2
Short-circuit current	$-I_{SC}$	–	–	3.5	V	$V_Q = 0$ V $T_C = 25$ °C to 110 °C	–



Test Circuit 1



Test Circuit 2

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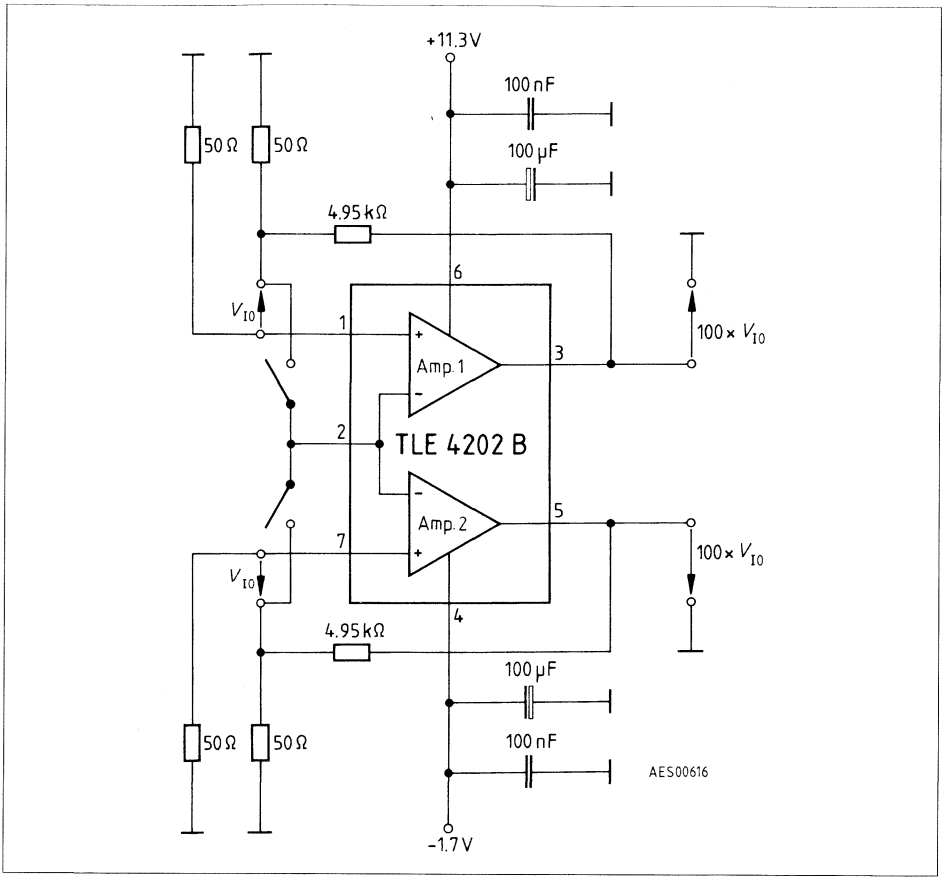
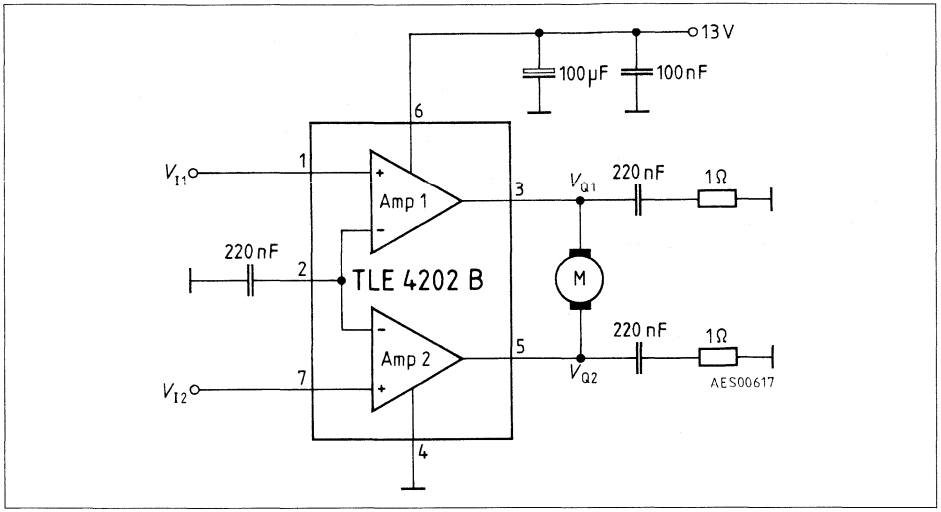
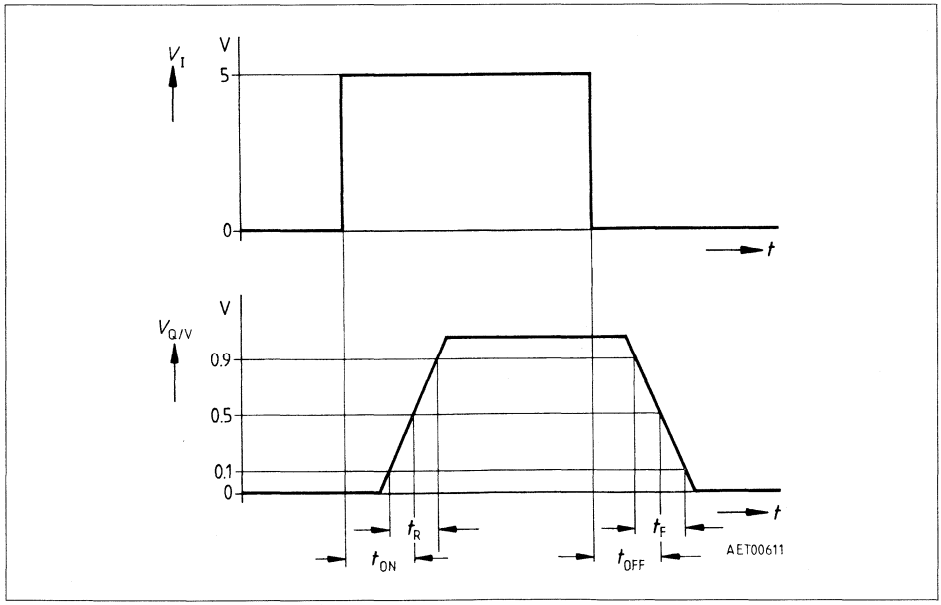


Test Circuit 3



Application Circuit



Diagrams

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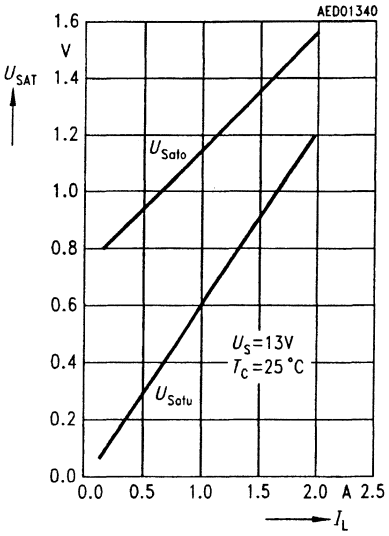
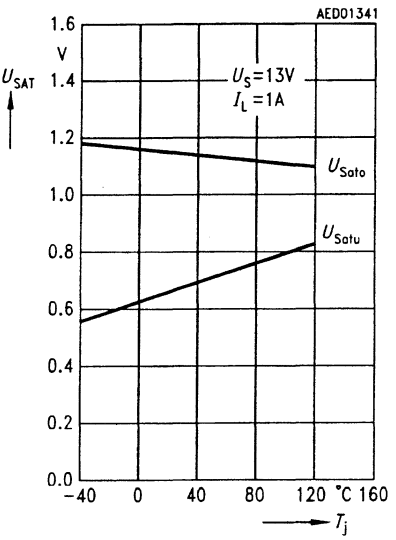
Saturation Voltage versus Output Current



Saturation Voltage versus Temperature



3-A Motor Driver

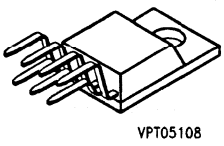
TLE 4204

Preliminary Data

Bipolar IC

Features

- Max. output current 4 A
- Outputs short-circuit proof to $\pm V_S$
- Thermal overload protection
- Integrated free-wheeling diodes to $\pm V_S$
- Max. supply voltage 45 V
- Suitable for automotive applications



P-TO220-7-1

Type	Ordering Code	Package
■ S TLE 4204	Q67000-A8182	P-TO220-7-1

■ Not for new design

Integrated 3 A full-bridge DC motor driver with temperature protection, fully protected output stages and integrated free-wheeling diodes. The case temperature range is – 40°C to 125°C. The IC is also especially suitable for application in automotive electronics.

Application Description

In industrial and automotive electronics full-bridge DC motor drivers are mostly applied in bidirectional motor drives. Both of the differential control inputs act on the outputs as follows:

State	Differential input voltage 1	Differential input voltage 2	Output 1	Output 2
1	< 0	< 0	V_{QL}	V_{QL}
2	< 0	> 0	V_{QL}	V_{QH}
3	> 0	< 0	V_{QH}	V_{QL}
4	> 0	> 0	V_{QH}	V_{QH}

V_{QL} means: Lower power unit conducts; upper power unit is blocked
V_{QH} means: Upper power unit conducts; lower power unit is blocked

Examples:
State 1: Motor is slowed down
State 2: Motor turns right
State 3: Motor turns left
State 4: Motor is slowed down

Circuit Description

Input Circuit

The input stages are designed as differential inputs with an open-loop gain of typ. 80 dB and a common-mode input voltage range to 0 V.

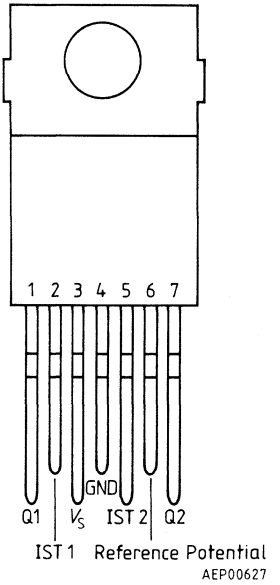
Output Stages

The output stages consist of two push-pull C stages. Using the protective circuits for limiting the power dissipation makes the outputs short-circuit proof to ground and to supply voltage throughout the entire operating range. Positive and negative voltage peaks which occur during switching of inductive loads, are limited by integrated diodes.

Monitoring and Protecting Functions

The IC is protected against thermal overload by a temperature protecting unit.

The power units are controlled by a protection circuit. At low voltages (up to 8 V) only the current is limited in order to protect the bond leads. At higher voltages the protection circuit controls the power dissipation in the power unit.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	**Output of channel 1** Short-circuit proof push-pull C output channel 1 for rated currents up to 3 A. Free-wheeling diodes to $+V_S$ and to ground are integrated.
2	IST1	**Control input for channel 1** Differential input referred to pin 6; of non-inverting effect on output channel 1. The common-mode range is specified from V_S – 2.5 V to ground.
3	V_S	**Supply voltage** Block against ground (pin 4) with a ceramic capacitor of 220 nF min. close to pin 3. For longer connections a low-inductance circuit-proof supporting electrolytic capacitor of at least 10 µF between pin 3 and 4 is to be supplied. The connection is to be designed for the maximum short-circuit current (2 × 4 A).
4	GND	**Ground** Design the connection for the maximum short-circuit current (2 × 4 A).
5	IST2	**Control input channel 2** Differential input referred to pin 6; of non-inverting effect on output 2. The common-mode range is specified from V_S – 2.5 V to ground.
6	Reference potential	**Input reference potential for channel 1 and 2** The user can individually determine the switching threshold with this input. The common-mode range is specified from V_S – 2.5 V to ground.
7	Q2	**Output of channel 2** Short-circuit proof push-pull C output channel 2 for rated currents up to 3 A. Free-wheeling diodes to $+V_S$ and to ground are integrated.

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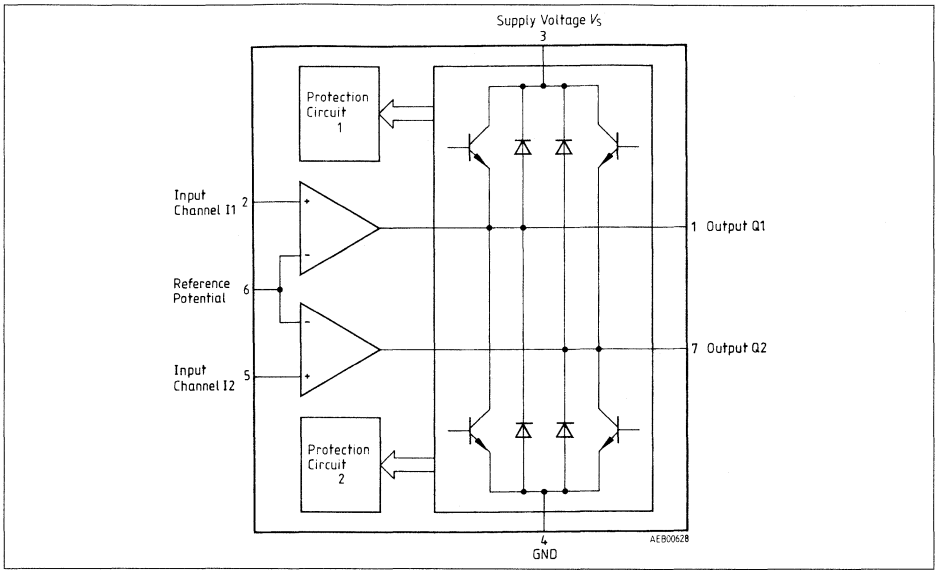

Block Diagram

Absolute Maximum Ratings

T_C = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage	V_S	– 0.3	45	V
Input voltages Pin 2, 5 and 6	V_I	– 0.3	+ V_S	V
Currents				
Supply current $T_C \leq 85$ °C	I_S	– 3	8	A
Output current $T_C \leq 85$ °C	$I_{Q1,2}$	– 4	4	A
Ground current $T_C \leq 85$ °C	I_{GND}	– 8	8	A
Diode peak currents				
to + V_S	I_{F+}	–	1.5	A
to ground	I_{F-}	–	4	A

Absolute Maximum Ratings (cont'd)
T_C = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Temperatures				
Junction temperature	T_j	–	150	°C
Storage temperature range	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	8	24	V
Case temperature $T_j \leq 150$ °C	T_C	– 40	125	°C
Thermal resistance				
system - case	$R_{th\,SC}$	–	4	K/W
system - ambient	$R_{th\,SA}$	–	65	K/W

Characteristics
V_S = 12 V; T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Ratings						
Quiescent current	I_1	–	15	30	mA	$V_{2,5}$ = 12 V; V_6 = 0 V
Control Inputs						
Input offset voltage	V_{I0}	– 10	–	10	mV	–
Input offset current	I_{I0}	– 100	–	100	nA	–
Input current	$-I_{I2,5}$	–	1	2	µA	$V_{2,5}$ = 0 V V_6 = 12 V
Input current	$-I_{I6}$	–	2	4	µA	$V_{2,5}$ = 12 V V_6 = 0 V
Common-mode input voltage ranges						
to + V_S	V_{C+}	–	2.5	3	V	Difference to + V_S
to ground	V_{C-}	–	– 0.5	0	V	to ground

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Characteristics (cont'd)
V_S = 12 V; T_C = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Stages						
Saturation voltages						
to + V_S	V_{QSato}	–	1.0	1.3	V	$V_{I6} < V_{I2,5}$; $I_Q = -1$ A [1]
to + V_S	V_{QSato}	–	2.0	2.5	V	$V_{I6} < V_{I2,5}$; $I_Q = -3$ A [1]
to ground	V_{QSatu}	–	1.0	1.3	V	$V_{I6} < V_{I2,5}$; $I_Q = 1$ A
to ground	V_{QSatu}	–	2.0	2.5	V	$V_{I6} < V_{I2,5}$; $I_Q = 3$ A
Forward voltages						
to + V_S	V_{Fo}	–	1.2	1.4	V	$V_{I6} < V_{I2,5}$; $I_Q = 1$ A [1]
to ground	V_{Fu}	–	– 1	– 1.2	V	$V_{I6} > V_{I2,5}$; $I_Q = -1$ A
to ground	V_{Fu}	–	– 1.4	– 1.6	V	$V_{I6} > V_{I2,5}$; $I_Q = -3$ A
Short-circuit currents						
at short-circuit to + V_S						S 1P, 2P closed
						$V_6 > V_{I2,5}$
	$I_{QP1,7}$	–	2.5	3.5	A	V_S = 12 V
	$I_{QP1,7}$	–	1.0	–	–	V_S = 24 V
at short-circuit						S 1M, 2M closed
to ground						$V_6 > V_{I2,5}$
	$-I_{QM1,7}$	–	2.5	–	A	V_S = 12 V
	$-I_{QM1,7}$	–	1.5	3.5	A	V_S = 24 V
Switching Times						
Turn-ON time	$t_{D\,ON}$	–	2	4	µs	**see figure 2**
Turn-OFF time	$t_{D\,OFF}$	–	3	6	µs	**see figure 2**

[1] measured to + V_S

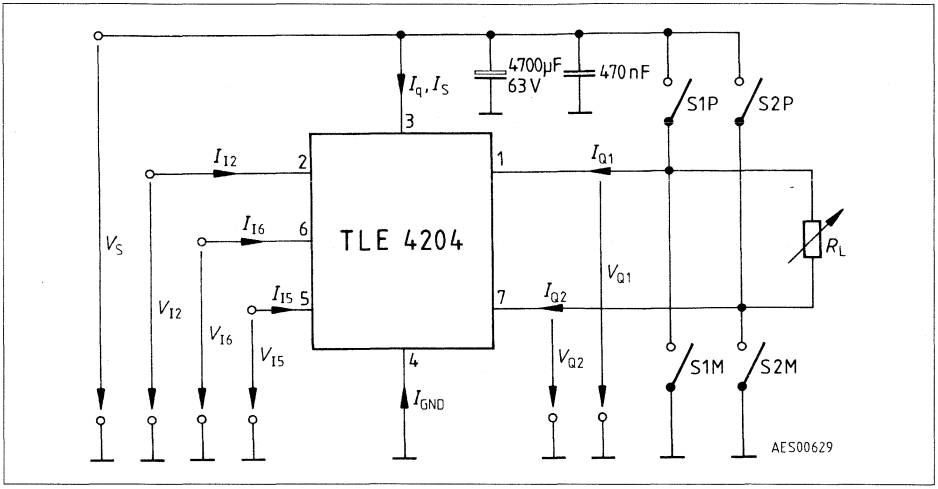


Figure 1
Test Circuit

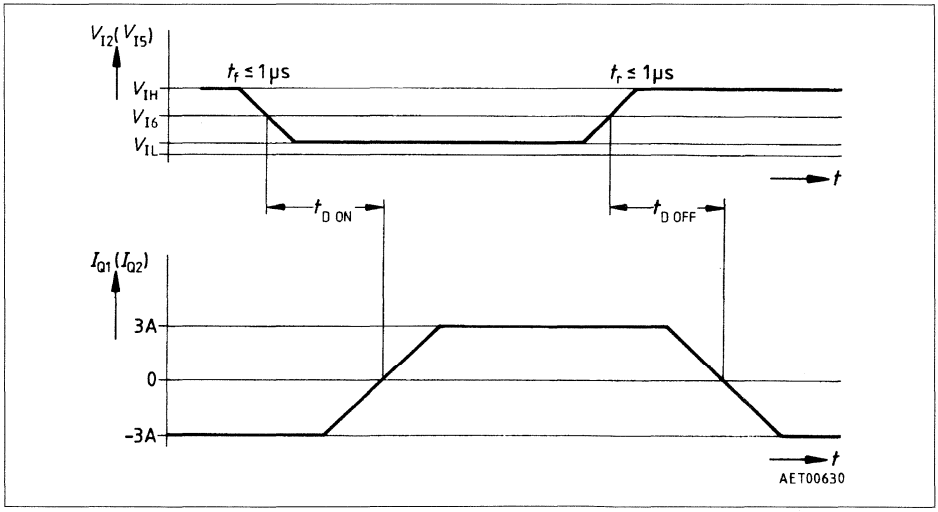


Figure 2
Timing Diagram

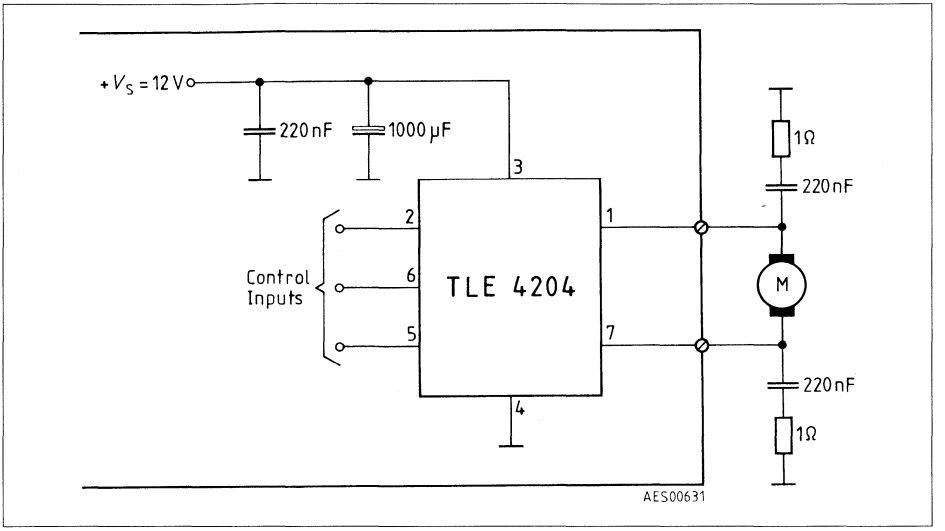
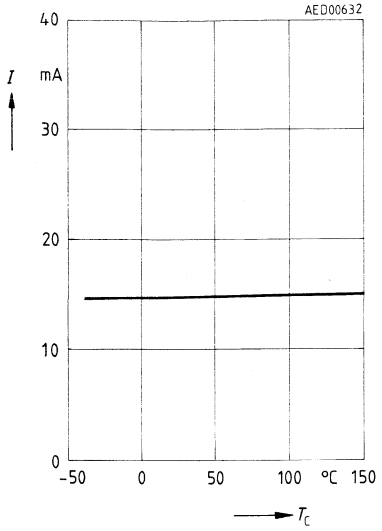


Figure 3
Application Circuit

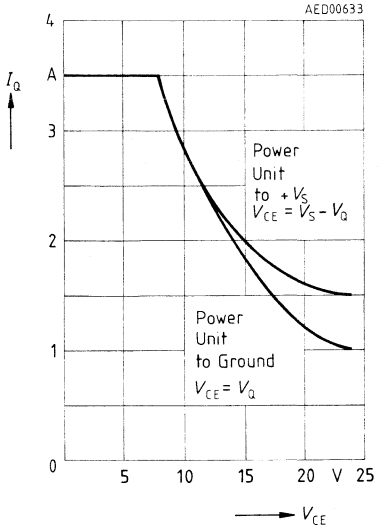
Quiescent Current versus Case Temperature T_C

V_S = 12 V; $V_{I2/5} = V_S$; V_{I6} = 0 V



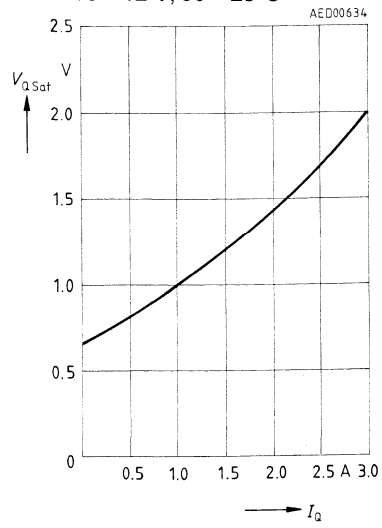
Short-Circuit Current versus Voltage V_{CE} of Power Unit

T_C = 25 °C



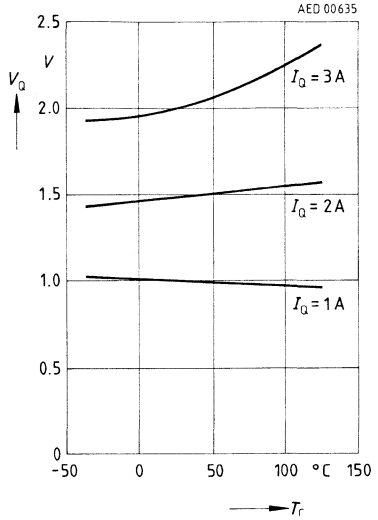
Saturation Voltage V_{QSat} versus Output Current I_Q

V_S = 12 V; T_C = 25 °C



Saturation Voltage versus Case Temperature T_C

V_S = 12 V; $P_D \leq$ 6 W



10

SIEMENS

DC Motor Driver

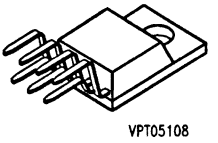
TLE 5203

Preliminary Data

SPT IC

Features

- Output current ± 3 A (peak ± 4 A)
- I/O error diagnostics
- Short-circuit proof
- Four-quadrant operation
- Integrated free-wheeling diodes
- Wide temperature range



P-TO220-7-1

Type	Ordering Code	Package
▼ TLE 5203	Q67000-A9096	P-TO220-7-1

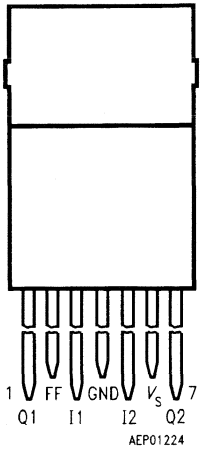
▼ New type

TLE 5203 is an integrated power bridge with DMOS output stages for driving DC motors.

This motor bridge is optimized for driving DC motors in reversible operation. The internal protective circuitry in particular ensures that no crossover currents can occur.

Because the free-wheeling diodes are integrated, the external circuitry that is necessary is restricted to the capacitors on the supply voltage.

The control inputs have TTL/CMOS-compatible levels.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	Q1	**Short-circuit proof output of channel 1;** free-wheeling diodes integrated for inductive loads
2	FF	**Error flag;** TTL/CMOS-compatible output for error detection (open drain)
3	I1	**Control input 1;** TTL/CMOS-compatible
4	GND	**Ground;** connected intenally to cooling lug
5	I2	**Control input 2;** TTL/CMOS-compatible
6	V_S	**Supply voltage;** wire with capacitor matching load
7	Q2	**Short-circuit proof output of channel 2;** free-wheeling diodes integrated for inductive loads

Circuit Description

Input Circuit

The control inputs consist of TTL/CMOS-compatible Schmitt triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages.

Output Stages

The output stages consist of a switched H-bridge. Protective circuits make the outputs short-circuit proof to ground and to the supply voltage throughout the operating range. Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated power diodes.

Monitoring and Protective Functions

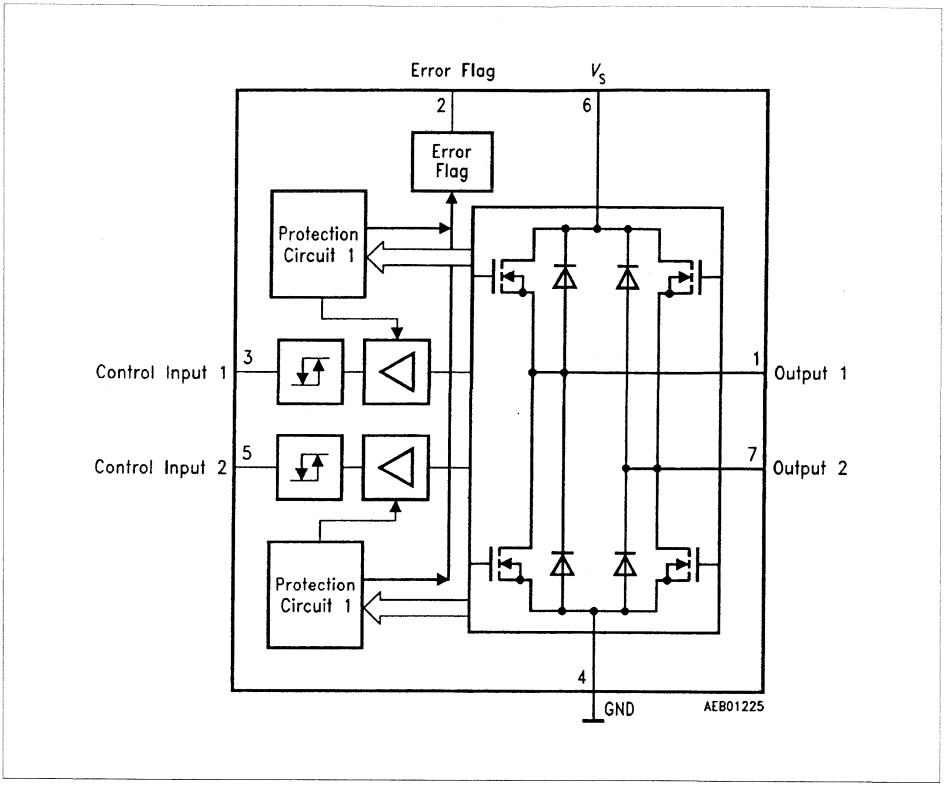
An internal circuit ensures that all output transistors are turned off if the supply voltage is below the operating range.

A monitoring circuit for each output transistor detects whether the particular transistor is active and in this case prevents the corresponding source transistor (sink transistor) from conducting in sink operation (source operation). This effectively guards against crossover currents. Pulse-width operation is possible up to a maximum switching frequency of 1 kHz for any load.

Depending on load higher frequencies are possible.

Various errors like short-circuit to + V_S, ground or across the load are detected. All faults result in turn-OFF of the output stages after a delay of 30 µs and setting of the error flag. Reset is by a change of the input signals so that, despite remanent errors, the outputs are no longer overloaded.

If the thermal shutdown responds at T_j > 160 °C, all four output stages are jointly disabled and the error flag is set without a delay.



Block Diagram

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The faults short-circuit, open circuit and overtemperature produce a fault message (error flag FF active low).

Short-Circuits

S	I1	I2	Q1	Q2	Q1/G	Q1/V_S	Q2/G	Q2/V_S	Load	OC	FF
1	L	L	H	L	X	–	–	X	X	–	L
2	L	H	L	H	–	X	X	–	X	–	L
3	H	L	L	L	–	X	–	X	–	–	L
4	H	H	HX	LX	–	–	–	–	–	X	L
Occurent	L	L/H	H/L	L/H	X/–	–/X	–/X	X/–	X	–	L
Temp	X	X	HX	LX	–	–	–	–	–	–	L

S = state; I = input; Q = output; G = ground; OC = open circuit; FF = fault flag; V_S = supply voltage

Q1, 2 L means: lower power element turned ON;
upper power element turned OFF
Q1, 2 H means: upper power element turned ON;
lower power element turned OFF
Q1 HX means: output stage high-impedance, pull-up to + V_S
Q2 LX means: output stage high-impedance, pull-down to ground
Ocurrent means: overcurrent and behaves like overload
Temp. means: overtemperature

For example: state 1: motor turns to right
state 2: motor turns to left
state 3: motor is braked
state 4: motor is unbraked

State1 of the table means that the motor turns. An error in this state is signaled if either output 1 is shorted to ground, output 2 is shorted to V_S or the load is shorted.

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltage					
Supply voltage	V_S	– 0.3	40	V	–
Supply voltage	V_S	– 1	–	V	t < 500 ms; I_S < 5 A
Logic input voltage	$V_{I1,2}$	– 0.3	7	V	V_S = 0 – 40 V
Diagnostics output voltage	V_{FF}	– 0.3	7	V	–
Current					
Free-wheeling current	I_F	– 4	4	A	$T_j \leq$ 150 °C
Output current	I_Q	– 4	4	A	–
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal Resistance					
Junction-case	$R_{th\,jC}$	–	3	K/W	–
Junction-ambient	$R_{th\,jA}$	–	65	K/W	–
Operating Range					
Supply voltage	V_S	6	24	V	–
Logic input voltage	$V_{I1,2}$	– 0.3	7	V	–
Switching frequency [1]	f	–	1	kHz	–
Junction temperature	T_j	– 40	150	°C	–

1) Depending on load higher frequencies are possible.

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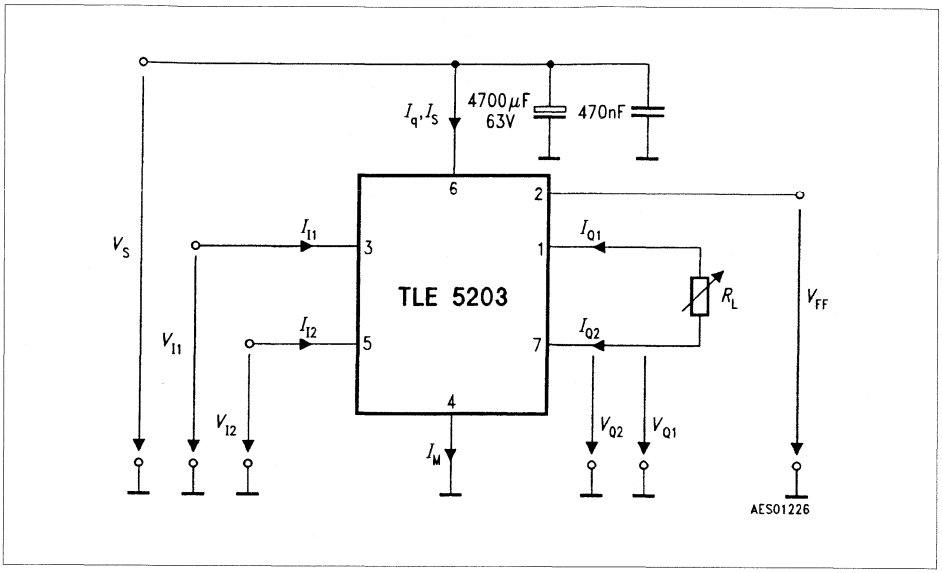
Electrical Characteristics

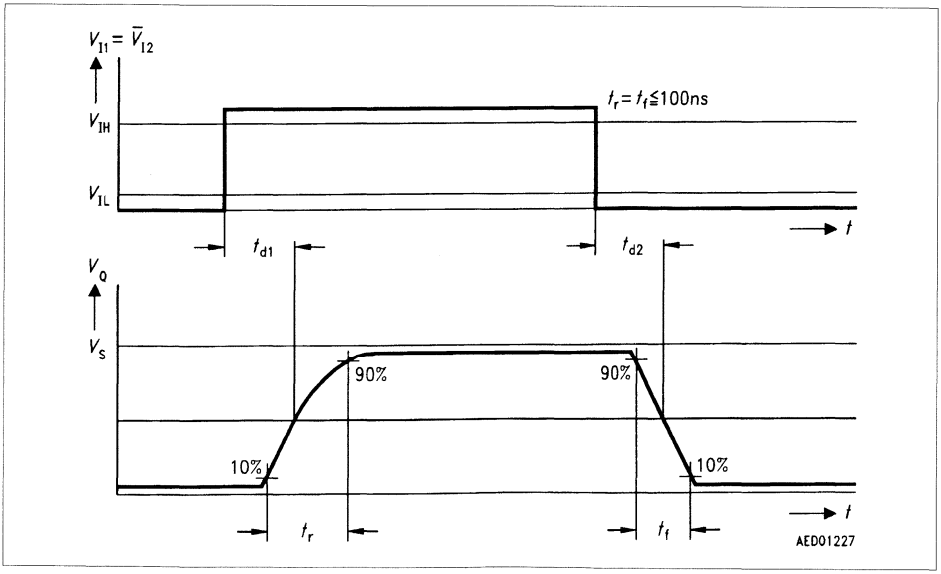
V_S = 9 to 18 V; T_A = – 25 to 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Quiescent current	I_q	–	3	10	mA	I_L = 0 A
Turn-ON delay	t_{d1}	–	–	10	µs	Input to output
Turn-OFF delay	t_{d2}	–	–	10	µs	Input to output
Turn-ON time	t_r	–	–	10	µs	I_Q = 2.5 A; cf diagram
Turn-OFF time	t_f	–	–	10	µs	I_Q = 2.5 A; cf diagram
Logic						
Control inputs						
H-input voltage	V_{IH}	2.8	–		V	–
L-input voltage	V_{IL}	–	–	1.2	V	–
Hysteresis of input voltage	ΔV_I	0.4	0.8	1.2	V	–
H-input current	I_I	– 10		10	µA	V_I = 0 – 5 V
Diagnostics output						
Delay time	t_d	20	30	40	µs	–
L-output voltage	V_{FF}	–	–	0.4	V	I = 3 mA
Leakage current	I_{RD}	–	–	10	µA	–
Error detection						
Switching threshold 1	V_{F1}	2	2.7	3.5	V	Error low
Switching threshold u	V_{Fu}	2	2.7	3.5	V	Error high
Overcurrent 1	I_{F1}	3	4	5	A	Error low
Outputs						
RDSONU	–	–	–	0.5	Ω	V_S > 6 V; T_j = 25 °C [1]
RDSONU	–	–	–	0.8	Ω	V_S > 6 V; T_j = 150 °C [1]
RDSONL	–	–	–	0.4	Ω	V_S > 6 V; T_j = 25 °C [1]
RDSONL	–	–	–	0.8	Ω	V_S > 6 V; T_j = 150 °C [1]
Diode forward voltage	V_F	–	–	1.5	V	I_F = 3 A
Pullup/pulldown	R	5	–10	25	kΩ	–

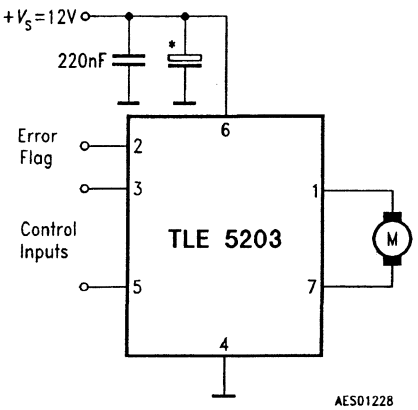
1) Values for RDSON are for t > 100 µs after applying + V_S.



Test Circuit



Timing Diagram

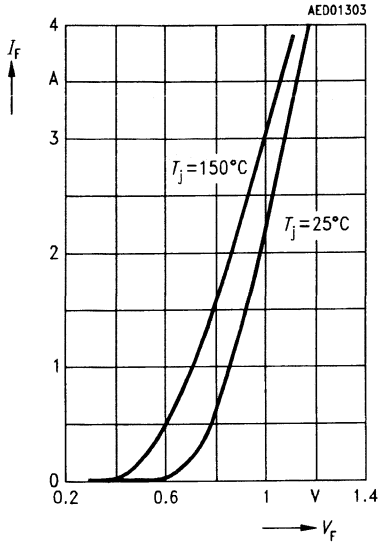


Application Circuit

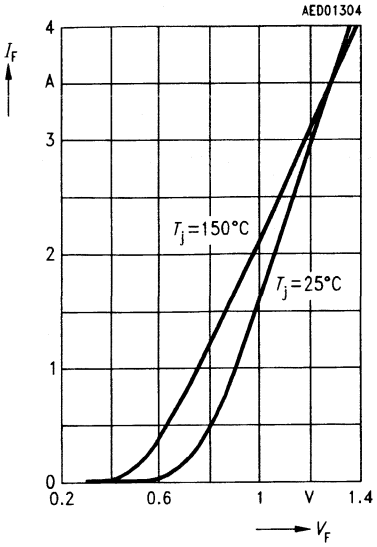
*) Necessary for isolating supply voltage or interruption (eg 470 µF).

Diagrams

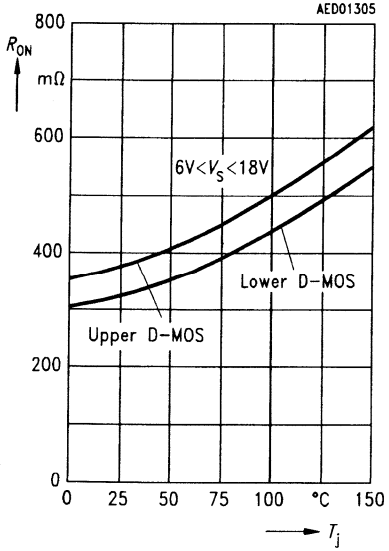
R_{ON} Resistance of Output Stage over Temperature



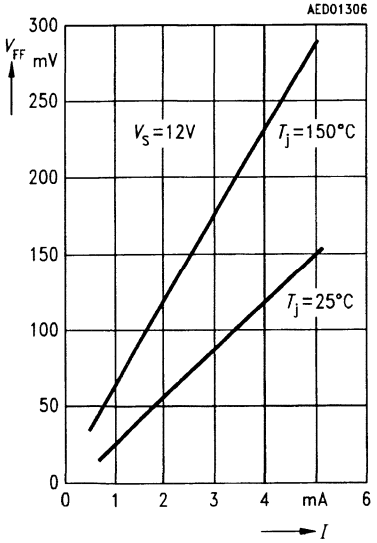
Output Voltage on Diagnostics Output versus Current



Forward Voltage of Upper Free-Wheeling Diode versus Current



Forward Voltage of Lower Free-Wheeling Diode versus Current



10

SIEMENS

4-A Motor Driver

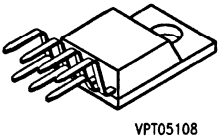
TLE 4203

Preliminary Data

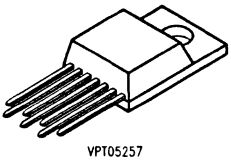
Bipolar IC

Features

- Integrated free-wheeling diodes
- Outputs short-circuit proof to V_S and ground
- Thermal overload protection
- Blocking of the output stages upon undervoltage
- Final push-pull stage free of cross-over



P-TO220-7-1



P-TO220-7-2

Type	Ordering Code	Package
S TLE 4203	Q67000-A8121	P-TO220-7-1
▼ TLE 4203 S	Q67000-A9101	P-TO220-7-2

▼ New type

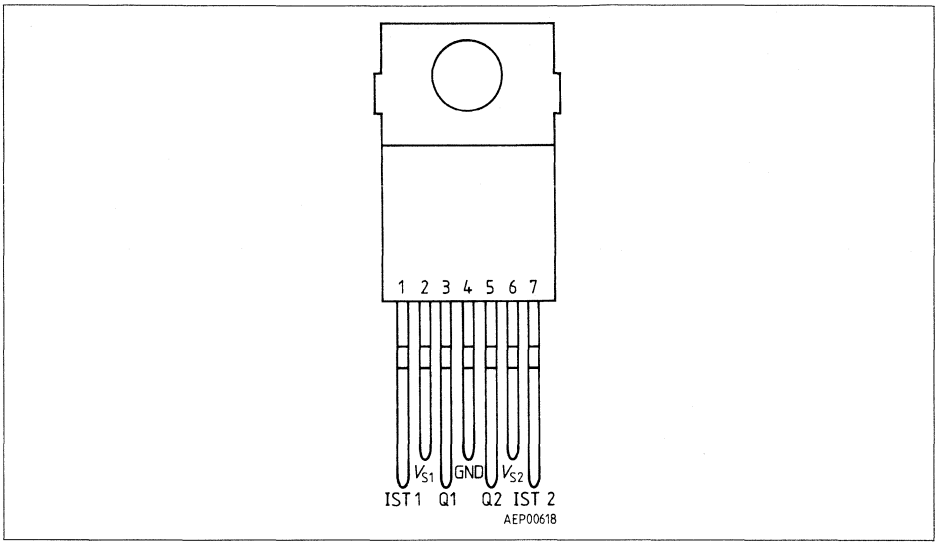
The integrated circuit TLE 4203 is a versatile double power driver of up to 4 A output current which is particularly suitable as a driver for DC motors in reversible operation.

The push-pull power output stages operate in the switching mode and can be combined to a full-bridge configuration.

The drive of the input stage is implemented using digital logic.

The device contains a temperature protection logic, output stages protected against short-circuit and integrated free-wheeling diodes.

Typical applications are for follow-up control, servo drives, servo motors, drive mechanisms, etc.

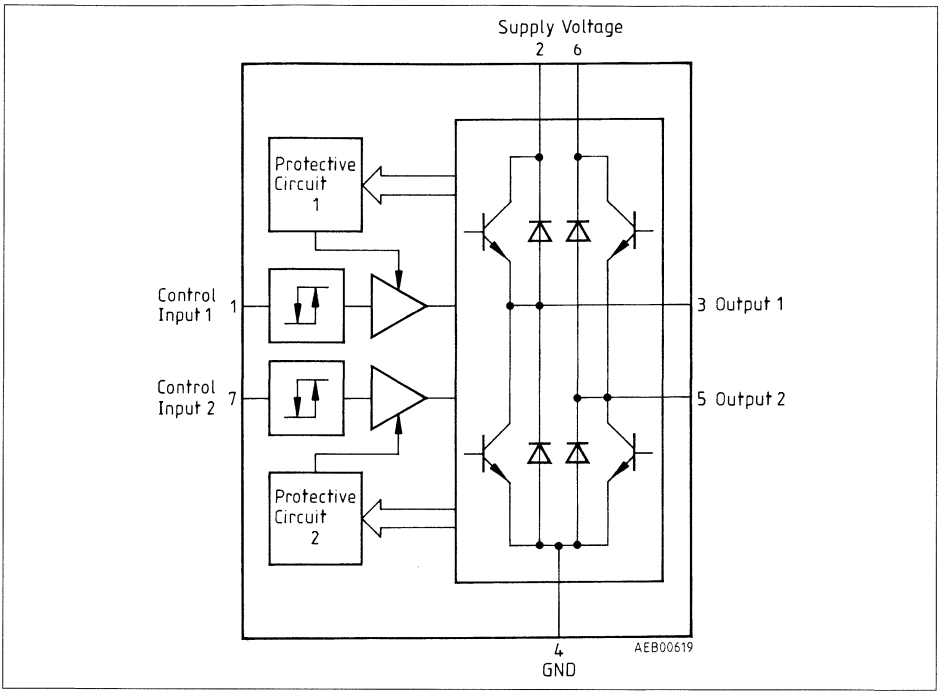


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	IST1	**Control input for channel 1** (TTL/CMOS-compatible), of non-inverting effect on the channel output.
2	V_{S1}	**Channel 1 supply voltage;** externally connected with the supply voltage pin for channel 2 (pin 6).
3	Q1	**Short-circuit protected push-pull C output** channel 1 for currents up to 6 A. Free-wheeling diodes are integrated on chip for inductive loads.
4	GND 1, 2	**Ground;** track should be designed for the max. short-circuit current (2 × 6 A).
5	Q2	**Short-circuit protected push-pull C output** channel 2 for curents up to 6 A. Free-wheeling diodes are integrated on chip for inductive loads.
6	V_{S2}	**Channel 2 supply voltage;** externally connected with the supply voltage pin for channel 1 (pin 2).
7	IST2	**Control input for channel 2** (TTL/CMOS-compatible), of non-inverting effect on the channel output.

10



Block Diagram

Application

In industrial and automotive electronics, power full-bridge DC motor drivers are mostly used for bidirectional motor drives. The two TTL and CMOS-compatible control inputs act on the output as follows:

Status	Input 1	Input 2	Output 1	Output 2
1	L	L	V_{QL}	V_{QL}
2	L	H	V_{QL}	V_{QH}
3	H	L	V_{QH}	V_{QL}
4	H	H	V_{QH}	V_{QH}

V_{QL} means: Lower power unit conducting; upper power unit blocked.
V_{QH} means: Upper power unit conducting; lower power unit blocked.

The following examples illustrate the operation:

Status 1: Motor is slowed down
Status 2: Motor turns right
Status 3: Motor turns left
Status 4: Motor is slowed down

Circuit Description

Input Circuit

The control inputs consist of TTL and CMOS-compatible Schmitt triggers with hysteresis. Buffer amplifiers, controlled from these stages, convert the logic signal into the form required for driving the power output stages.

Output Stages

The output stages consist of two push-pull C stages. Using protective circuits for limiting the power dissipation makes the outputs short-circuit proof to ground and to supply voltage throughout the entire operating range. Positive and negative voltage peaks, which occur when switching inductive loads, are limited by integrated power diodes.

Monitoring and Protecting Functions

The IC is protected against thermal overloads by a temperature protecting circuit.

In addition an internal circuit ensures that all output transistors are blocked for supply voltages below the operating range.

A monitoring stage logic for each output stage transistor detects whether the relevant transistor is active and in this case for sink operation (source operation) prevents the corresponding source transistor (sink transistor) from being turned on. Direct cross-over currents are effectively prevented with this method.

Absolute Maximum Ratings

$T_C = -40$ to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage	V_S	– 0.3	45	V
Logic input voltages	$V_{I1,2}$	– 45	45	V
Currents				
Supply current $T_C \leq 85$ °C	I_S	– 12	12	A
Output current $T_C \leq 85$ °C	$I_{Q1,2}$	– 6	6	A
Ground current $T_C \leq 85$ °C	I_{GND}	– 12	12	A

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Absolute Maximum Ratings (cont'd)
T_C = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Temperatures				
Junction temperature	T_j	–	150	°C
Storage temperature range	T_{stg}	– 50	150	°C
Thermal resistances				
system - case	$R_{th\,SC}$	–	3	K/W
system - ambient	$R_{th\,SA}$	–	65	K/W
Operating Range				
Supply voltage	V_S	5.0	20	V
Logic input voltage	$V_{I1,2}$	– 10	40	V
Case temperature $T_j \leq 150$ °C	T_C	– 40	125	°C

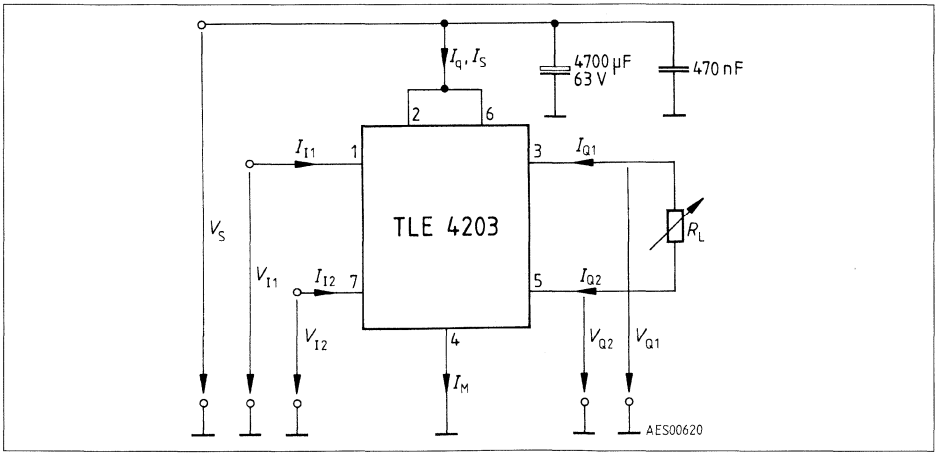
Characteristics
V_S = 8 to 18 V, T_j = – 25 to 125 °C (typ. V_S = 12 V; T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current	I_q	–	70	100	mA	$V_{I1} = V_{I2} > V_{IH}$
Quiescent current	I_q	–	180	230	mA	$V_{I1} = V_{I2} < V_{IL}$
Logic						
Control inputs						
H-input voltage	V_{IH}	2.8	–	–	V	–
L-input voltage	V_{IL}	–	–	1.2	V	–
Hysteresis of input voltage	ΔV_I	–	0.7	–	V	–
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	–	–	10	µA	V_I = 0.5 V

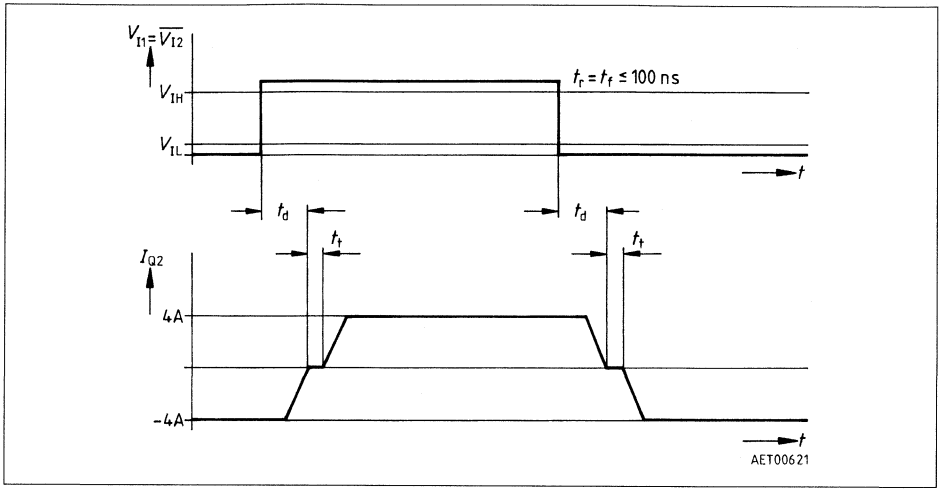
Characteristics (cont'd)
V_S = 8 to 18 V, T_C = – 25 to 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Stages						
Saturation voltages						
to + V_S	V_{QSato}	–	1.1	1.3	V	$V_{I1,2} > V_{IH}$; $I_Q = -1$ A [1]
to + V_S	V_{QSato}	–	1.5	1.8	V	$V_{I1,2} > V_{IH}$; $I_Q = -2$ A [1]
to + V_S	V_{QSato}	–	2.5	3.5	V	$V_{I1,2} > V_{IH}$; $I_Q = -4$ A [1]
to ground	V_{QSatu}	–	0.3	0.6	V	$V_{I1,2} < V_{IL}$; $I_Q = 1$ A
to ground	V_{QSatu}	–	0.6	1.0	V	$V_{I1,2} < V_{IL}$; $I_Q = 2$ A
to ground	V_{QSatu}	–	1.6	3.2	V	$V_{I1,2} < V_{IL}$; $I_Q = 4$ A
Forward Voltages						
Diode to + V_S	$-V_{QFo}$	–	0.95	1.3	V	$V_{I1/2} > V_{IH}$; $I_Q = 1$ A [1]
Diode to + V_S	$-V_{QFo}$	–	1.05	1.5	V	$V_{I1/2} > V_{IH}$; $I_Q = 2$ A [1]
Diode of + V_S	$-V_{QFo}$	–	1.30	1.8	V	$V_{I1/2} > V_{IH}$; $I_Q = 4$ A [1]
Diode to ground	$-V_{QFu}$	–	0.95	1.3	V	$V_{I1/2} < V_{IL}$; $I_Q = -1$ A
Diode to ground	$-V_{QFu}$	–	1.00	1.5	V	$V_{I1/2} < V_{IL}$; $I_Q = -2$ A
Diode to ground	$-V_{QFu}$	–	1.20	1.8	V	$V_{I1/2} < V_{IL}$; $I_Q = -4$ A

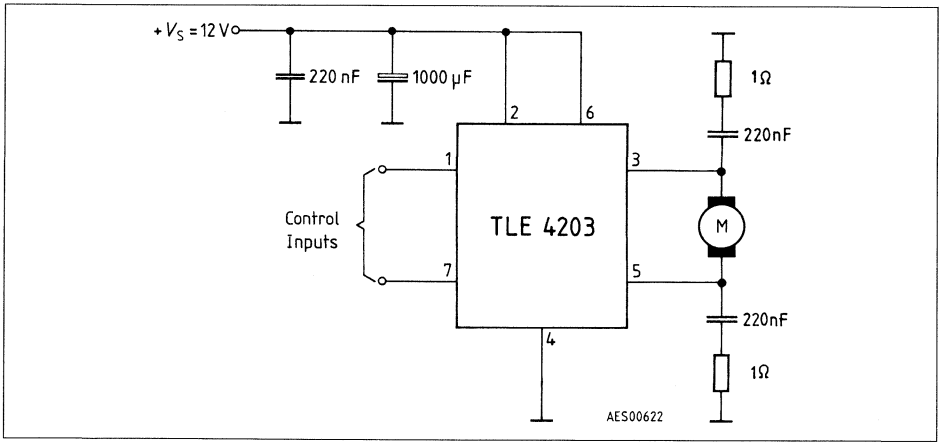
[1] measured to + V_S



Test Circuit

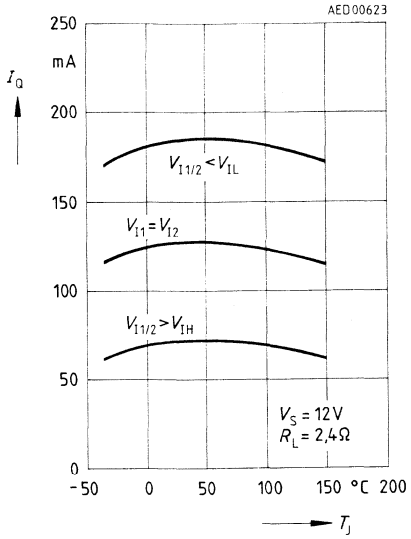


Timing Diagram



Application Circuit

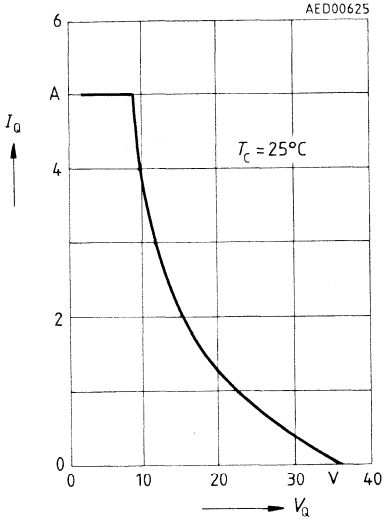
Saturation Voltage versus Output Current



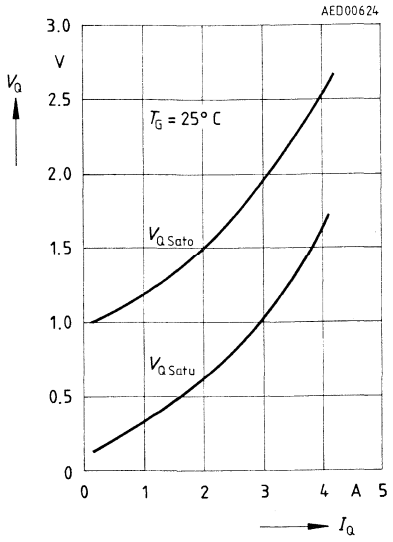
Short-Circuit Current versus Output Voltage

$V_A = V_Q$ for sink operation

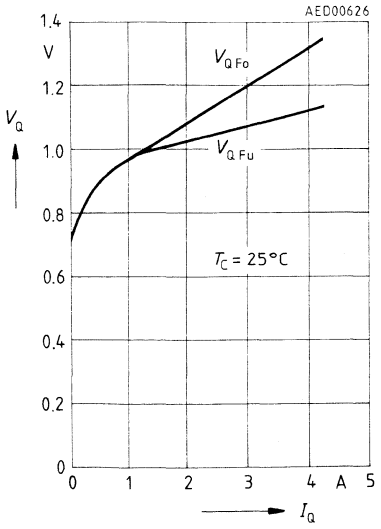
$V_A = V_S - V_Q$ for source operation



Saturation Voltage versus Output Current



Diode Forward Voltage versus Output Current



10

SIEMENS

2-Phase Stepper-Motor Driver

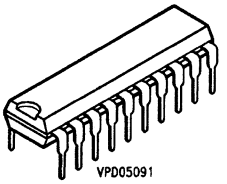
TCA 3727

Preliminary Data

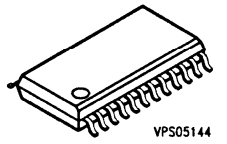
Bipolar IC

Features

- 2 x 0.75 amp. / 50 V outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 52 V
- Outputs free of crossover current
- Offset-phase turn-ON of output stages
- Z-diode for logic supply
- Low standby-current drain
- Full, half, quarter, mini, quasi-sine step



P-DIP-20-1



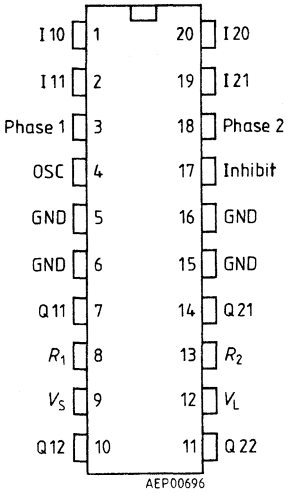
P-DSO-24-1

Type	Ordering Code	Package
TCA 3727	Q67000-A8302	P-DIP-20-1
TCA 3727 G	Q67000-A8335	P-DSO-24-1 (SMD)

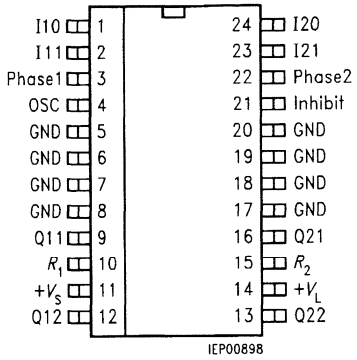
TCA 3727 is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 0.75 A per phase at operating voltages up to 50 V.

The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration have integrated, fast free-wheeling diodes and are free of crossover current. The logic is supplied either separately with 5 V or taken from the motor supply voltage by way of a series resistor and an integrated Z-diode. The device can be driven directly by a microprocessor with the possibility of all modes from full step through half step to mini step or quasi-sine.

TCA 3727



TCA 3727 G



Pin Configuration
(top view)

10

Pin Definitions and Functions

Pin	Function
1, 2, 19, 20 (1, 2, 23, 24) [1]	**Digital control inputs IX0, IX1** for the magnitude of the **current** of the particular phase.

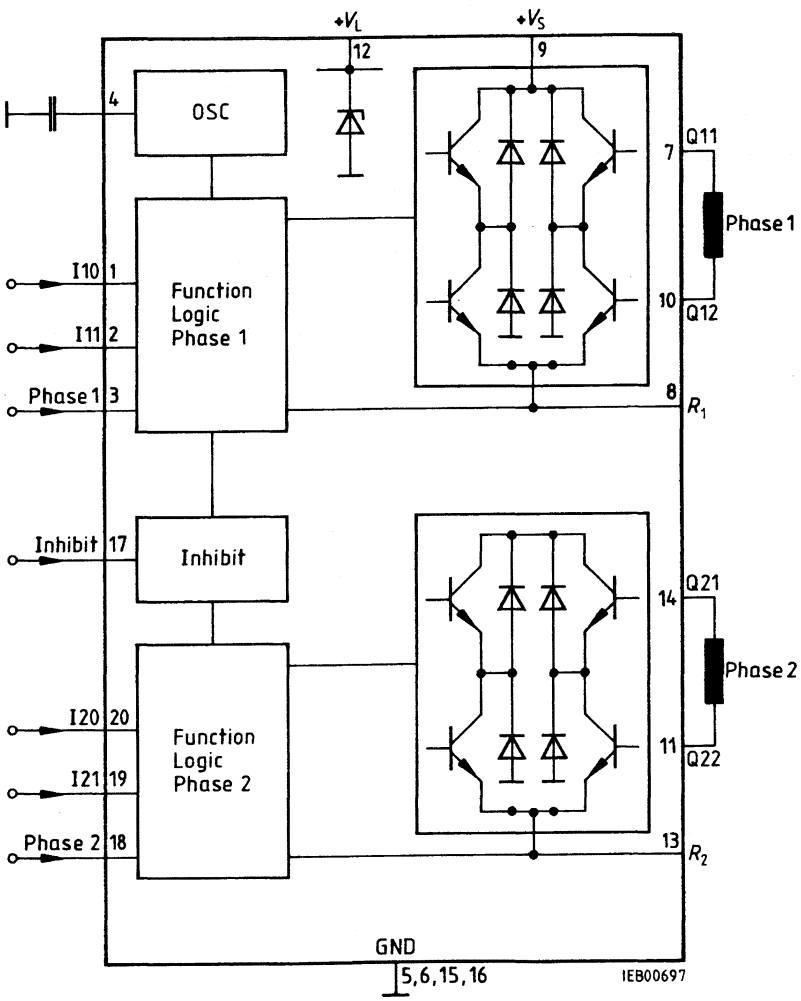
IX1	IX0	Phase current	Example of motor status
H	H	0	No current
H	L	1/3 I_{max}	Hold
L	H	2/3 I_{max}	Normal mode
L	L	I_{max}	Accelerate

$$I_{max1} = \frac{0.75\ V}{R_1}$$

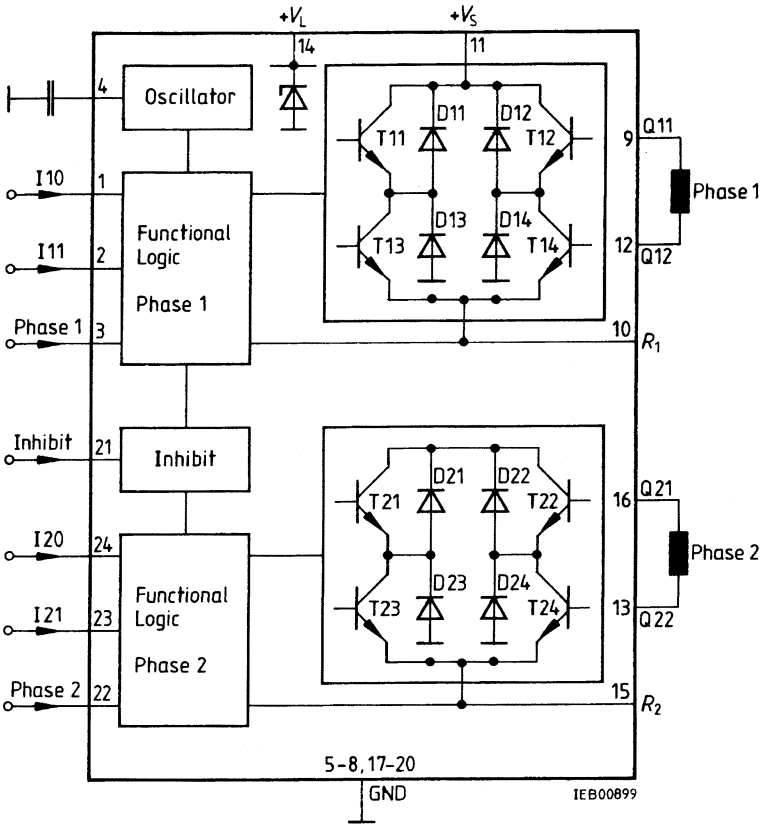
$$I_{max2} = \frac{0.75\ V}{R_2}$$

3	**Input Phase 1**; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.
5, 6, 15, 16 (5, 6, 7, 8, 17, 18, 19, 20) [1]	**Ground**; all pins are connected internally.
4	**Oscillator**; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.
8 (10) [1]	**Resistor** R_1 for sensing the current in phase 1.
7, 10 (9, 12) [1]	**Push-pull outputs Q11, Q12** for phase 1 with integrated free-wheeling diodes.
9 (11) [1]	**Supply voltage**; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 10 µF in parallel with a ceramic capacitor of 220 nF.
12 (14) [1]	**Logic supply voltage**; either supply with 5 V or connect to + V_S across a series resistor. A Z-diode of approx. 7 V is integrated. In both cases block to ground directly on the IC with a stable electrolytic capacitor of 10 µF in parallel with a ceramic capacitor of 100 nF.
11, 14 (13, 16) [1]	**Push-pull outputs Q22, Q21** for phase 2 with integrated free wheeling diodes.
13 (15) [1]	**Resistor** R_2 for sensing the current in phase 2.
17 (21) [1]	**Inhibit input**; the IC can be put on standby by low potential on this pin. This reduces the current consumption substantially.
18 (22) [1]	**Input phase 2**; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.

1) TCA 3727 G only



Block Diagram
TCA 3727



Block Diagram
TCA 3727 G

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	0	52	V	–
Logic supply voltage	V_L	0	6.5	V	Z-diode
Z-current of V_L	I_L	–	50	mA	–
Output current	I_Q	–	1	A	–
Ground current	I_{GND}	–	2	A	–
Logic inputs	V_{Ixx}	– 6	V_L + 0.3	V	I_{XX}; Phase 1, 2; Inhibit
R_1, R_2 input voltage	V_{RX}	– 0.3	V_L + 0.3	V	–
Diode currents					
to + V_S	I_{F+}	–	1	A	–
to ground	I_{F-}	–	1	A	–
Junction temperature	T_j	–	125	°C	–
	T_j	–	150	°C	max. 10,000 h
Storage temperature	T_{stg}	–	125	°C	–

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Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	5	50	V	–
Logic supply voltage	V_L	4.5	6.5	V	without series resistor
Case temperature	T_C	– 40	125	°C	measured on pin 5 P_{diss} = 2 W
Output current	I_Q	–	750	mA	–
Logic inputs	V_{IXX}	– 5	V_L	V	I_{XX}; Phase 1, 2; Inhibit
Thermal resistances					
system-air	$R_{th\ SA}$	–	56	K/W	P-DIP-20-1
system-air (soldered on a 35 µm thick 20 cm² PC board copper area)	$R_{th\ SA}$	–	40	K/W	P-DIP-20-1
system-case	$R_{th\ SC}$	–	10	K/W	measured on pin 5 P-DIP-20-1
system-air	$R_{th\ SA}$	–	75	K/W	P-DSO-24-1
system-air (soldered on a 35 µm thick 20 cm² PC board copper area)	$R_{th\ SA}$	–	50	K/W	P-DSO-24-1
system-case	$R_{th\ SC}$	–	6	K/W	measured on pin 5 P-DSO-24-1

Characteristics

V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
from + V_S	I_S	–	0.2	–	mA	V_{inh} = low
from + V_S	I_S	–	5	–	mA	V_{inh} = high $I_{Q1/2}$ = 0
from + V_L	I_L	–	1.7	–	mA	V_{inh} = low
from + V_L	I_L	–	20	–	mA	V_{inh} = high
Oscillator						
Output charging current	I_{OSC}	–	110	–	µA	
Charging threshold	V_{OSCL}	–	1.4	–	V	T_C = 40 °C
Discharging threshold	V_{OSCH}	–	2.4	–	V	T_C = 40 °C
Frequency	f_{OSC}	–	25	–	kHz	C_{OSC} = 2.2 nF
Phase Current Selection (R_{sense} = 1 Ω)						
No current	I_Q	–	0	–	mA	IX0 = H; IX1 = H
Hold	I_Q	–	250	–	mA	IX0 = L; IX1 = H
Setpoint	I_Q	–	500	–	mA	IX0 = H; IX1 = L
Accelerate	I_Q	–	750	–	mA	IX0 = L; IX1 = L
Logic Inputs (I_{X1} ; I_{X0} ; phase x; inhibit)						
Threshold (I_{XX}, Phase X)	V_I	1.4 (H→L)	–	2.3 (L→H)	V	–
L-input current (logic inputs)	I_{ILInh}	– 10	–	–	µA	V_I = 1.4 V
L-input current (i_{X1}, i_{X0}, phase)	I_{IL}	– 100	–	–	µA	V_I = 0 V
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
Standby Cutout (inhibit)						
Threshold	V_{Inh} (L→H)	2.0	3.0	4.0	V	V_L = 5 V
Threshold	V_{Inh} (H→L)	1.7	2.3	2.9	V	V_L = 5 V
Hysteresis	V_{Inhhy}	0.3	0.7	1.1	V	V_L = 5 V
Internal Z-Diode						
Z-voltage	V_{LZ}	–	7.4	–	V	I_L = 50 mA

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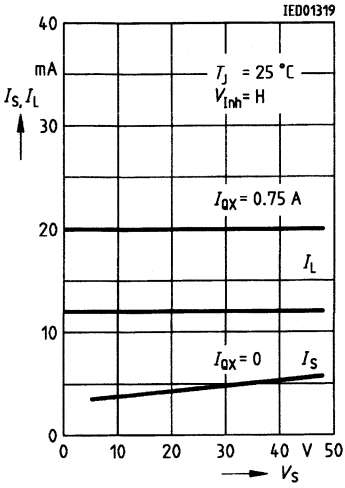
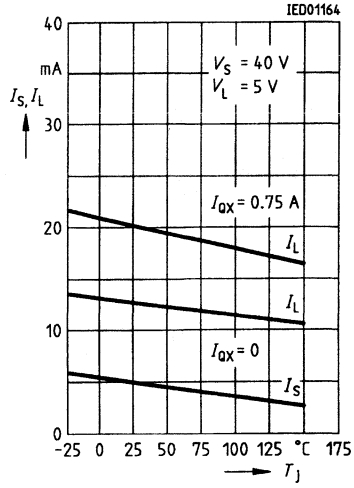
Characteristics (cont'd)
V_S = 40 V; V_L = 5 V; – 25 °C ≤ T_j ≤ 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satL}	–	0.4	–	V	I_Q = – 0.5 A
Saturation voltage	V_{satL}	–	0.7	–	V	I_Q = – 0.75 A
Reverse current	I_{R1}	–	300	–	µA	V_Q = 40 V
Forward voltage	V_{F1}	–	0.9	–	V	I_Q = 0.5 A
Forward voltage	V_{F1}	–	1.0	–	V	I_Q = 0.75 A
Diode Transistor Source Pair (D11, T11; D12, T12; D21, T21; D22, T22)						
Saturation voltage	V_{satuC}	–	1.0	–	V	I_Q = 0.5 A; charge
Saturation voltage	V_{satuD}	–	0.4	–	V	I_Q = 0.5 A; discharge
Saturation voltage	V_{satuC}	–	1.2	–	V	I_Q = 0.75 A; charge
Saturation voltage	V_{satuD}	–	0.8	–	V	I_Q = 0.75 A; discharge
Reverse current	I_{Ru}	–	300	–	µA	V_Q = 0 V
Forward voltage	V_{Fu}	–	1.0	–	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	–	1.1	–	V	I_Q = – 0.75 A
Diode leakage current	I_{SL}	–	1	–	mA	I_F = – 0.75 A

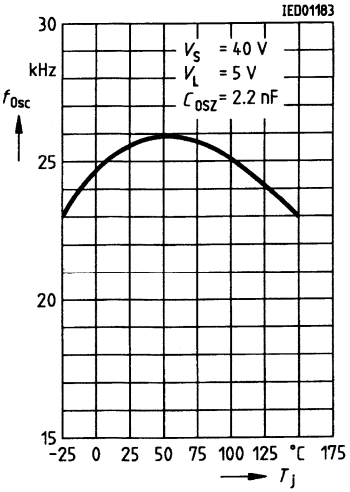
Quiescent Current I_S, I_L versus Supply Voltage V_S V_L = 5 V



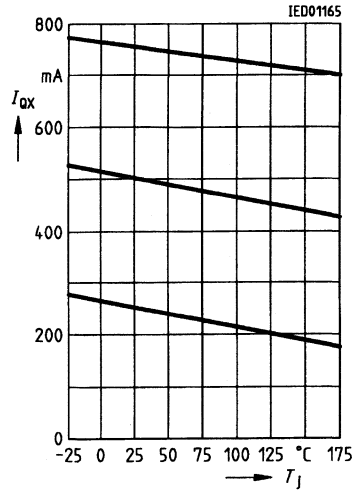
Quiescent Current I_S, I_L versus Junction Temperature T_j



Oscillator Frequency f_{Osc} versus Junction Temperature T_j



Output Current I_{QX} versus Junction Temperature T_j



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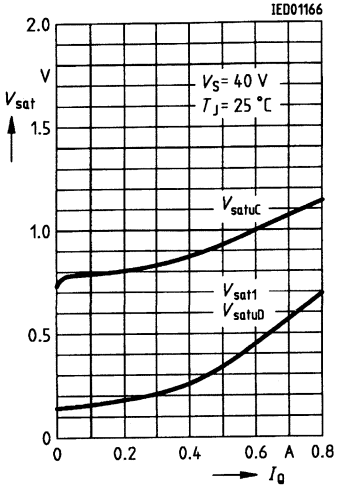
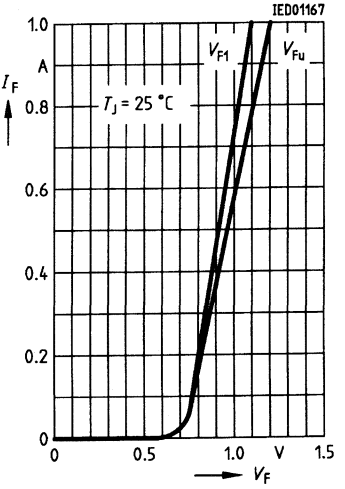
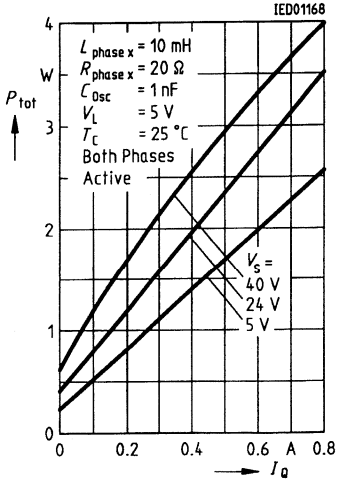
Output Saturation Voltages V_{sat} versus Output Current I_Q



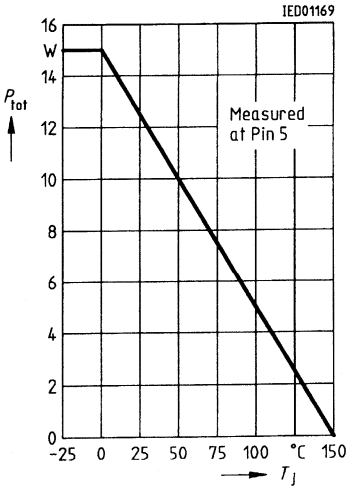
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



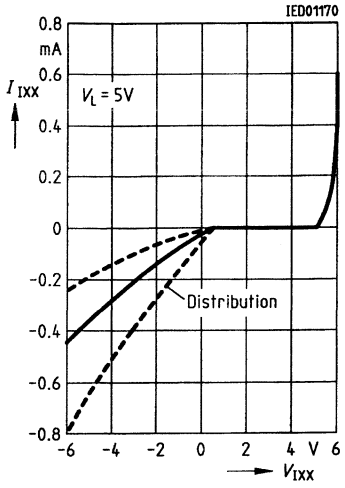
Typical Power Dissipation P_{tot} versus Output Current I_Q (Non Stepping)



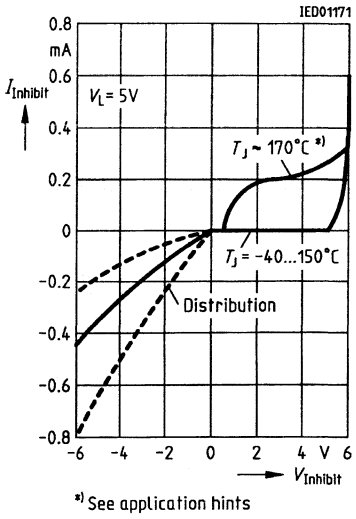
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



Input Characteristics of I_{xx}, Phase X

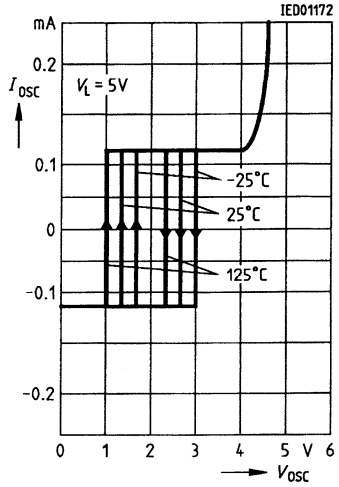


Input Characteristics of Inhibit



*) See application hints

Input Characteristics of OSC



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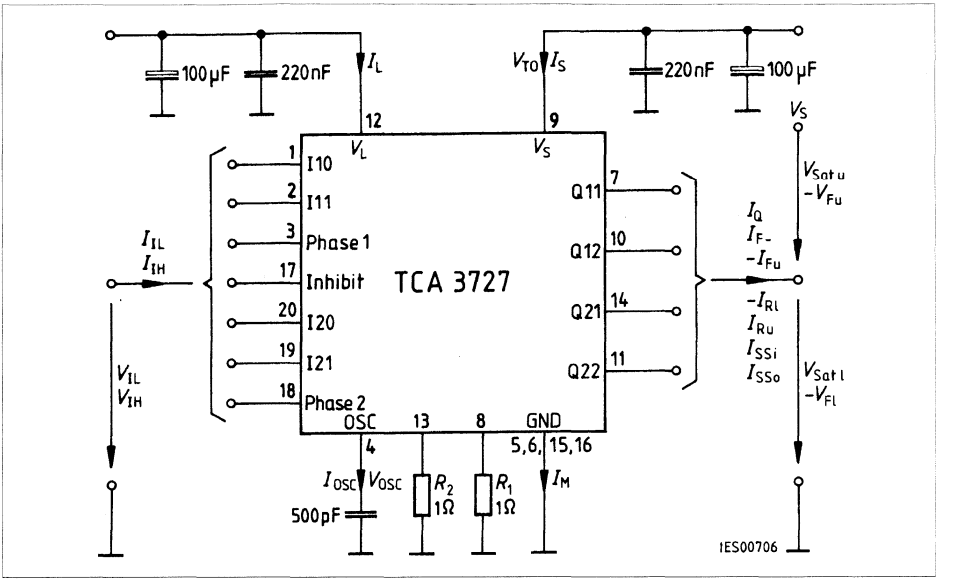
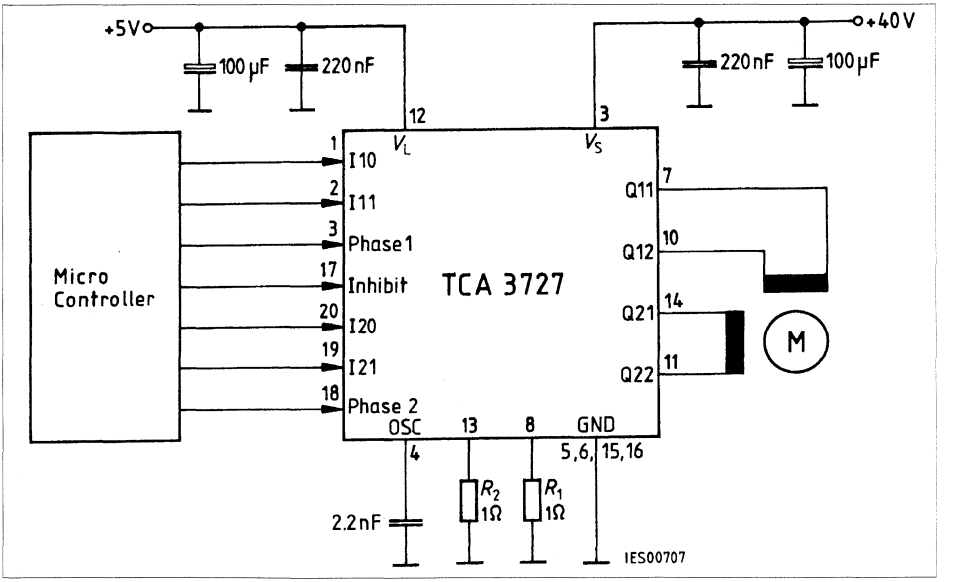
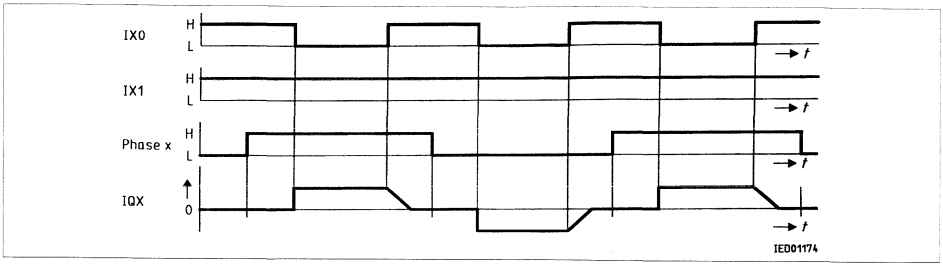


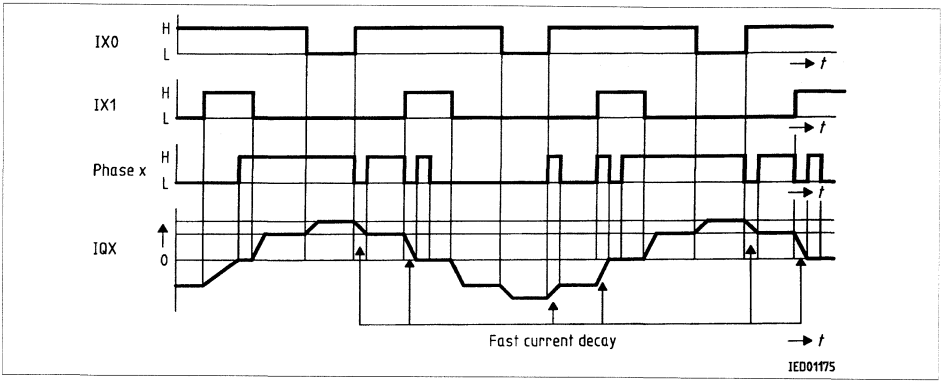
Test Circuit



Application Circuit



Half-Step Operation



Quarter-Step Operation with Phase Reversal for Fast Current Decay

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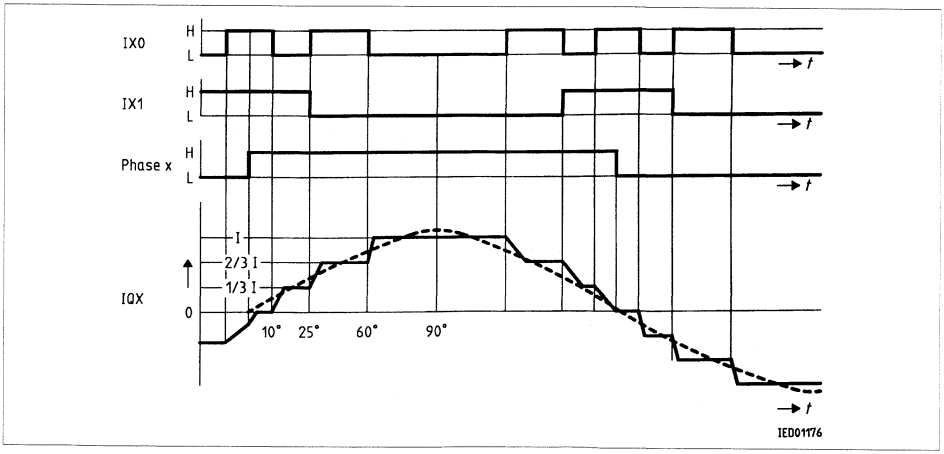
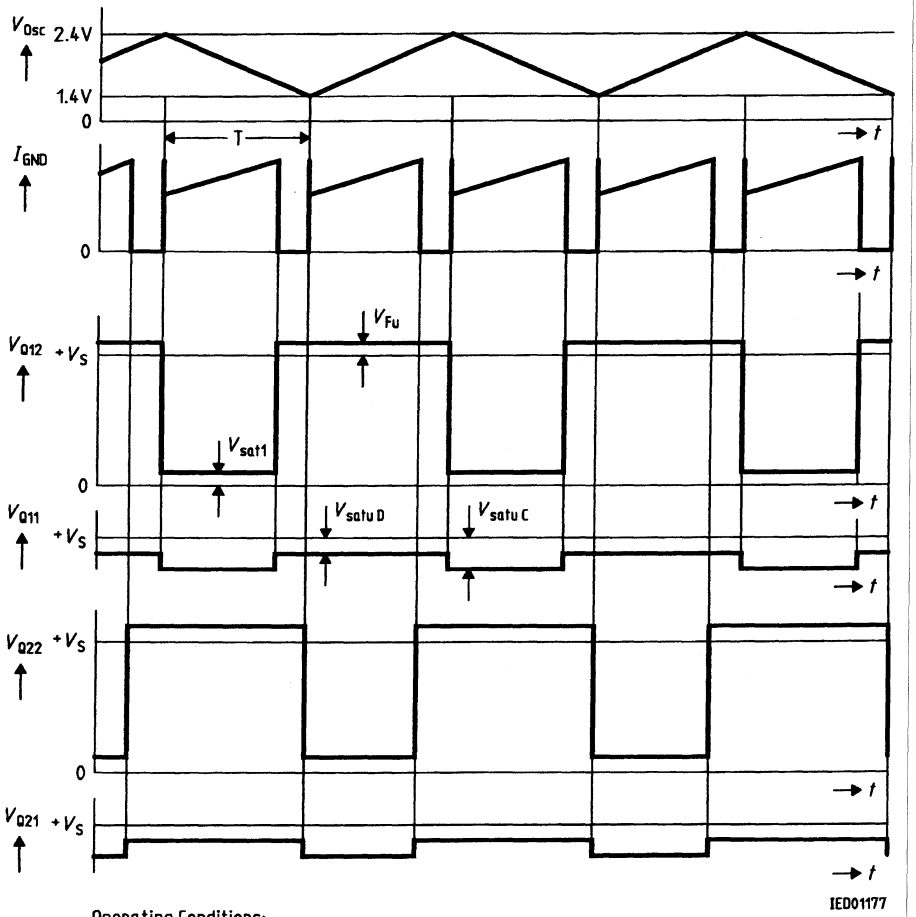


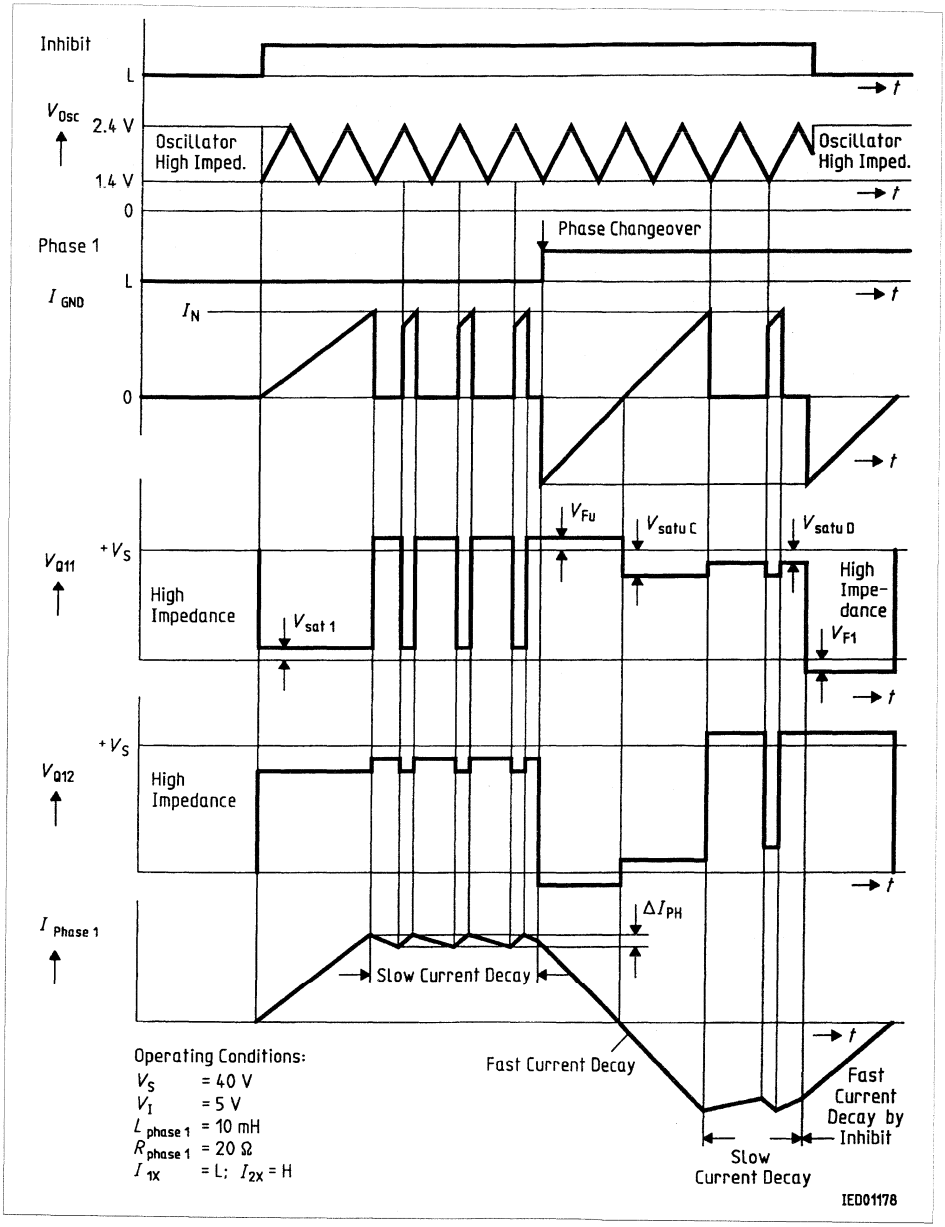
Quasi-Sine Operation without Phase Reversal



Operating Conditions:

V_S	= 40 V
V_L	= 5 V
$L_{phase\,x}$	= 10 mH
$R_{phase\,x}$	= 20 Ω
$V_{phase\,x}$	= H
$V_{Inhibit}$	= H
V_{xx}	= L

Current Control



Phase Reversal and Inhibit

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Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages),
quiescent losses P_q	(quiescent current times supply voltage) and
switching losses P_s	(turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

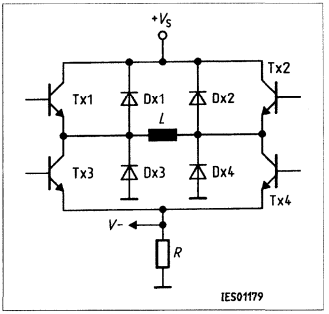
$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

where

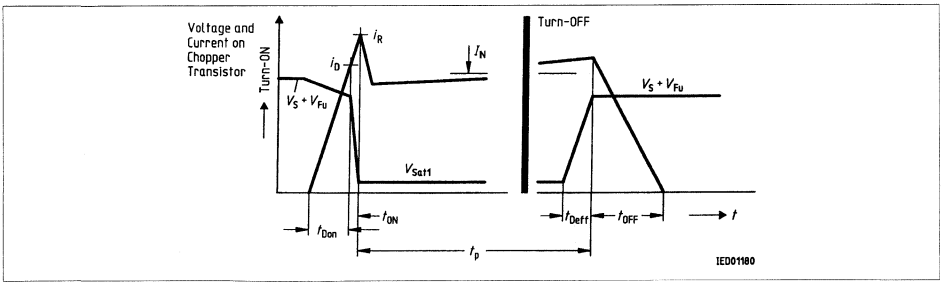
$$P_{sat} \cong I_N \{ V_{sat1} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_S + I_L \times V_L$$

$$P_S \cong \frac{V_S}{T} \{ \frac{i_D \times t_{DON}}{2} + \frac{i_D + i_R \times t_{ON}}{4} + \frac{I_N}{2} t_{DOFF} + t_{OFF} \}$$



I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFFdelay
T = cycle duration
d = duty cycle t_p/T
V_{sat1} = saturation voltage of sink transistor (T3, T4)
V_{satuC} = saturation voltage of source transistor (T1, T2) during charge cycle
V_{satuD} = saturation voltage of source transistor (T1, T2) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (D1, D2)
V_S = supply voltage
V_L = logic supply voltage
I_L = current from logic supply



Application Hints

The TCA 3727 is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TCA 3727 will work with supply voltages ranging from 5 V to 50 V at pin V_s. As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.22 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_1 and R_2. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.25 V, 0.5 V and 0.75 V); (R_1, R_2 = 1 Ω). These thresholds are neither affected by variations of V_L nor by variations of V_S.

Due to chopper control fast current rises (up to 10A/µs) will occure at the sensing resistors R_1 and R_2. To prevent malfunction of the current sensing mechanism R_1 and R_2 should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desireable to reduce acoustic interference. This can be done by forcing the oscillator of the TCA 3727 by a pulse generator overdriving the oscillator loading currents (approximately ± 100 µA). In these applications low level should be between 0 V and 1 V while high level should be between 2.6 V and V_L.

10

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TCA 3727 uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented. To provide a warning in critical applications, the current of the sensing element is wired to input Inhibit. Before thermal shut down occures Inhibit will start to pull down by some hundred microamperes. This current can be sensed to build a temperature prealarm.

SIEMENS

2-Phase Stepper Motor Driver

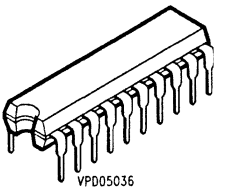
TLE 4727

Preliminary Data

Bipolar IC

Features

- 2 x 1 amp. outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 45 V
- Overvoltage cut-out
- Outputs free of crossover current
- Offset-phase turn-ON of output stages
- 5 V output for logic supply
- All outputs short-circuit proof
- Integrated 5 V voltage regulator
- Error-flag for overload, open load, overtemperature



P-DIP-20-1

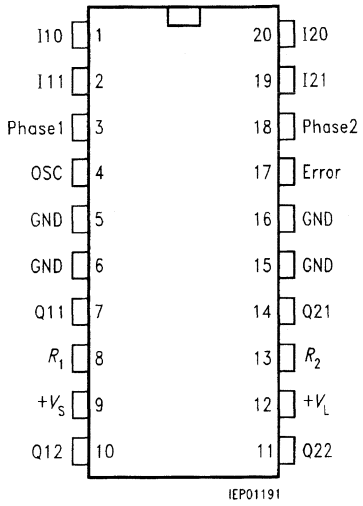
Type	Ordering Code	Package
▼ TLE 4727	Q67000-A-9099	P-DIP-20-1

▼ New type

The TLE 4727 is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate on constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 1.0 A per phase at operating voltages up to 25 V.

The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in a full-bridge configuration include fast integrated free-wheeling diodes and are free of crossover current. The device can be driven directly by a microprocessor in several modes by programming phase direction and current control of each bridge independently.

A stabilized 5 V output allows the supply of external components up to 5 mA. With the error output the TLE 4727 signals malfunction of the device. Setting the control inputs high resets the error flag and by reactivating the bridges one by one the location of the error can be found.



Pin Configuration
(top view)

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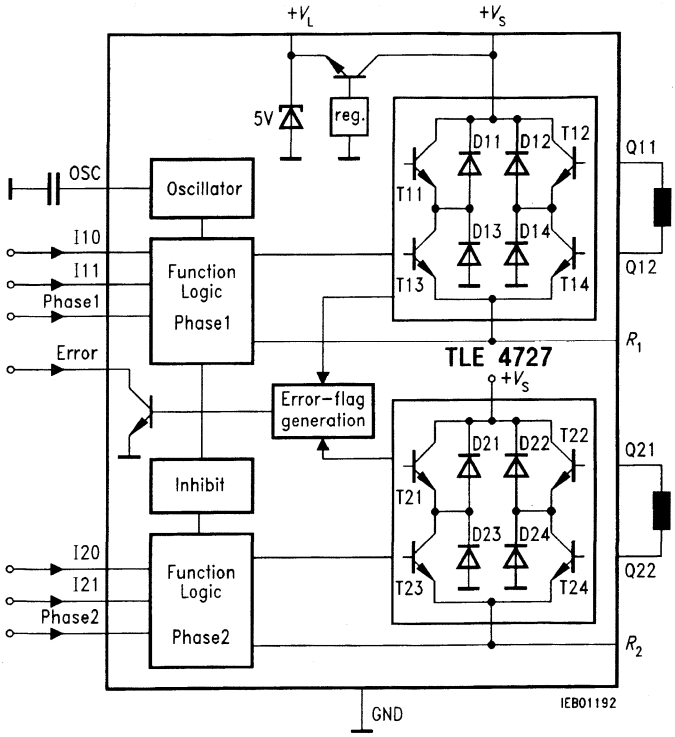
Pin Definitions and Functions

Pin	Function
1, 2, 19, 20	**Digital control inputs IX0, IX1** for the magnitude of the current of the particular phase. I_{set} = 375 mA with R_{Sense} = 1 Ω

IX1	IX0	Phase current	Example of motor status
H	H	0	No current *
H	L	0.133 x I_{set}	Hold
L	H	I_{set}	Normal mode
L	L	2 x I_{set}	Accelerate

*** "No Current" in both bridges inhibits the circuit and current consumption will sink below 2 mA**

3	**Input Phase 1**; controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.
5, 6, 15, 16	**Ground**; all pins are connected at leadframe internally.
4	**Oscillator**; works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.
8	**Resistor** R_1 for sensing the current in phase 1.
7, 10	**Push-pull outputs Q11, Q12** for phase 1 with integrated free-wheeling diodes.
9	**Supply voltage**; block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 47 µF in parallel with a ceramic capacitor of 220 nF.
12	**Logic supply voltage**; internally generated 5 V voltage for logic supply up to 5 mA; short circuit protected. Block to ground with a stable electrolytic capacitor of 4.7 µF
11, 14	**Push-pull outputs Q22, Q21** for phase 2 with integrated free wheeling diodes.
13	**Resistor** R_2 for sensing the current in phase 2.
17	**Error output**; signals with "low" one of the following errors: open load and overload of one or more outputs, overtemperature, overvoltage at + V_S.
18	**Input phase 2**; controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.



Block Diagram

Absolute Maximum Ratings

T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	0	45	V	–
Error output	V_{Err} I_{Err}	0 –	45 3	V mA	– –
Logic supply voltage	V_L	0	6.5	V	–
Output-current of V_L	I_L	–	–	–	int. limited
Output current	I_Q	–	1	A	–
Ground current	I_{GND}	–	2	A	–
Logic inputs	V_{Ixx}	– 15	15	V	I_{XX}; Phase 1, 2
R_1, R_2 input voltage	V_{RX}	– 0.3	5	V	
Diode currents to + V_S to ground	 I_{F+} I_{F-}	 – –	 1 1	 A A	 – –
Junction temperature	T_j	–	150	°C	max. 70.000 h
Operating junction temperature	T_{jop}	–	125	°C	10.000 h 750 mA each bridge
Storage temperature	T_{stg}	– 50	125	°C	
Thermal resistance system-air system-air (soldered on a 35 µm thick 20 cm² PC board copper area) system case	 $R_{th\ SA}$ $R_{th\ SA}$ $R_{th\ SC}$	 – – –	 56 40 17	 K/W K/W K/W	 – – measured on pin 5

Operating Range

Supply voltage	V_S	4.75	25	V	–
Current from logic supply	I_L	–	5	mA	–
Case temperature	T_C	– 40	125	°C	measured on pin 5 P_{diss} = 2 W
Output current	I_Q	–	750	mA	R_{Sense} = 1 Ω
Logic inputs	V_{IXX}	– 5	+ 5	V	I_{XX}; Phase 1, 2
Error output	V_{Err} I_{Err}	– 0	25 1	V mA	– –

Characteristics

V_S = 6 to18 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption no load at V_L						
from + V_S	I_S	–	1.5	–	mA	I_{XX} = H
from + V_S	I_S	–	30	–	mA	$I_{Q1,2}$ = 0.5 A
Oscillator						
Output charging current	I_{OSC}	–	110	–	µA	
Charging threshold	V_{OSCL}	–	1.4	–	V	T_j = 40 °C
Discharging threshold	V_{OSCH}	–	2.4	–	V	T_j = 40 °C
Frequency	f_{OSC}	–	25	–	kHz	C_{OSC} = 2.2 nF
Phase Current Selection (R_{sense} = 1 Ω)						
No current	I_Q	–	0	–	mA	I_{X0} = H; I_{X1} = H
Hold	I_Q	–	50	–	mA	I_{X0} = L; I_{X1} = H
Setpoint	I_Q	–	375	–	mA	I_{X0} = H; I_{X1} = L
Accelerate	I_Q	–	750	–	mA	I_{X0} = L; I_{X1} = L
Logic Inputs (I_{X1} ; I_{X0} ; phase x)						
Threshold	V_I	1.4	1.7	2.0	V	–
L-input current	I_{IL}	– 10	–	–	µA	V_I = 1.4 V
L-input current	I_{IL}	– 100	–	–	µA	V_I = 0 V
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
Error Output						
Saturation voltage	V_{ErrSat}	–	0.2	–	V	I_{Err} = 1 mA
Leakage current	I_{ErrL}	–	–	10	µA	V_{Err} = 25 V
Logic Supply Output						
Output voltage	V_L	4.5	5	5.5	V	1 mA < I_L < 5 mA T_j < 150 °C V_S = 6...45 V

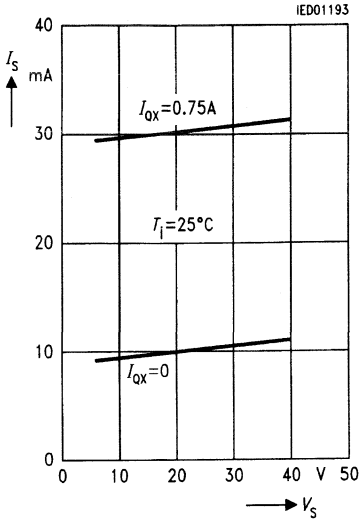
10

Characteristics (cont'd)

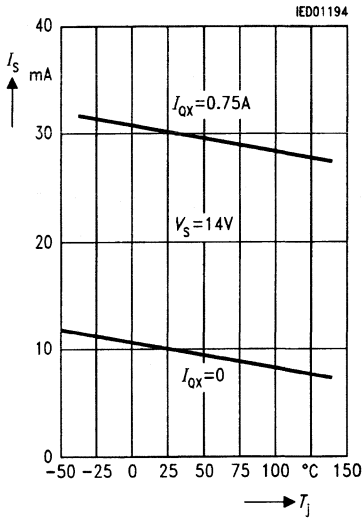
V_S = 6 to18 V; T_j = – 40 to 130 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Thermal Protection						
Shutdown	T_{jsd}	–	150	–	°C	$I_{Q1,2}$ = 0 A
Prealarm	T_{jpa}	–	130	–	°C	V_{Err} = L
Delta	ΔT_j	–	20	–	K	$\Delta T_j = T_{jsd} - T_{jpa}$
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satI}	–	0.4	–	V	I_Q = – 0.5 A
Saturation voltage	V_{satI}	–	1.0	–	V	I_Q = – 0.75 A
Reverse current	I_{RI}	–	900	–	µA	$V_S = V_Q$ = 40 V
Forward voltage	V_{FI}	–	0.9	–	V	I_Q = 0.5 A
Forward voltage	V_{FI}	–	1.0	–	V	I_Q = 0.75 A
Diode Transistor Source Pair (D11, T11; D12, T12; D21, T21; D22, T22)						
Saturation voltage	V_{satuCI}	–	1.0	–	V	I_Q = 0.5 A; charge
Saturation voltage	V_{satuD}	–	0.4	–	V	I_Q = 0.5 A; discharge
Saturation voltage	V_{satuC}	–	1.2	–	V	I_Q = 0.75 A; charge
Saturation voltage	V_{satuD}	–	0.8	–	V	I_Q = 0.75 A; discharge
Reverse current	I_{Ru}	–	800	–	µA	V_S = 40 V, V_Q = 0 V
Forward voltage	V_{Fu}	–	1.0	–	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	–	1.1	–	V	I_Q = – 0.75 A
Diode leakage current	I_{SL}	–	1	–	mA	I_F = – 0.75 A

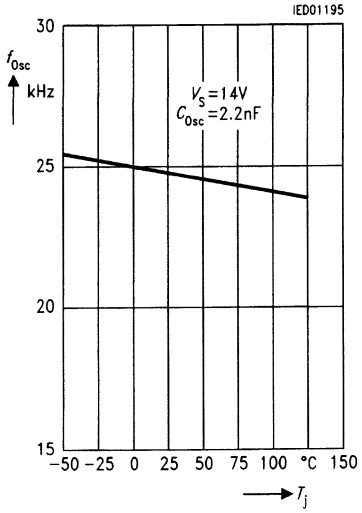
Quiescent Current I_S versus Supply Voltage V_S



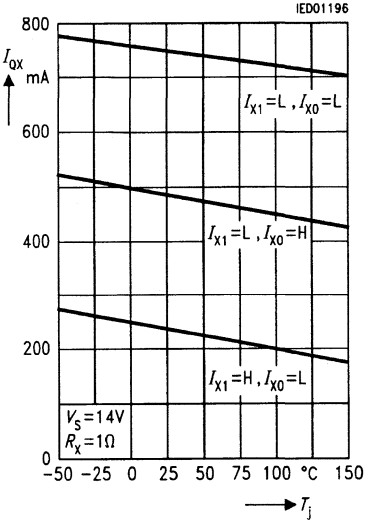
Quiescent Current I_S versus Junction Temperature T_j



Oscillator Frequency f_{Osc} versus Junction Temperature T_j



Output Current I_{QX} versus Junction Temperature T_j



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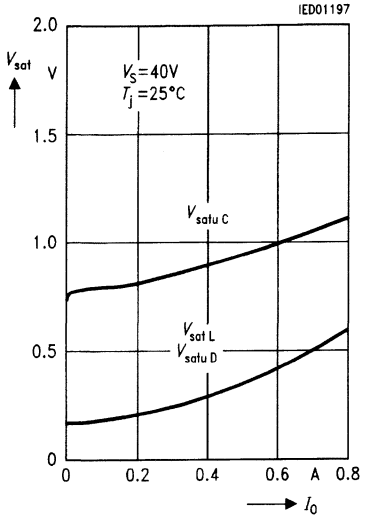
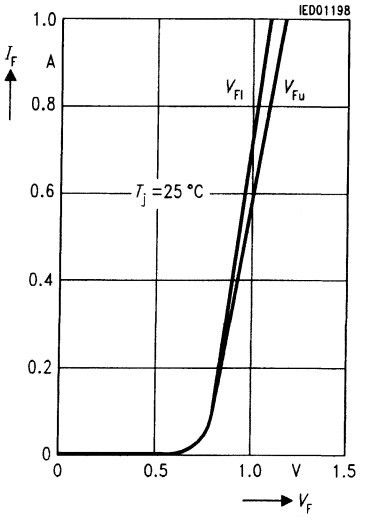
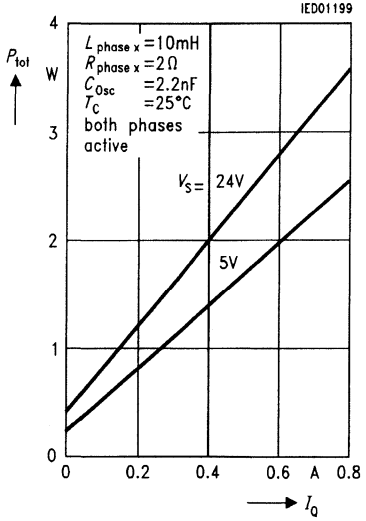
Output Saturation Voltages V_{sat} versus Output Current I_Q



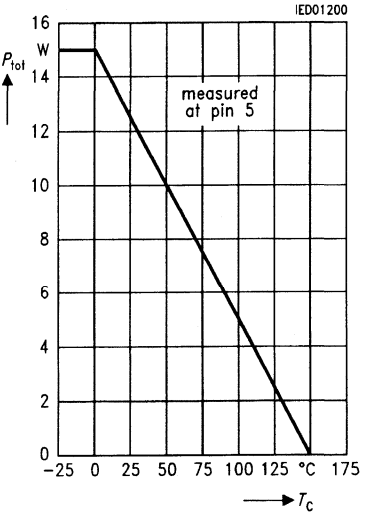
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



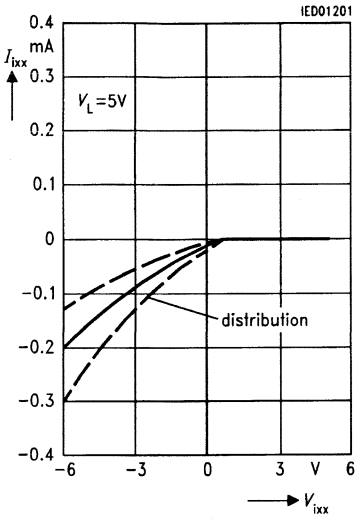
Typical Power Dissipation P_{tot} versus Output Current I_Q (Non Stepping)



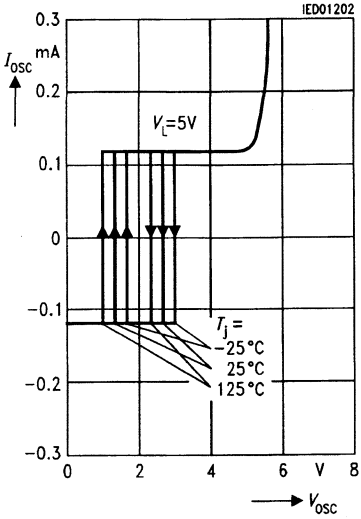
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



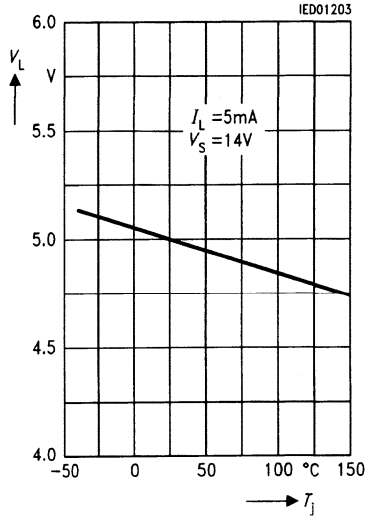
Input Characteristics of I_{xx}, Phase X



Input Characteristics of OSC



Logic Supply Output Voltage versus Junction Temperature T_j



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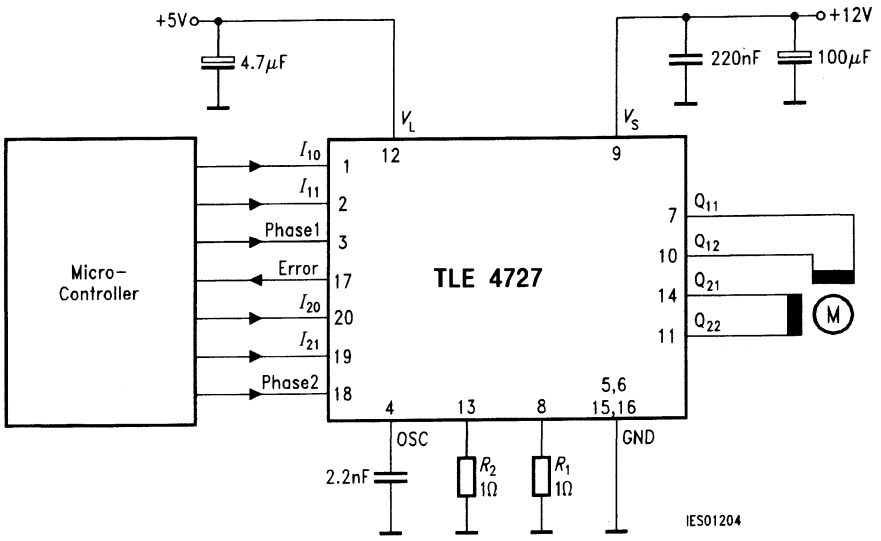
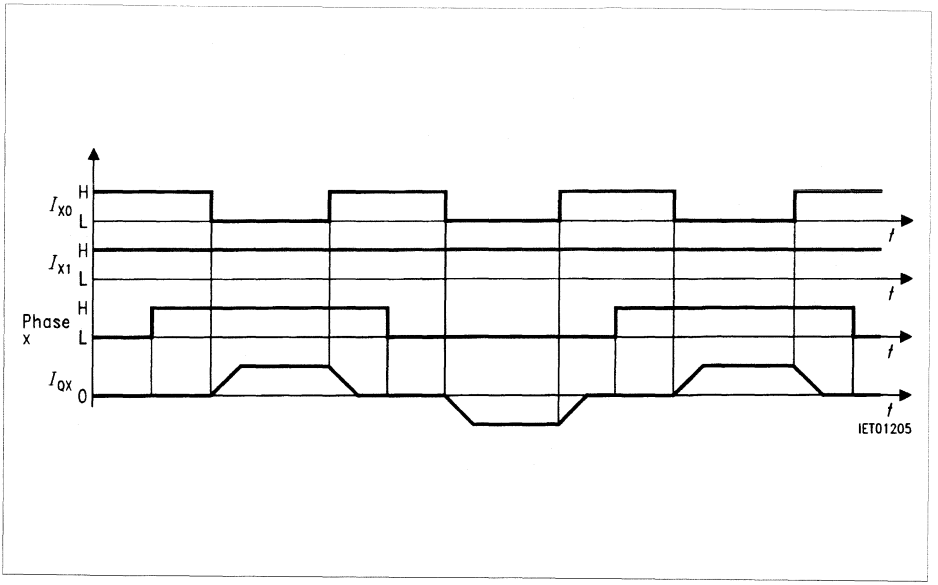
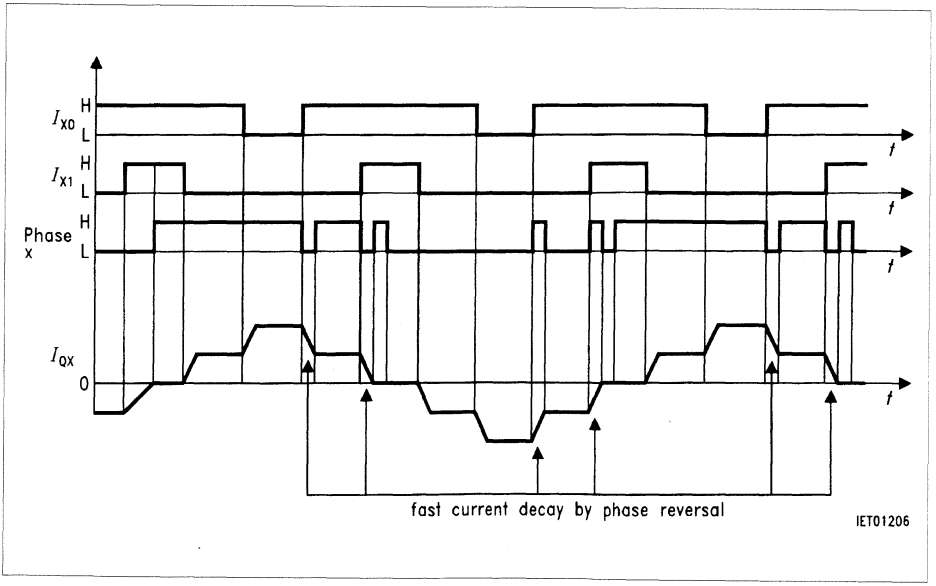


Application Circuit



Half-Step Operation



Quarter-Step Operation with Phase Reversal for Fast Current Decay

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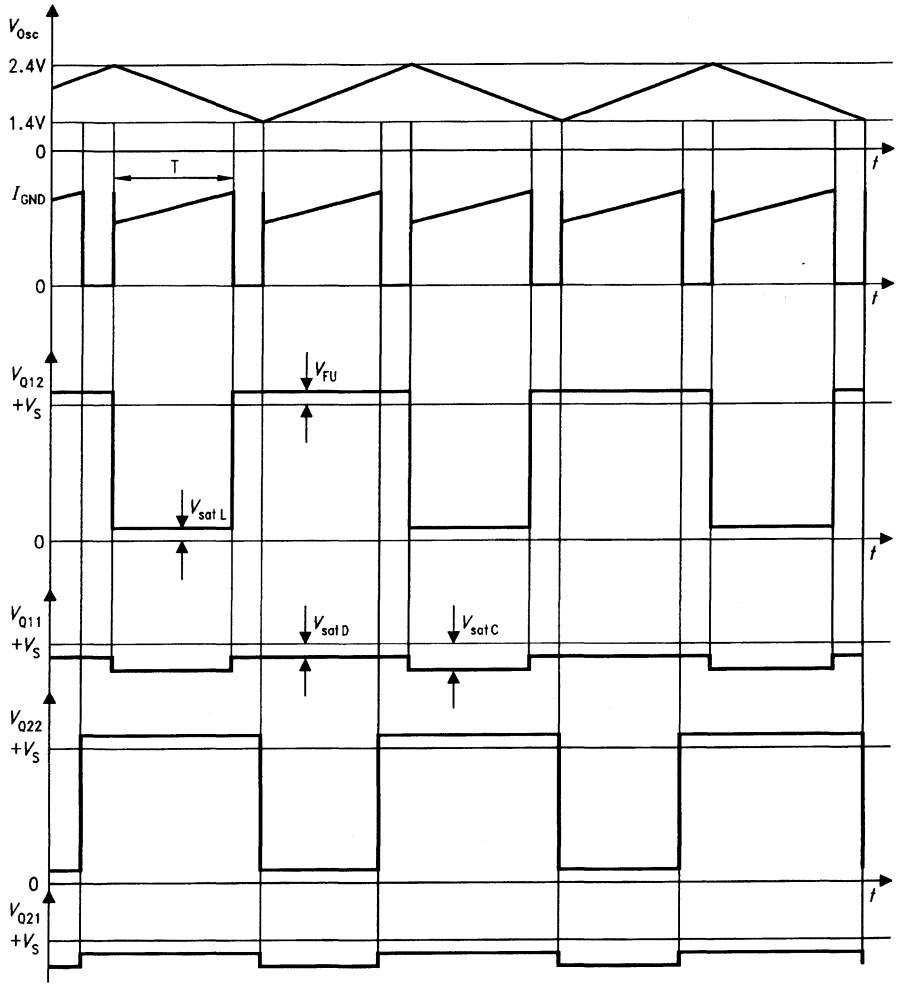
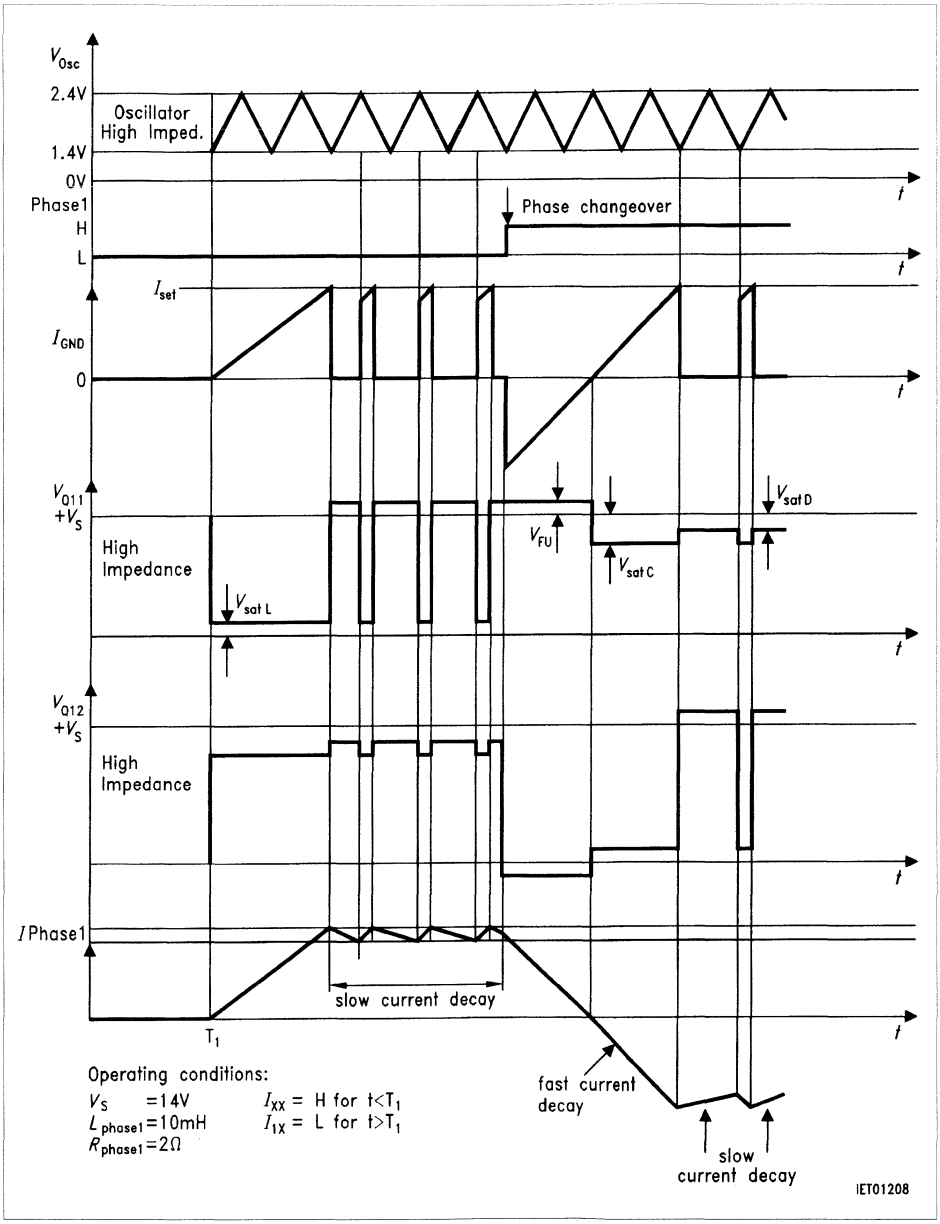


Current Control



Phase Reversal and Inhibit

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Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages),
quiescent losses P_q	(quiescent current times supply voltage) and
switching losses P_s	(turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

$$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$$

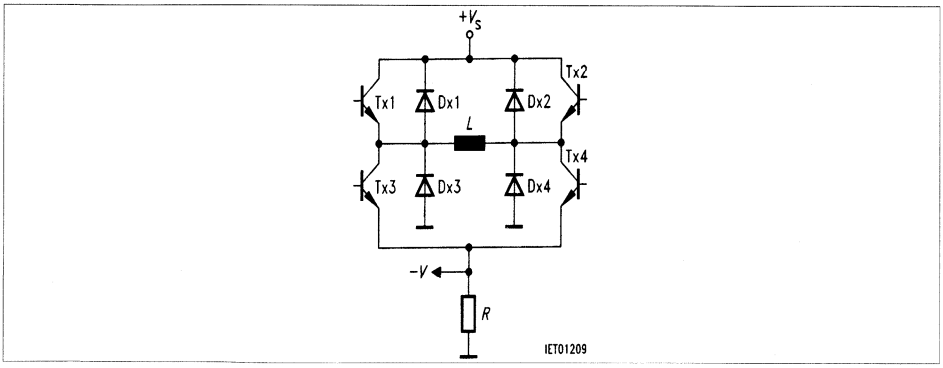
where

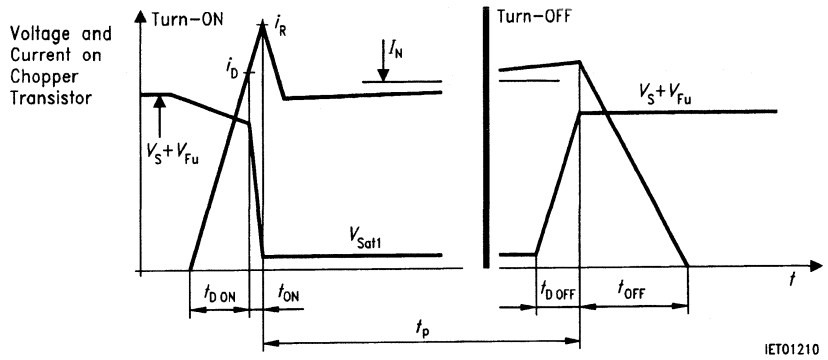
$$P_{sat} \cong I_N \{ V_{satI} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_S$$

$$P_S \cong \frac{V_S}{T} \{ \frac{i_D \times t_{DON}}{2} + \frac{(i_D + i_R) \times t_{ON}}{4} + \frac{I_N}{2} (t_{DOFF} + t_{OFF}) \}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFF delay
T = cycle duration
d = duty cycle t_p / T
V_{sat} = saturation voltage of sink transistor (TX3, TX4)
V_{satuC} = saturation voltage of source transistor (TX1, TX2) during charge cycle
V_{satuD} = saturation voltage of source transistor (TX1, TX2) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (DX1, DX2)
V_S = supply voltage





Voltage and Current on Chopper Transistor

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Application Hints

The TLE 4727 is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE 4727 will work with supply voltages ranging from 4.75 V to 25 V at pin V_s. Surges exceeding 25 V at V_s will turn off the circuit, but wont harm it up to 45 V. As soon as the voltage drops below approximately 25 V the TLE 4727 will turn on again.

As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.22 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_1 and R_2. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.05 V, 0.375 V and 0.75 V). These thresholds are not affected by variations of V_S. Consequently unstabilized supplies will not affect the performance of the regulation.

Due to chopper control fast current rises (up to 10A/µs) will occure at the sensing resistors R_1 and R_2. To prevent malfunction of the current sensing mechanism R_1 and R_2 should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desireable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE 4727 by a pulse generator overdriving the oscillator loading currents (approximately ± 100 µA). In these applications low level should be between 0 V and 1 V while high level should be between 2.6 V and 5 V.

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE 4727 uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented.

Application Hints (cont'd)

Error Monitoring

The error output signals with low-potential one of the following errors:

overtemperature: implemented as pre-alarm; appears approximately 20 K before thermal shut down.

short circuit: a connection of one output to + V_S or GND or a shortening of the load for longer than 20 µs sets an internal error flip flop.
A phase change-over of the affected bridge resets the flip flop.
Being a separate flip flop for each bridge, the error can be located in such way.

underload: the recirculation of the inductive load will be detected. If there is no recirculation after a phase change-over, the error flip flop will be set.

SIEMENS

2-Phase Stepper-Motor Driver

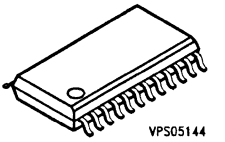
TLE 4728

Preliminary Data

Bipolar-IC

Features

- 2 x 1 amp. full bridge outputs
- Integrated driver, control logic and current control (chopper)
- Fast free-wheeling diodes
- Max. supply voltage 45 V
- Overvoltage cut-out
- Output stages are free of crossover current
- Offset-phase turn-ON of output stages
- All outputs short-circuit proof
- Error-flag overload, open load, overtemperature
- SMD package P-DSO-24-1



P-DSO-24-1

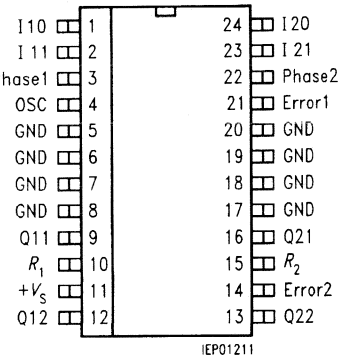
	Type	Ordering Code	Package
▼	TLE 4728 G	Q6700-A9077	P-DSO-24-1 (SMD)

▼ New type

TLE 4728 G is a bipolar, monolithic IC for driving bipolar stepper motors, DC motors and other inductive loads that operate by constant current. The control logic and power output stages for two bipolar windings are integrated on a single chip which permits switched current control of motors with 1.0 A per phase at operating voltages up to 25 V.

The direction and value of current are programmed for each phase via separate control inputs. A common oscillator generates the timing for the current control and turn-on with phase offset of the two output stages. The two output stages in full-bridge configuration include fast integrated free-wheeling diodes and are free of crossover current. The device can be driven directly by microprocessor in several modes by programming phase direction and current control of each bridge independently.

With the two error outputs the TLE 4728; G signals malfunction of the device. Setting the control inputs high resets the error flag and by reactivating the bridges one by one the location of the error can be found.



Pin Configuration
(top view)

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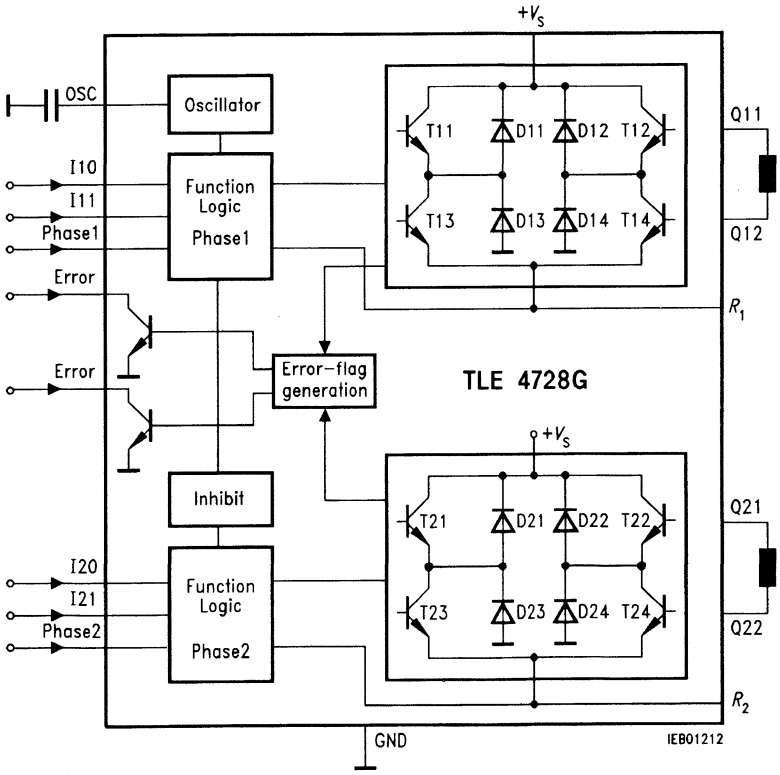
Pin Definitions and Functions

Pin	Function
1, 2, 23, 24	**Digital control inputs IX0, IX1** for the magnitude of the current of the particular phase. I_{set} = 375 mA with R_{sense} = 1 Ω **IX1 IX0** / **Phase current** / **Example of motor status** H H / 0 / No current * H L / 0.133 x I_{set} / Hold L H / I_{set} / Normal mode L L / 2 x I_{set} / Accelerate *"No current" in both bridges inhibits the circuit and current consumption will sink below 2 mA
3	**Input phase 1;** controls the current through phase winding 1. On H-potential the phase current flows from Q11 to Q12, on L-potential in the reverse direction.
5...8, 17...20	**Ground;** all pins are connected at leadframe internally.
4	**Oscillator;** works at approx. 25 kHz if this pin is wired to ground across 2.2 nF.
10	**Resistor R_1** for sensing the current in phase 1.
9, 12	**Push-pull outputs Q11, Q12** for phase 1 with integrated free-wheeling diodes.
11	**Supply voltage;** block to ground, as close as possible to the IC, with a stable electrolytic capacitor of at least 47 µF in parallel with a ceramic capacitor of 220 nF.
14	**Error 2 output;** signals with "low" the errors: short circuit of one or more outputs or overtemperature.
13, 16	**Push-pull outputs Q22, Q21** for phase 2 with integrated free-wheeling diodes.
15	**Resistor R_2** for sensing the current in phase 2.
21	**Error 1 output;** signals with "low" the errors: open load of one or more outputs or overtemperature.
22	**Input phase 2;** controls the current flow through phase winding 2. On H-potential the phase current flows from Q21 to Q22, on L potential in the reverse direction.



Block Diagram

Absolute Maximum Ratings

T_A = – 40 to 150°C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	0	45	V	–
Error outputs	V_{Err} I_{Err}	0 –	45 3	V mA	– –
Output current	I_Q	–	1	A	–
Ground current	I_{GND}	–	2	A	–
Logic inputs	V_{Ixx}	–15	15	V	I_{xx}; Phase 1, 2
R_1, R_2 input voltage	V_{RX}	– 0.3	5	V	–
Diode currents to + V_S to ground	 I_{F+} I_{F-}	 – –	 1 1	 A A	 – –
Junction temperature	T_j	–	150	°C	max. 70.000 h
Operating junction temperature	T_{Jop}	–	125	°C	10.000 h 750 mA each bridge
Storage temperature	T_{stg}	– 50	125	°C	
Thermal resistances system-air system-air (soldered on a 35 µm thick 20 cm² PC board copper area) system-case	 $R_{th\ SA}$ $R_{th\ SA}$ $R_{th\ SC}$	 – – –	 75 35 15	 K/W K/W K/W	 – – measured on pin 5

Operating Range

Supply voltage	V_S	4.75	25	V	–
Case temperature	T_C	– 40	125	°C	measured on pin 5 P_{diss} = 2 W
Output current	I_Q	–	750	mA	R_{Sense} = 1 Ω
Logic inputs	V_{Ixx}	– 5	+ 5	V	I_{xx}; Phase 1, 2
Error outputs	V_{Err} I_{Err}	– 0	25 1	V mA	– –

Characteristics

V_S = 6 to18 V; T_j = – 40 to 130°C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
From + V_S	I_S	–	1.5	–	mA	I_{XX} = H
From + V_S	I_S	–	30	–	mA	$I_{Q1,2}$ = 0.5 A
Oscillator						
Output charging current	I_{OSC}	–	110	–	µA	–
Charging threshold	V_{OSCL}	–	1.4	–	V	T_j = 40°C
Discharging threshold	V_{OSCH}	–	2.4	–	V	T_j = 40°C
Frequency	f_{OSC}	–	25	–	kHz	C_{OSC} = 2.2 nF
Phase Current Selection (R_{sense} = 1 Ω)						
No current	I_Q	–	0	–	mA	I_{X0} = H; I_{X1} = H
Hold	I_Q	–	50	–	mA	I_{X0} = L; I_{X1} = H
Setpoint	I_Q	–	375	–	mA	I_{X0} = H; I_{X1} = L
Accelerate	I_Q	–	750	–	mA	I_{X0} = L; I_{X1} = L
Logic Inputs (I_{X1} ; I_{X0} ; phase x)						
Threshold	V_I	1.4	1.7	2.0	V	–
L-input current	I_{IL}	– 10	–	–	µA	V_I = 1.4 V
L-input current	I_{IL}	– 100	–	–	µA	V_I = 0 V
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
Error Outputs						
Saturation voltage	V_{ErrSat}	–	0.2	–	V	I_{Err} = 1mA
Leakage current	I_{ErrL}	–	–	10	µA	V_{Err} = 25 V
Thermal Protection						
Shutdown	T_{jsd}	–	150	–	°C	$I_{Q1,2}$ = 0 A
Prealarm	T_{jpa}	–	130	–	°C	V_{Err} = L
Delta	ΔT_j	–	20	–	K	$\Delta T_j = T_{jsd} - T_{jpa}$

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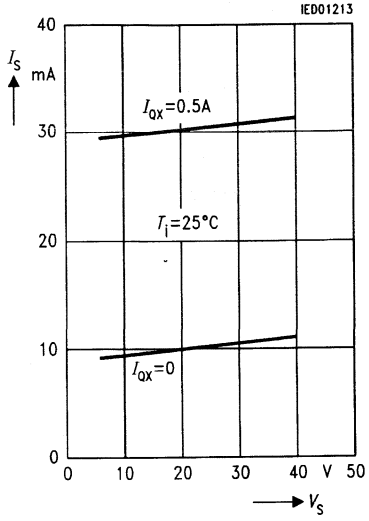
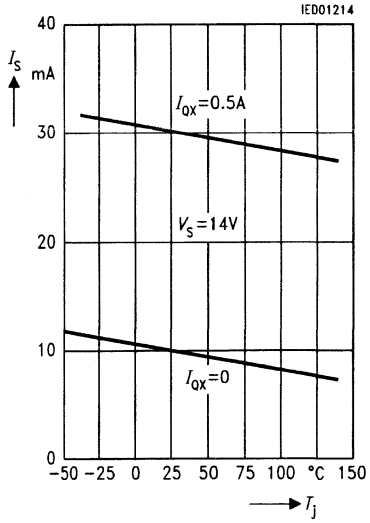
Characteristics (cont'd)
V_S = 6 to18 V; T_j = – 40 to 130°C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power Outputs						
Diode Transistor Sink Pair (D13, T13; D14, T14; D23, T23; D24, T24)						
Saturation voltage	V_{satI}	–	0.4	–	V	I_Q = – 0.5 A
Saturation voltage	V_{satI}	–	1.0	–	V	I_Q = – 0.75 A
Reverse current	I_{RI}	–	900	–	µA	$V_S = V_Q$ = 40 V
Forward voltage	V_{FI}	–	0.9	–	V	I_Q = 0.5 A
Forward voltage	V_{FI}	–	1.0	–	V	I_Q = 0.75 A
Diode Transistor Source Pair (T11, D11; T12, D12; T21, D21; T22, D22)						
Saturation voltage	V_{satuC}	–	1.0	–	V	I_Q = 0.5 A; charge
Saturation voltage	V_{satuD}	–	0.4	–	V	I_Q = 0.5 A; discharge
Saturation voltage	V_{satuC}	–	1.2	–	V	I_Q = 0.75 A; charge
Saturation voltage	V_{satuD}	–	0.8	–	V	I_Q = 0.75 A; discharge
Reverse current	I_{Ru}	–	800	–	µA	V_S = 40 V, V_Q = 0 V
Forward voltage	V_{Fu}	–	1.0	–	V	I_Q = – 0.5 A
Forward voltage	V_{Fu}	–	1.1	–	V	I_Q = – 0.75 A
Diode leakage current	I_{SL}	–	1	–	mA	I_F = – 0.75 A

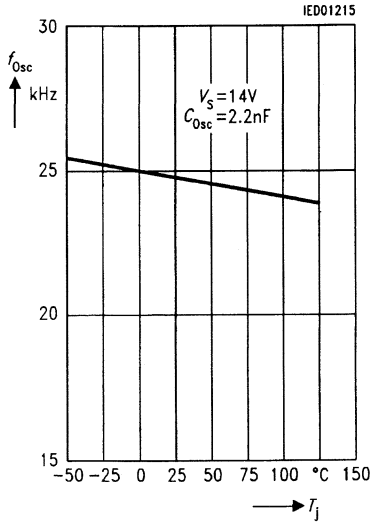
Quiescent Current I_S versus Supply Voltage V_S



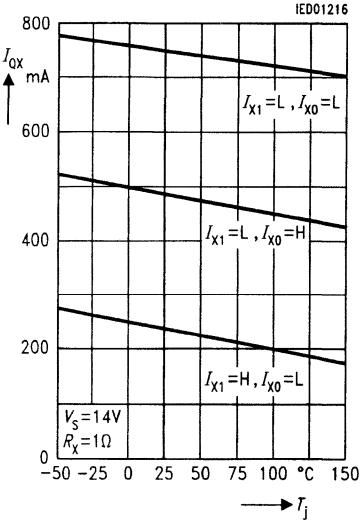
Quiescent Current I_S versus Junction Temperature T_j



Oscillator Frequency f_{Osc} versus Junction Temperature T_j



Output Current I_{QX} versus Junction Temperature T_j



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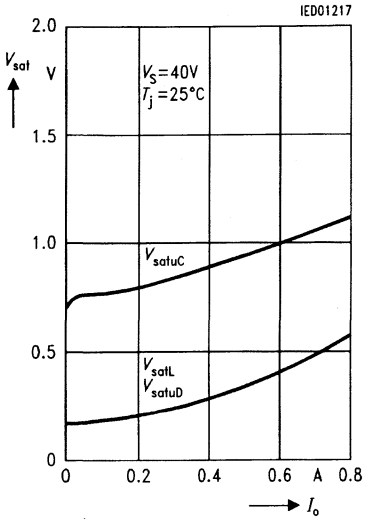
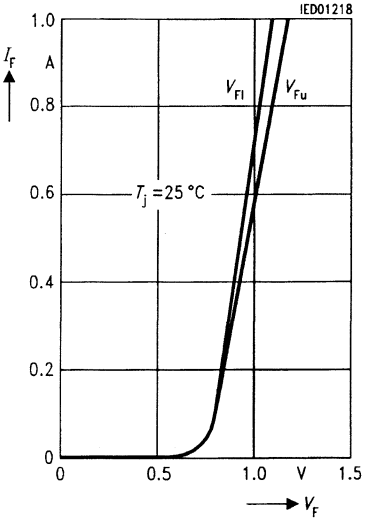
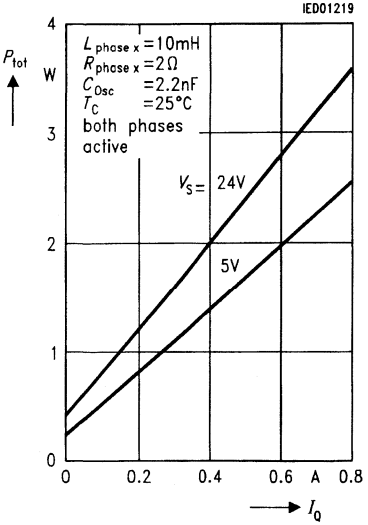
Output Saturation Voltages V_{sat} versus Output Current I_Q



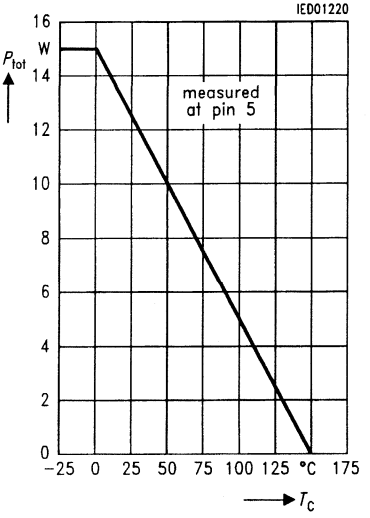
Forward Current I_F of Free-Wheeling Diodes versus Forward Voltages V_F



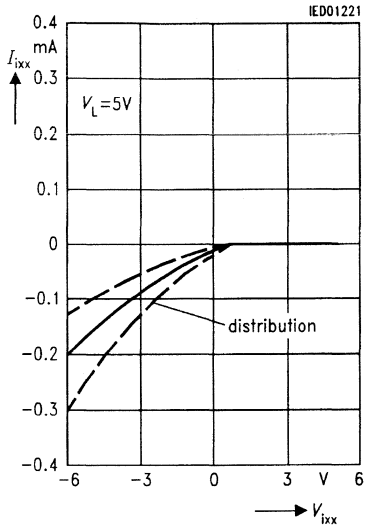
Typical Power Dissipation P_{tot} versus Output Current I_Q (Non Stepping)



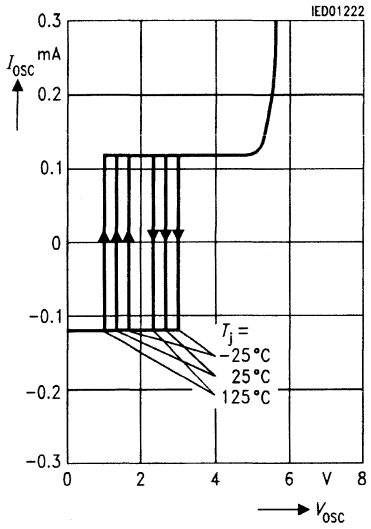
Permissible Power Dissipation P_{tot} versus Case Temperature T_C



Input Characteristics of I_{xx} Phase X



Input Characteristics of OSC



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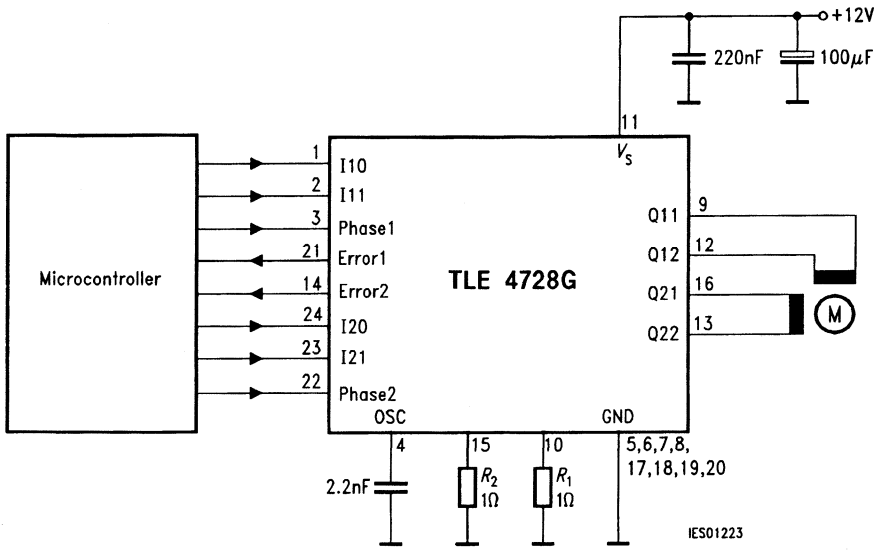
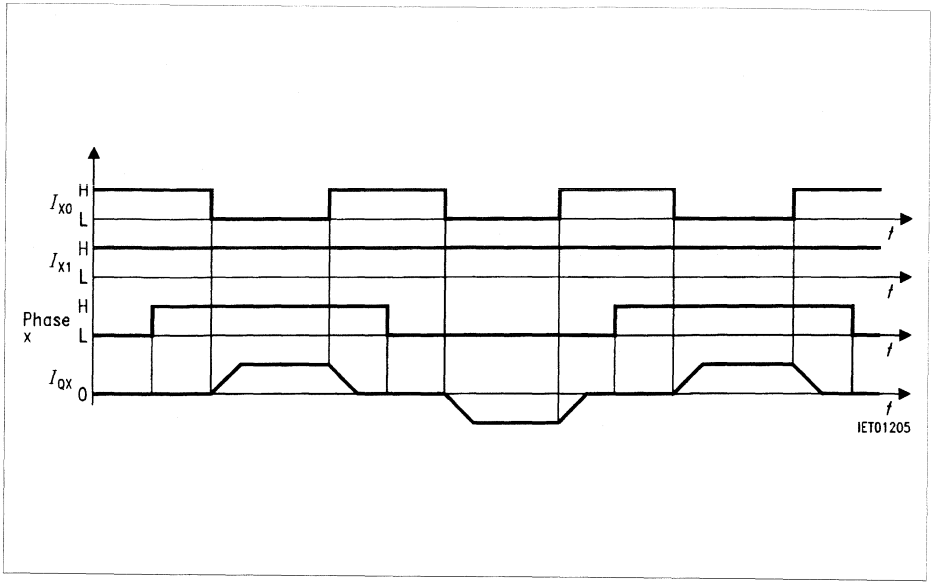
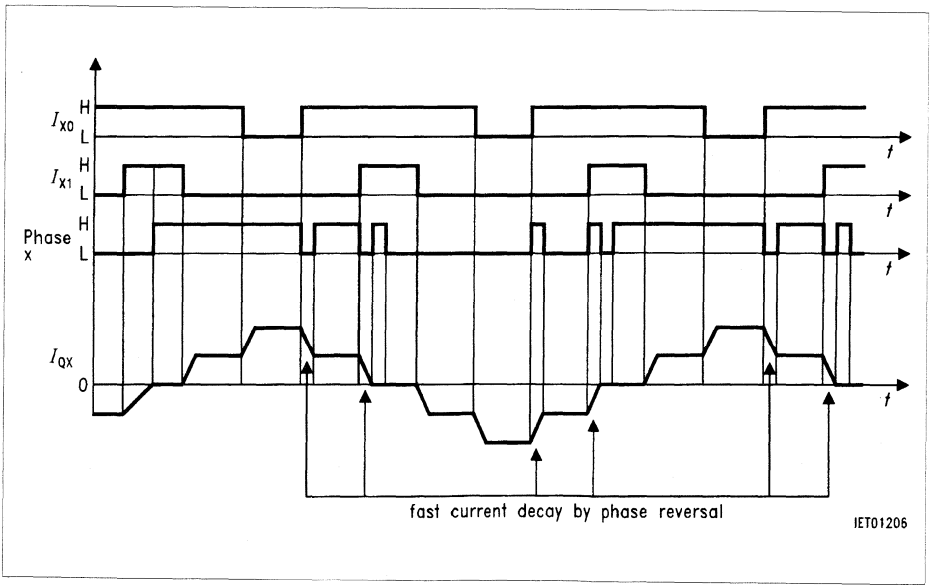


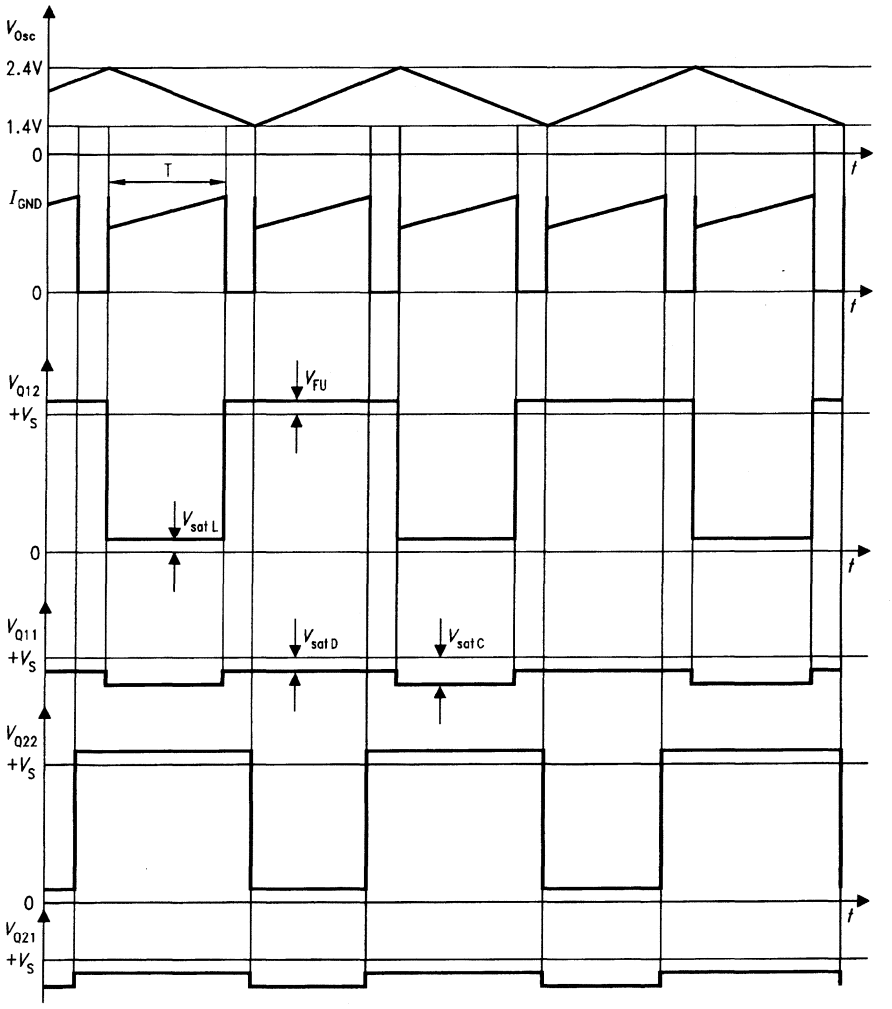
Application Circuit



Half-Step Operation



Quarter-Step Operation with Phase Reversal for Fast Current Decay



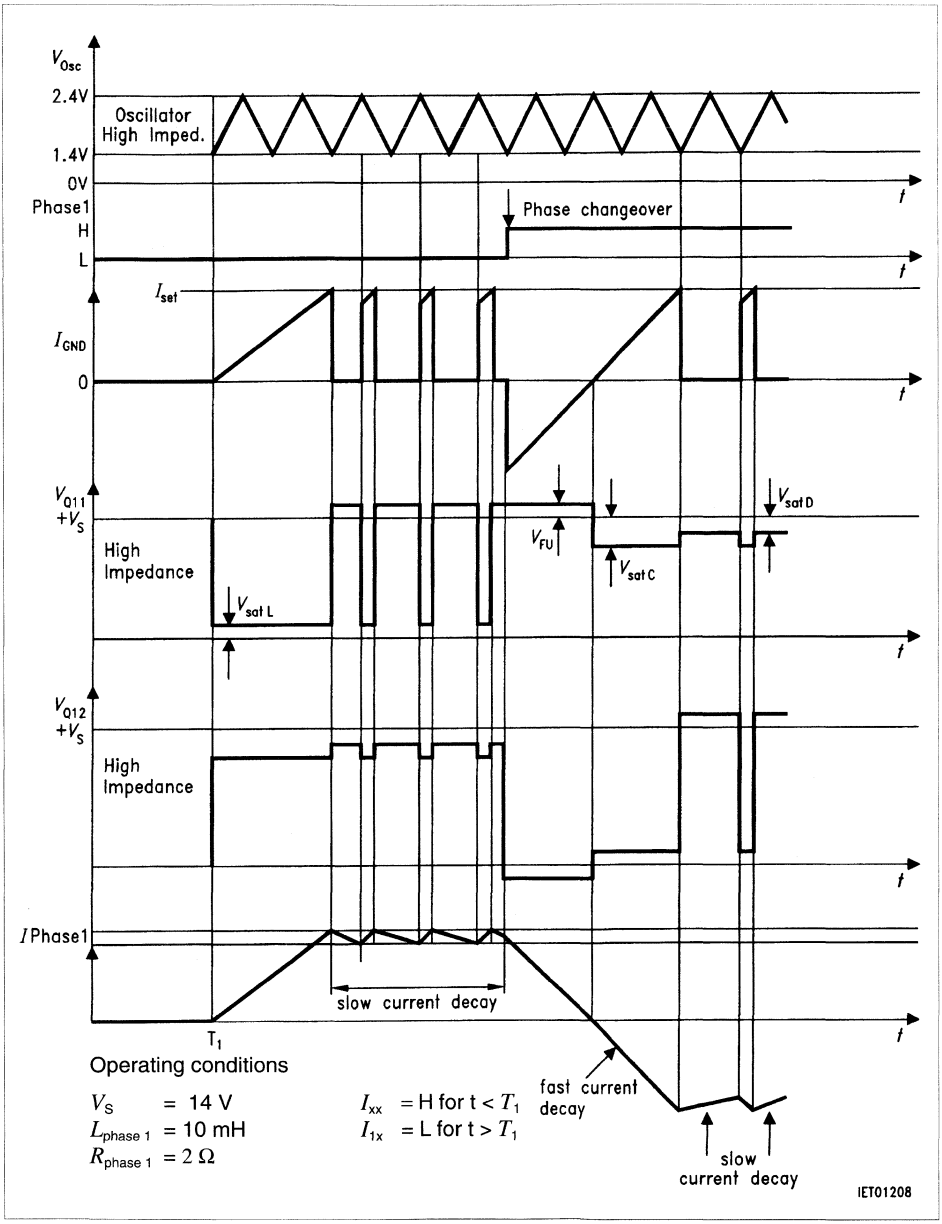
Operating conditions

V_S = 14 V
$L_{phase\,x}$ = 10 mH
$R_{phase\,x}$ = 2 Ω

Phase $_x$ = H
I_{xx} = L

IET01207

Current Control



Phase Reversal and Inhibit

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Calculation of Power Dissipation

The total power dissipation P_{tot} is made up of

saturation losses P_{sat}	(transistor saturation voltage and diode forward voltages),
quiescent losses P_q	(quiescent current times supply voltage) and
switching losses P_s	(turn-ON / turn-OFF operations).

The following equations give the power dissipation for chopper operation without phase reversal. This is the worst case, because full current flows for the entire time and switching losses occur in addition.

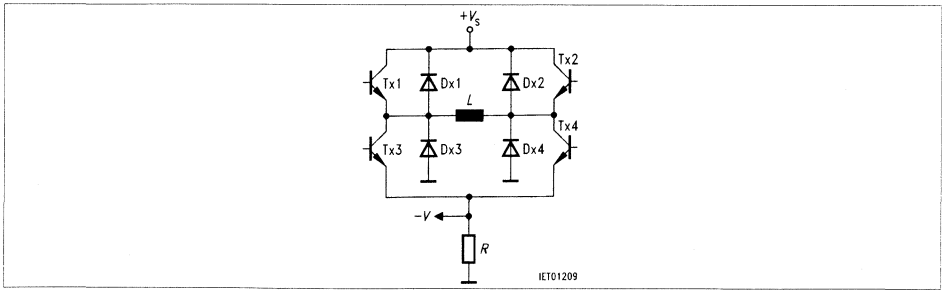
$P_{tot} = 2 \times P_{sat} + P_q + 2 \times P_s$
where

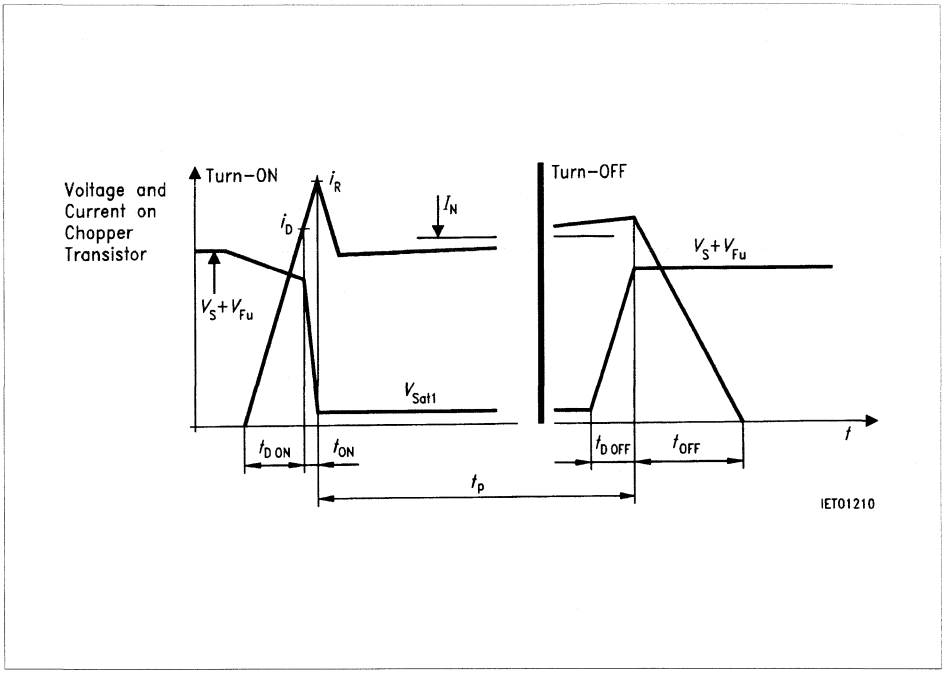
$$P_{sat} \cong I_N \{ V_{satI} \times d + V_{Fu} (1 - d) + V_{satuC} \times d + V_{satuD} (1 - d) \}$$

$$P_q = I_q \times V_s$$

$$P_q \cong \frac{V_S}{T} \{ \frac{i_D \times t_{DON}}{2} + \frac{(i_D + i_R) \times t_{ON}}{4} + \frac{I_N}{2} (t_{DOFF} + t_{OFF}) \}$$

I_N = nominal current (mean value)
I_q = quiescent current
i_D = reverse current during turn-on delay
i_R = peak reverse current
t_p = conducting time of chopper transistor
t_{ON} = turn-ON time
t_{OFF} = turn-OFF time
t_{DON} = turn-ON delay
t_{DOFF} = turn-OFF delay
T = cycle duration
d = duty cycle t_p / T
V_{satL} = saturation voltage of sink transistor (TX3, TX4)
V_{satuC} = saturation voltage of source transistor (TX1, TX2) during charge cycle
V_{satuD} = saturation voltage of source transistor (TX1, TX2) during discharge cycle
V_{Fu} = forward voltage of free-wheeling diode (DX1, DX2)
V_S = supply voltage





Voltage and Current on Chopper Transistor

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Application Hints

The TLE 4728 G is intended to drive both phases of a stepper motor. Special care has been taken to provide high efficiency, robustness and to minimize external components.

Power Supply

The TLE 4728 G will work with supply voltages ranging from 4.75 V to 25 V at pin V_S. Surges exceeding 25 V at V_S will turn off the circuit, but wont harm it up to 45 V. As soon as the voltage drops below approximately 25 V the TLE 4728 G will turn on again.

As the circuit operates with chopper regulation of the current, interference generation problems can arise in some applications. Therefore the power supply should be decoupled by a 0.22 µF ceramic capacitor located near the package. Unstabilized supplies may even afford higher capacities.

Current Sensing

The current in the windings of the stepper motor is sensed by the voltage drop across R_1 and R_2. Depending on the selected current internal comparators will turn off the sink transistor as soon as the voltage drop reaches certain thresholds (typical 0 V, 0.05 V, 0.375 V and 0.75 V). These thresholds are not affected by variations of V_S. Consequently unstabilized supplies will not affect the performance of the regulation.

Due to chopper control fast current rises (up to 10 A/µs) will occure at the sensing resistors R_1 and R_2. To prevent malfunction of the current sensing mechanism R_1 and R_2 should be pure ohmic. The resistors should be wired to GND as directly as possible. Capacitive loads such as long cables (with high wire to wire capacity) to the motor should be avoided for the same reason.

Synchronizing Several Choppers

In some applications synchrone chopping of several stepper motor drivers may be desireable to reduce acoustic interference. This can be done by forcing the oscillator of the TLE 4728 G by a pulse generator overdriving the oscillator loading currents (approximately ± 100 µA). In these applications low level should be between 0 V and 1 V while high level should between 2.6 V and 5 V.

Application Hints (cont'd)

Optimizing Noise Immunity

Unused inputs should always be wired to proper voltage levels in order to obtain highest possible noise immunity.

To prevent crossconduction of the output stages the TLE 4728 G uses a special break before make timing of the power transistors. This timing circuit can be triggered by short glitches (some hundred nanoseconds) at the Phase inputs causing the output stage to become high resistive during some microseconds. This will lead to a fast current decay during that time. To achieve maximum current accuracy such glitches at the Phase inputs should be avoided by proper control signals.

Thermal Shut Down

To protect the circuit against thermal destruction, thermal shut down has been implemented.

Error Monitoring

The error output signals with low-potential one of the following errors:

overtemperature: implemented as pre-alarm; appears approximately 20 K before thermal shut down.

short circuit: a connection of one output to + V_S or GND or a shortening of the load for longer than 20 µs sets an internal error flip flop. A phase change-over of the affected bridge resets the flip flop. Being a separate flip flop for each bridge, the error can be located in such way.

open load: to detect an open load, the recirculation of the inductive load is watched. If there is no recirculation after a phase change-over, the error flip flop will be set.

10

Application Hints (cont'd)

Logic Table

Kind of Error	Error Output	
	Error 1	**Error 2**
No error	H	H
Short circuit	H	L
Open load	L	H
Temperature pre-alarm	L	L

additional hints:

- except short circuits in practice may appear ohmic shunts in parts of the windings of a stepper motor. If such defects do not cause the maximum current, no error will be detected.
- in some kinds of short circuits there won't flow any current through the motor. Therefore after a phase-changeover will be no inductive recirculation and the error "open load" appears additional.

SIEMENS

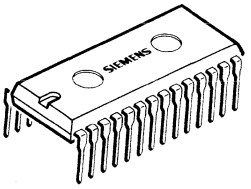
Pulse-Width Modulator

SLE 4520

MOS IC

Features

- Digital sine synthesis for controlling the speed and torque of three-phase motors
- 2-chip solution (e.g. SAB 8051 with SLE 4520) for easy configuration of a powerful frequency converter.
- Motor frequencies from 0 to 3 kHz selectable at a switching frequency up to 23.4 kHz
- Adaptation to different output stages through programmable dead time.
- Functional and performance features determined by dedicated software.



VPD 05037

P-DIP-28

Type	Ordering Code	Package
■ S SLE 4520	Q671000-H8271	P-DIP-28

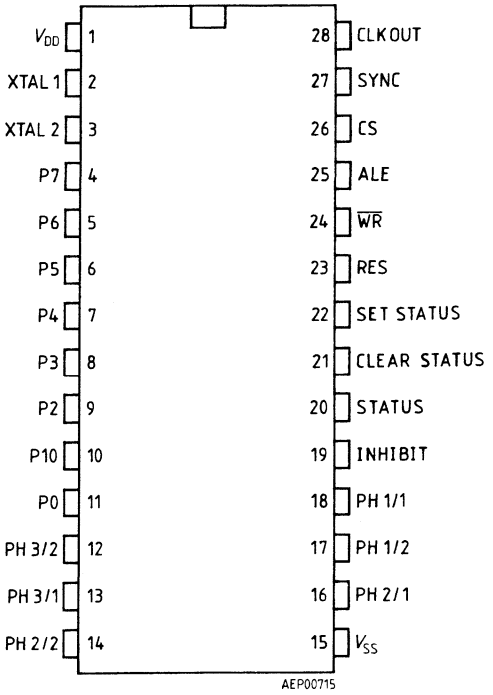
■ Not for new design

Application

The new pulse-width modulator (PWM) converts an 8-bit data word into a rectangular signal of corresponding width.

Three independently operating channels consisting of a latch, loadable counter and zero detector are used for this purpose. Together with a microcontroller (e.g. SAB 8051) and suitable software, pulses are generated to drive AC converters and inverters (three-phase) with an almost unlimited range of waveforms (sinusoidal, triangular) and phase relationships. An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program dead times are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage the V/f ratio of which is kept almost constant with variable frequency. For the generation of this three-phase voltage a frequency converter is required, which rectifies and filters the AC supply voltage and, subsequently, reconverts it into an AC voltage of another frequency the aid of a drive circuit and three power half-bridges. In order to avoid high losses the output stages operate in switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulses with a repetition frequency (switching frequency) up to and above the audible range, a drive block consisting of the SAB 8051 microcontroller and the SLE 4520 PWM as a minimum configuration has proved to be best suited to do the job.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{DD}	+ 5 V pin
2	XTAL1	Crystal pin
3	XTAL2	Crystal pin
4	P7	Data bus pins (inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P10	
11	P0	
12	PH3/2	Output phase 3 inverted
13	PH3/1	Output phase 3 normal (active low)
14	PH2/2	Output phase 2 inverted
15	V_{SS}	Ground
16	PH2/1	Output phase 2 normal (active low)
17	PH1/2	Output phase 1 inverted
18	PH1/1	Output phase 1 normal (active low)
19	INHIBIT	Inhibit (active high) sets all phase outputs to high
20	STATUS	Output of status flipflop
21	CLEAR STATUS	Resets status flipflop
22	SET STATUS	Sets status flipflop
23	RES	Chip reset
24	$\overline{WR}$	Input for $\overline{WR}$ pulse from microcontroller
25	ALE	Input for ALE clock from microcontroller
26	CS	Chip select
27	SYNC	Input for trigger pulse from microcontroller
28	CLK OUT	Output crystal frequency for microcontroller

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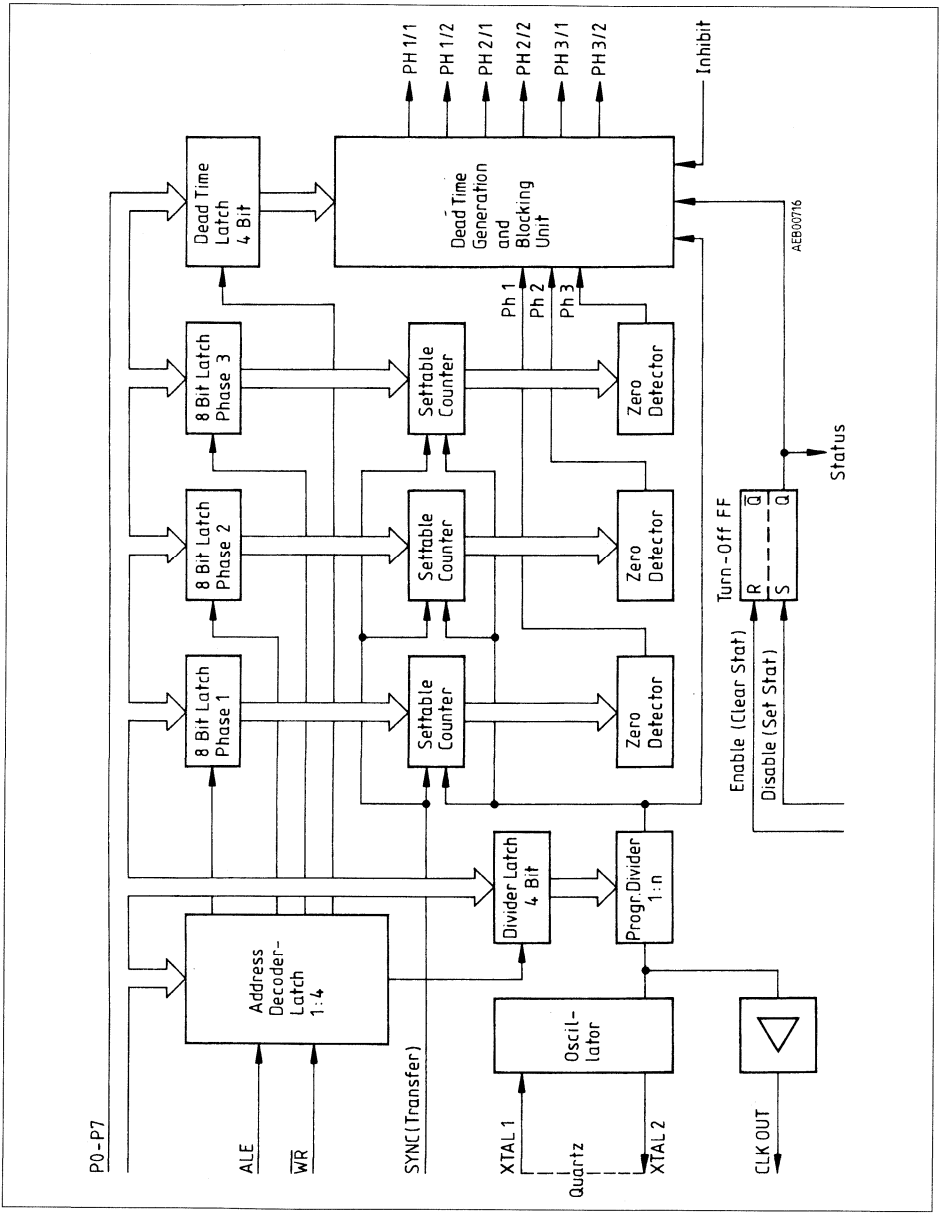

Block Diagram

Functional Description

The following description deals with the combination of the SAB 8051 microcontroller and the SLE 4520 PWM and a program developed by Siemens. Other hardware combinations are possible as well.

An on-chip oscillator directly feeds the programmable prescaler and has a buffered output for the connected microcontroller. The interface to the microcontroller has a width of 8 bits.

Data from the SAB 8051 microcontroller to the SLE 4520 PWM are transferred via the data bus P0 using the control signals ALE and $\overline{WR}$. In the PWM component three 8-bit registers for the three phases and two 4-bit registers for dead time and divider ratio respectively as well as an address decoder latch to buffer the relevant addresses are connected to the internal data bus of the SLE 4520 (**see Block Diagram**).

Addresses are as follows:

Address	Register
00	8-bit register for phase 1
01	8-bit register for phase 2
02	8-bit register for phase 3
03	dead time control register
04	divider control register

The last two registers have to be written only once when being initialized. In the case of a controller output the above-mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse-width modulator.

The required divider ratio for the production of low switching frequencies at a simultaneously high operating frequency of the microcontroller is set by the divider control register. The divider control register is best loaded with an adequate value in the starting routine.

Allocation of value and divider ratio is shown in **table 1**:

Table 1

Allocation of Value in the Divider Register to the Divider Ratio by which the SLE 4520 Operating Frequency is Selected

Value	Divider Ratio Counter	Divider Ratio Delay Clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

After the ratio has been determined, the length of the switching frequency cycle should be selected in such a way that the maximum pulse width is just reached. This means that with a PWM counter clock of, e.g. 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 µs (switching frequency cycle 128 µs).

Table 2 gives a number of useful allocations of counter frequency and switching frequency for the SAB 8051 (12-MHz clock).

Table 2

Allocation of Counter Frequency and Switching Frequency of SAB 8051

Divider Ratio	Counter Frequency	Operating Time Timer 0	Switching Frequency	Resolution
1:6	2 MHz	64 µs	15.6 kHz	7 bit
1:6	2 MHz	128 µs	7.8 kHz	8 bit
1:12	1 MHz	128 µs	7.8 kHz	7 bit
1:12	1 MHz	256 µs	3.9 kHz	8 bit
1:24	500 kHz	256 µs	3.9 kHz	7 bit
1:24	500 kHz	2 × 256 µs	1.95 kHz	8 bit
1:48	250 kHz	2 × 256 µs	1.95 kHz	7 bit
1:48	250 kHz	4 × 256 µs	975 Hz	8 bit

Converting a Data Word into a Pulse Width

Pulse generation in the three processing channels is done by a presettable 8-bit down-counter and a zero detector (NOR gate) which is connected to the eight counter outputs. With the transfer pulse from the microcontroller (width 1 instruction cycle), whose repetition rate determines the length of the switching frequency, the presettable counter is loaded with the contents of the appropriate register and 0 appears at the zero detector's output (provided the register does not contain 00H).

This 0 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio serves as clock frequency for the PWM counter.

Dead-time Control Register and Dead-Time Setting in Order to Avoid Overlapping Switching Operations

The dead time between the drive pulses for the two transistors of a half-bridge must consider the storage times of the bipolar driver and the power transistors, otherwise dangerous overlapping switching operations might occur. In the pulse-width modulator the dead time is obtained by linking the pulse-width modulated signal source with a delay signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs.

The shift pulse is either $f_{CRYSTAL}/6$ or $f_{CRYSTAL}/4$, depending on the values in the divider control register.

By writing a value between 0 and $0F_H$ into the appropriate control register 16 dead times are presettable (incl. zero dead time).

The dead time depends on the crystal frequency and the preset divider ratio. Programmable dead times for a 12-MHz crystal frequency are shown in **table 3**.

Table 3

Dead Times Presettable in the Dead Time Control Register Using Divider Ratios of 1:4 and 1:6

Word in Dead Time Memory	Divider Ratio 1:4 Dead Time (µs)	Divider Ratio 1:6 Dead Time (µs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

10

The Interface to the Power Circuit is Provided by Outputs PH1/1 to PH3/2

Without dead time PH1/2 is inverted to PH1/1, PH2/2 to PH2/1 and PH3/2 to PH3/1. The active switching state is low.

With a programmed dead time the negative edges of the output signal are shifted to the right by the dead time.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive block and power circuit with a current up to 20 mA.

Static or Dynamic Interlocking of Outputs is Possible

Within the duration of the inhibit signal (pin 19) all six outputs can be set to high level. In case the outputs are connected to optocouplers the light emitting diodes are currentless and all six individual transistors of the power circuit are blocked. This option is particularly necessary when switching on the drive block, as proper pulses at the pulse-width modulator output are only available after the oscillator output has been built up and the initialization routine has been executed.

As the SAB 8051 sets the port outputs to high when switched on, only one port pin of the microcontroller has to be connected to inhibit. At the end of the initialization routine this port pin is set to low.

Another way of inhibiting the outputs (hold function) is to apply a high pulse to the "Set" input (pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (pin 20) and can be used to indicate or inform the microcontroller (active high; used, for example, in the event of power failure, short circuit, overtemperature etc.).

The status flipflop is cleared by a high pulse at the "Clear Status" input (pin 21).

Features

- Generation of three pairs of pulse-width modulated rectangular pulses (phase angle between one phase and the next is, for example, 120 °) to drive six individual transistors of an inverter power block.
- Programmable dead time to reliably drive both power switches of a half-bridge from 0 to $15 \times \frac{6}{f_{crystal}}$ or $15 \times \frac{4}{f_{crystal}}$ in 15 steps.

  It is the negative edge which is in each case delayed because the output signal is active low.
- Programmable divider in the pulse-width modulator to obtain low switching frequencies (for output stages with thyristors, GTOs, and bipolar transistors) and to simultaneously operate the microcontroller at higher crystal frequencies.
- Direct drive of an optocoupler interface to isolate control and load circuits (I_{sink} = 20 mA maximum).
- All six outputs of the SLE 4520 are set to high level either dynamically by an inhibit signal (INHIBIT) or statically by an R-S flipflop (SET STATUS). Thus blocking of all six individual transistors of the power circuit is possible.
- DC braking by selecting different, fixed duty cycles in the three output pairs.
- Direction of rotation is software-reversed by changing between two phases.
- Sine-wave frequency range about 0 to > 2600 Hz.
- Switching frequency range < 1 to > 20 kHz.

  8-bit resolution of the desired sine-wave function with a switching frequency of $\frac{f_{crystal}}{6 \times 2^8}$ or 7 bits with a switching frequency of $\frac{f_{crystal}}{6 \times 2^7}$ ($f_{crystal}$ = 12 MHz and resolution = 7 bits result in a 15.6-kHz switching frequency).
- Smallest increment of the pulse-width is 333 ns with $f_{crystal}$ = 12 MHz and divider ratio 1:4.
- Changing the switching frequency cycle in 1-µs steps allows the transition from one sine-wave frequency stage to the next quasi continuously (virtually analog).
- Evaluating the bit pattern at one port of the microcontroller enables many (256) different speed-control programs to be selected.
- Low current consumption of the pulse-width modulator due to ACMOS technology.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	– 0.3		6	V
Input voltage	V_I	– 0.3		V_{DD} + 0.3	V
Storage temperature	T_{stg}	– 50		125	°C
Total power dissipation Power dissipation per output	P_{tot} P_Q			500 50	mW mW

Operating Range

Supply voltage Supply current (outputs not connected)	V_{CC} I_{DD}	4.5	5	5.5 15	V mA
Operating frequency	f_{CLK}			12	MHz
Ambient temperature	T_A	– 40		85	°C

DC Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
All Input Signals Except XTAL2						
H-input voltage	V_{IH}	2.2		V_{DD}	V	
L-input voltage	V_{IL}	0		0.8	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Input Signal XTAL2 for External Clock						
H-input voltage	V_{IH}	4.0			V	
L-input voltage	V_{IL}	0		0.3	V	
Input capacitance	C_I			10	pF	
Input current	I_{IL}			1	µA	
Output Signals STATUS, CLK OUT						
H-output voltage	V_{QH}	V_{DD} – 0.8			V	I_Q = 0.5 mA
L-output voltage	V_{QL}			0.4	V	I_Q = 1.6 mA
Output Signals PH 1/1, PH 1/2, PH 2/2, PH 3/1, PH 3/2						
L-output voltage	V_{QL}			1	V	I_Q = 20 mA
H-output voltage	V_{QH}	V_{DD} – 0.8 V			V	I_Q = 1 mA

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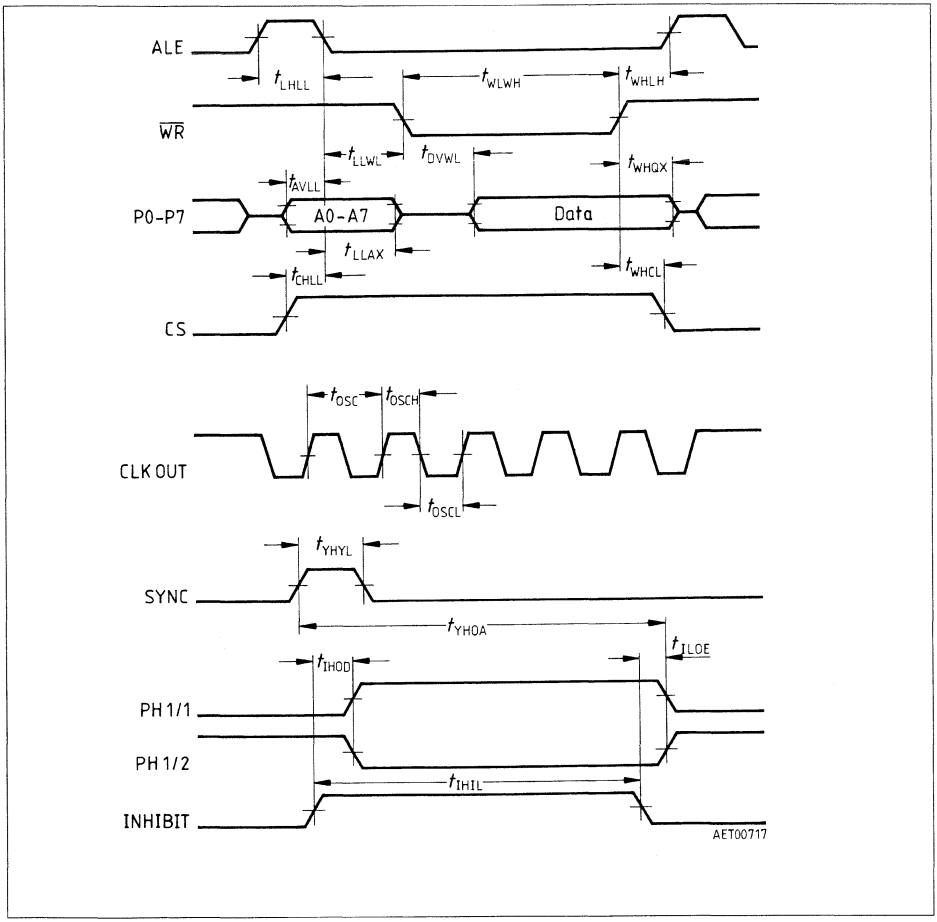
AC Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LHLL}	100		ns
Address setup to ALE	t_{AVLL}	30		ns
Address hold after ALE	t_{LLAX}	30		ns
WRN pulse width	t_{WLWH}	200		ns
WRN high to ALE high	t_{WHLH}	50		ns
Data setup after WRN low	t_{DVWL}		20	ns
ALE low to WRN low	t_{LLWL}	100		ns
Data hold after WRN [1]	t_{WHQX}	30		ns
Oscillator period	t_{OSC}	83		ns
High time	t_{OSCH}	35		ns
Low time	t_{OSCL}	35		ns
SYNC pulse width	t_{YHYL}	200		ns
INHIBIT low to output enable	t_{ILOE}		100	ns
Delay between SYNC high to output active	t_{YHOA}	4 t_{OSC}	97 t_{OSC} + 20	ns
Chip select setup to ALE low	t_{CHLL}	20		ns
Chip select hold after WRN high	t_{WHCL}	30		ns
Reset pulse width	t_{RHRL}	12 t_{OSC}		ns
Set status pulse width	t_{SHSL}	200		ns
Clear status pulse width	t_{CHCL}	200		ns
INHIBIT high to output disable	t_{IHOD}		100	ns
Set status high to output disable	t_{SHOD}		100	ns
Clear status high to output enable	t_{CHOD}		100	ns
Set status pulse length	t_{SHTH}	100		ns
Clear status pulse length	t_{CHTL}	100		ns
Inhibit pulse length	t_{IHIL}	100		ns

[1] If t_{WLWH} is less than 2 t_{OSC} + 20 ns, then t_{WHQX} is 50 ns



Pulse Diagrams

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Selector Guide

Type	Max. Current (A)	Operating Range V_S (V)	Max. Voltage V_S (V)	Error monitoring Overload, open circuit Short circuit to ground Overvoltage Overtemperature	Typ. saturation voltage at I_{max} (V) / Resistance	Temperature Range (°C)	Package	Page
TLE 4220	1 x 4	6.5 - 18	65	●	0.8	– 40 ... 110	P-TO220-7-1	685
TLE 4224	1 x 4	5.5 - 4.5	60	●	0.25 Ω	– 40 ... 110	P-TO220-7-1	697
TLE 4214	2 x 0.5	6 - 25	70	●	0.6	– 40 ... 125	P-DIP-8	707
TLE 4214 G							P-DSO-20-1	707
TLE 4215	2 x 0.5	5 - 25	70	●	1.2	– 40 ... 125	P-DIP-16	719
TLE 4211	2 x 2	5 - 20	70	●	0.6	– 40 ... 125	P-TO220-7-1	729
TLE 5224 G	2 x 4	5.5 - 45	60	●	2 x 0.25 Ω	– 40 ... 85	P-DSO-24-1	739
TLE 4216	2 x 0.5 +	5.2 - 30	40	overload +	2 x 0.5	– 40 ... 110	P-DIP-20-1	748
TLE 4216 G	4 x 0.05			overtemp.	4 x 0.4		P-DSO-24-1	748
TLE 4226 G	2 x 0.5 +	5.2 - 30	40	overload +	2 x 0.5	– 40 ... 110	P-DSO-24-1	759
	4 x 0.05			overtemp.	4 x 0.4			759

= SMD

SIEMENS

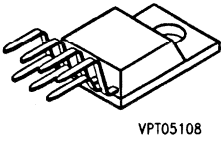
Intelligent 4-A Low-Side Switch

TLE 4220

Bipolar IC

Features

- Single low-side switch, 4 A
- Power limitation
- Overtemperature shutdown
- Reverse polarity protection
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-diodes
- Temperature range – 40 to 110 °C



P-TO220-7-1

Type	Ordering Code	Package
S ▼ TLE 4220	Q67000-A9010	P-TO220-7-1

▼ New type

TLE 4220 is an integrated low-side power switch with reverse-polarity protection, power limitation, temperature monitoring, error signaling via a status output and an integrated Z-diode for output clamping. TLE 4220 is designed for automotive applications.

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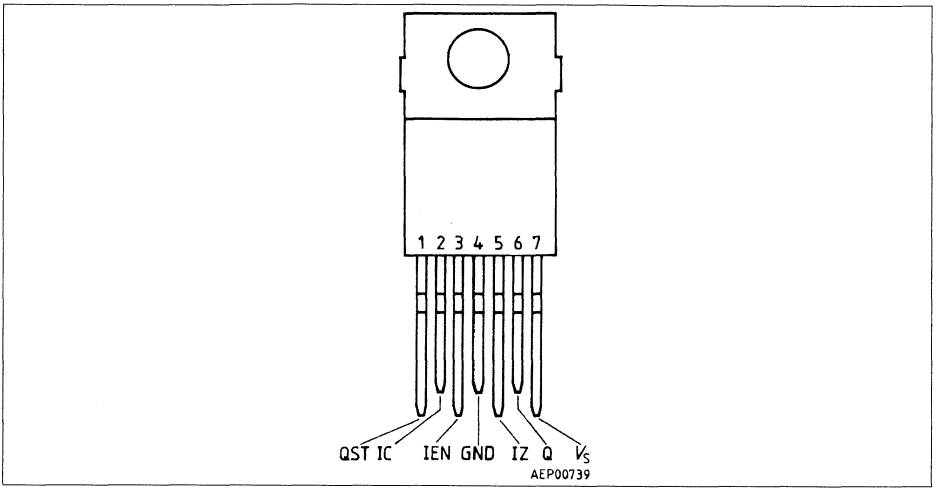
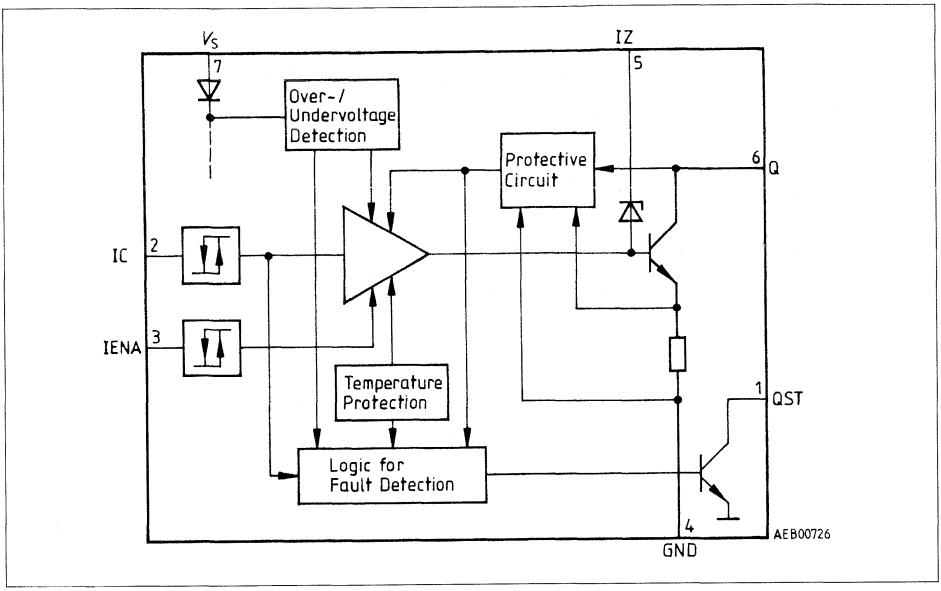


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	QST	**Status output** (open collector) for status monitoring; shorted load-protected to $V_{ST} \leq 6.25$ V
2	IC	**Control input,** active high.
3	IENA	**Enable input,** active high.
4	GND	**Ground,** connected internally to cooling lug.
5	IZ	**Clamp-diode;** if this pin is not connected to pin 6, appropriate provisions have to be taken for protecting the power output against the discharging EMF when inductive loads are turned off.
6	Q	**Power output** (open collector) for inductive loads; shorted-load protected.
7	V_S	**Supply voltage;** if there is overvoltage on this pin, the major part of the circuitry is deactivated.



Block Diagram

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). An integrated clamp diode limits the discharging EMF when pin 5 is connected to pin 6. It is also possible to implement this limitation through external measures (clamp diode, Z-diode). For the detection of errors there is a status output, which monitors the following errors by logic level:

- Overvoltage or undervoltage on supply,
- Overvoltage in the load circuit,
- Open and shorted load to ground in active and inactive mode,
- Overloading of output (also shorted load to supply) in active mode.

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Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of Schmitt triggers with hysteresis. The control signal activates the buffer amplifier for the output stage when there is high potential on the enable input.

Switching Stages

The power output consist of a NPN power transistor with open collector. A protective circuit for limiting power dissipation makes the output stage shorted-load-protected throughout the operating range. The integrated clamp-diode can be connected externally to the output and in this way limits voltage spikes produced when inductive loads are discharged.

Protective Circuits

At supply voltages that are above or below the operating range, the output stage is turned off independently of the input signals. An integrated diode protects against reverse poling of the supply voltage within the operating voltage. The load circuit withstands reverse poling within the bounds of the maximum ratings (no shorted load permissible at the same time). There is temperature protection to guard the IC against thermal overload.

Error Detection

The status output signals overvoltage or undervoltage on supply as well as overtemperature and, with the enable input activated, errors on the output (overload, underload, overvoltage) by the logic connectives given in the table

Supply Voltage	Control Input	Output State	Status Output
Overvoltage	X	X	H
Undervoltage	X	X	H
Operating range	L	No error	L
Operating range	H	No error	H
Operating range	L	Error or overtemperature	H
Operating range	H	Error or overtemperature	L

x = random

Because of the internal propagation delays, the correct status information is monitored with a delay of up to 50 µs. Therefore a corresponding wait interval is necessary before precise evaluation of the status signal can commerce.

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 45	45	V	–
Supply voltage	V_S	–	65	V	$t \leq 500$ ms
Output voltage	V_Q	–	45	V	–
Output voltage	V_Q	–	70	V	$t \leq 500$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	V_I	– 45	45	V	–
Input voltage	V_F	– 45	45	V	–
Currents					
Clamp diode current	I_Z	– 1	1	mA	pin 5 not connected to pin 6
Output current	I_Q	limited internally; for driving via Z-diode only inductive off-commutating current is permissible			
Current on reverse poling	I_Q; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 1	–	mA	–
Output current, status pin	I_{ST}	–	1	mA	$V_{ST} \geq 6.25$ V
Discharging energy for inductive load	E	–	200	mJ	–
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	6.5	18	V	–
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs	–
Input voltages	V_I, V_F	– 5	40	V	–
Output voltage	V_{ST}	–	40	V	–
Output current	I_{ST}	0	1	mA	–
Ambient temperature	T_A	– 40	110	°C	$T_j \leq 150$ °C
Thermal shutdown	–	150	–	°C	165 °C typical
Thermal resistance Junction to case Junction to ambient	 $R_{th\ JC}$ $R_{th\ JA}$	 – –	 3 65	 KW KW	 – –

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Characteristics
V_S = 6.5 to 18 V (typ. 12 V)
T_A = – 40 to 110 °C; $T_j \leq$ 150 °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Control Input						
H-input voltage	V_{IH}	–	–	2.0	V	–
L-input voltage	V_{IL}	1.0	–	–	V	–
Hysteresis	ΔV_I	–	0.5	–	V	–
H-input current	I_{IH}	0	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	0	–	10	µA	V_I = 0.5 V
Enable Input						
H-input voltage	V_{FH}	–	–	2.4	V	–
L-input voltage	V_{FL}	1.6	–	–	V	–
Hysteresis	ΔV_F	–	0.4	–	V	–
H-input current	I_{FH}	0	–	10	µA	V_F = 5 V
L-input current	$-I_{FL}$	0	–	10	µA	V_F = 0.5 V
Status Output						
L-voltage level	V_{ST}	–	–	0.5	V	I_{ST} = 1 mA; V_D variable
L-voltage level	V_{ST}	–	–	0.3	V	I_{ST} = 125 µA; V_D variable
Leakage current	I_{ST}	–	–	2	µA	V_S = 0 V
Delay time	t_{ST}	–	–	50	µs	–
Output Stages						
Saturation voltage	V_{QSat}	–	–	1.25	V	I_Q = 4 A; $T_j \leq$ 125 °C
Saturation voltage	V_{QSat}	–	–	1.25	V	I_Q = 3 A **see Diagram**
Overload current	I_{QL}	–	–	–	–	**see SOA Diagram**
Leakage current	I_{QR}	–	–	100	µA	$V_I < V_{IL}$; V_S = 6 V
Turn-ON time	t_{dON}	–	–	5	µs	**see Timing**
Turn-OFF time	t_{dOFF}	–	–	10	µs	**Diagram;** I_Q = 2 A
Output voltage negative clamp	$-V_{QF}$	–	–	2	V	I_Q = – 4 A
Clamp Diode						
Clamp voltage	V_Z	26	–	34	V	I_Z = 0.1 A; $V_Z = V_Q$
Serial resistance	r_Z	–	–	1	Ω	0A < I_Q < 4A; V_Z =

Characteristics (cont'd)
V_S = 6.5 to 18 V (typ. 12 V)
T_C = – 40 to 110 °C; $T_j \leq$ 150 °C (typ. 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	–	10	mA	$V_I < V_{IL}$ or $V_F < V_{FL}$
Supply current	I_S	–	100	180	mA	$V_I > V_{IH}$ and $V_F > V_{FH}$
Overvoltage shutdown threshold (supply)	V_{Sov}	18	–	28	V	$V_I < V_{IL}$; $V_{ST} > 5$ V
Overvoltage shutdown threshold (output)	V_{Qov}	34	–	44	V	$V_I < V_{IL}$; $V_{ST} > 5$ V
Differential voltage	ΔV_{QZ}	4	–	–	V	$V_{Qov} - V_Z$
Open load current	I_{Qu}	–	–	450	mA	$V_I > V_{IH}$; $V_F > V_{FH}$; $V_{ST} < 0.5$ V
Open load shutdown voltage threshold	V_{Qu}	–	2.4	–	V	$V_I < V_{IL}$; $V_F > V_{FH}$; $V_{ST} > 5$ V
Overload shutdown voltage threshold	V_{QL}	1.5	–	2.5	V	$V_I > V_{IH}$; $V_F > V_{FH}$; $V_{ST} < 0.5$ V

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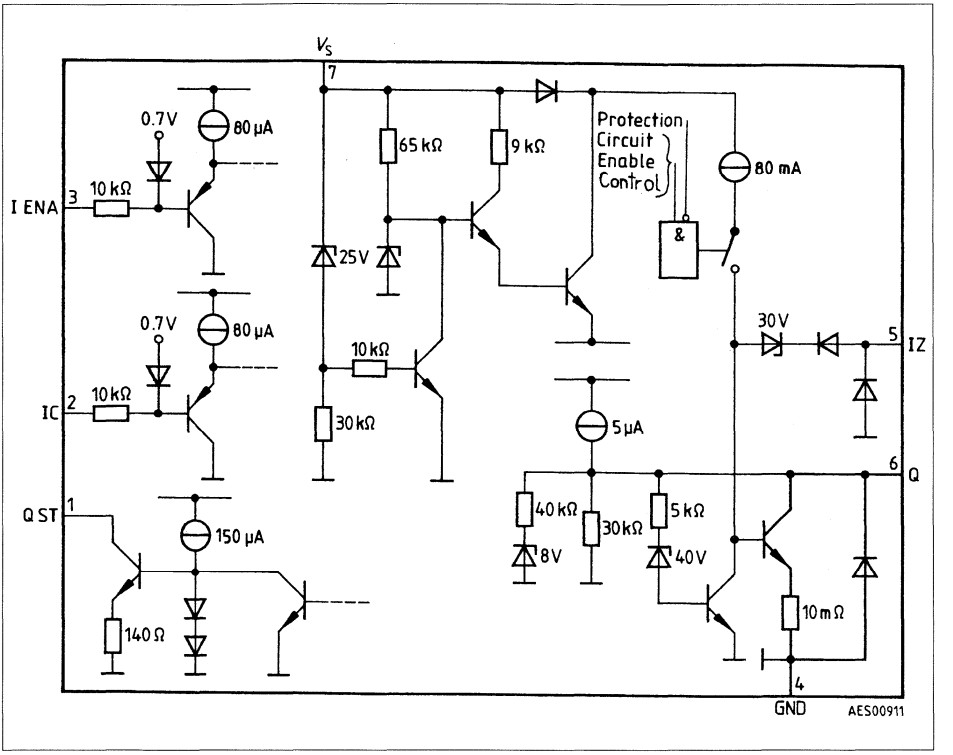
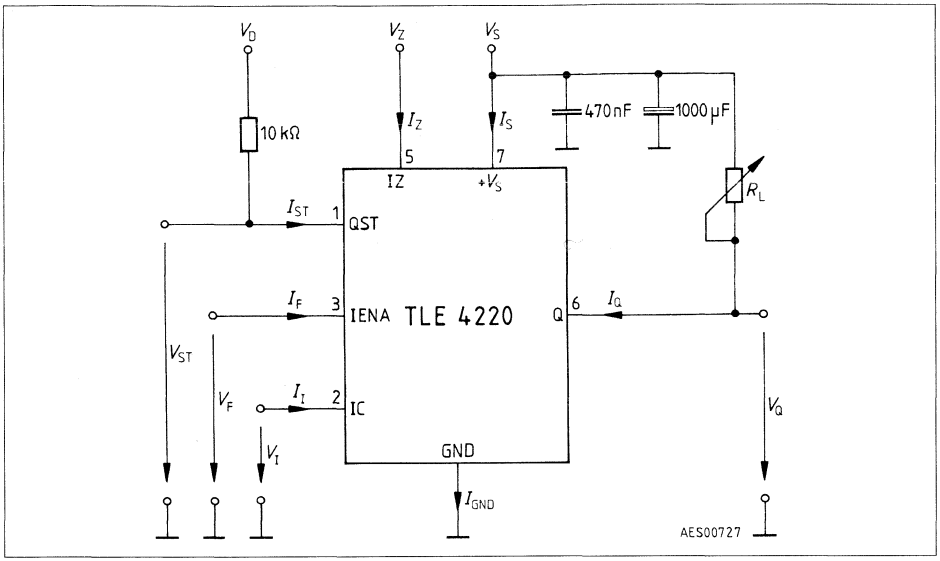
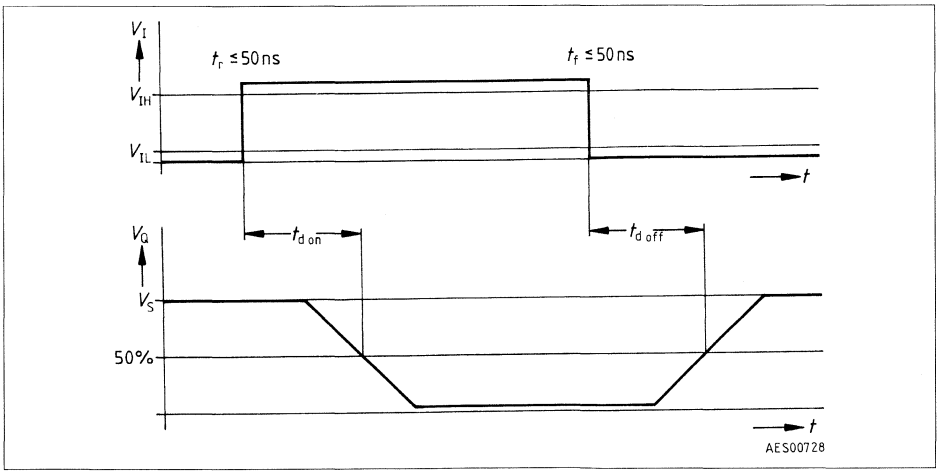


Circuit Diagram



Test Circuit



Timing Diagram

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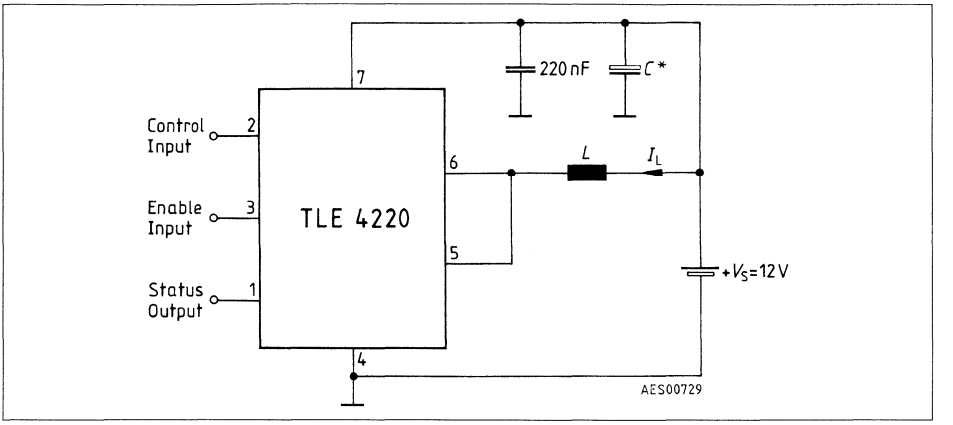
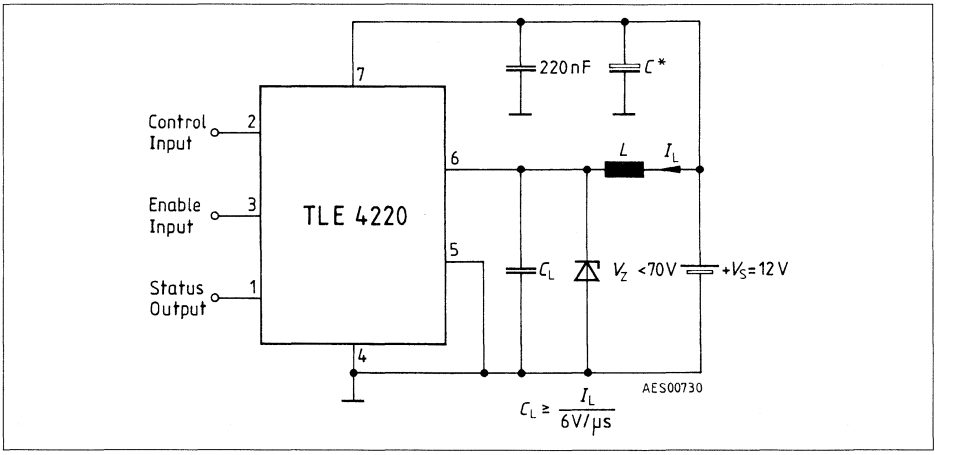


Application Circuit 1

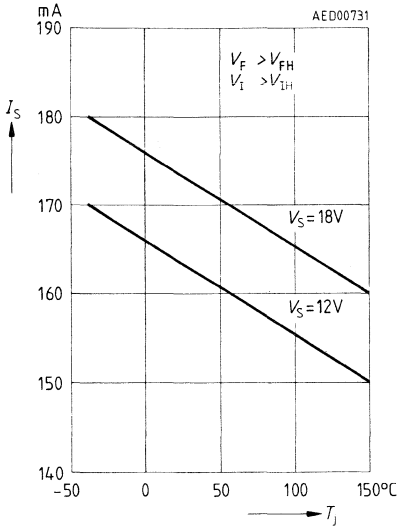


Application Circuit 2

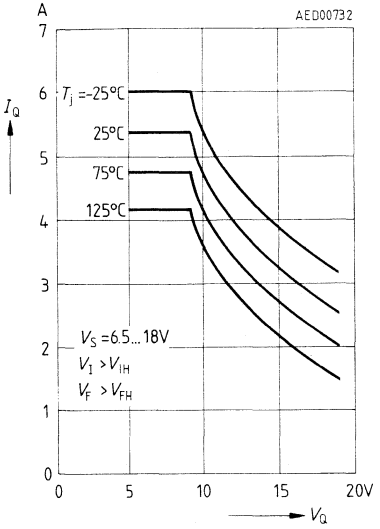
The blocking capacitor C^* is to be rated large enough so that the maximum ratings of the IC for negative supply voltage are not exceeded during the off-commutating operation in interruption of the battery voltage.

Diagrams

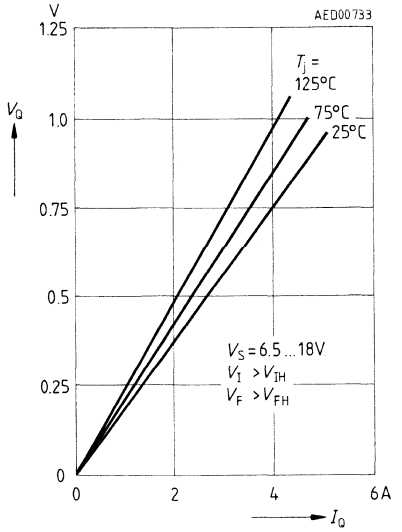
Max. Quiescent Current I_S versus Junction Temp. T_j in Active State



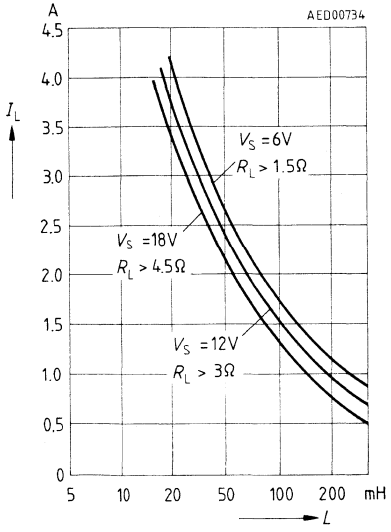
Shorted-Load Current I_Q versus Output Voltage V_Q



Typical Output Voltage V_Q versus Output Current I_Q



Maximum Load Current I_L versus Load Inductance L



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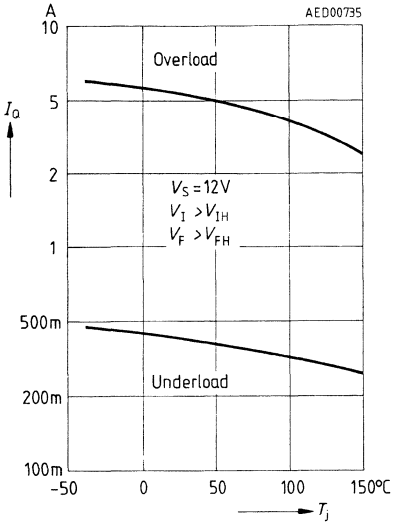
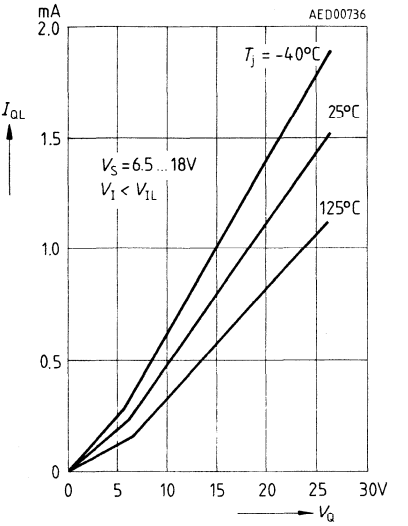
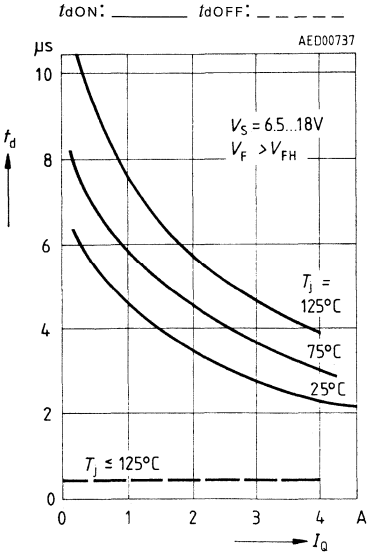
Response Threshold of Status Signal versus Junction Temperature T_j



Typical Output Leakage Current I_{QL} versus Output Voltage V_Q



Typical Delay Times versus Output Current I_Q



Intelligent 4-A Low-Side Switch

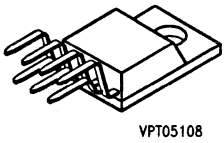
TLE 4224

Preliminary Data

SPT-IC

Features

- Single low-side switch, 4 A
- Low-ON-resistance (typ. 0.25 Ω)
- Power limitation
- Overtemperature shutdown
- Overload shutdown
- Reverse polarity protection
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-diodes
- Temperature range – 40 to 110 °C



P-TO220-7-1

Type	Ordering Code	Package
▼ TLE 4224	Q67000-A9062	P-TO220-7-1

▼ New type

TLE 4224 is an integrated low-side power switch with reverse-polarity protection, load interrupt and shorted-load detection, temperature monitoring, error signaling via a status output and an integrated Z-diode for output clamping. TLE 4224 is designed for automotive applications.

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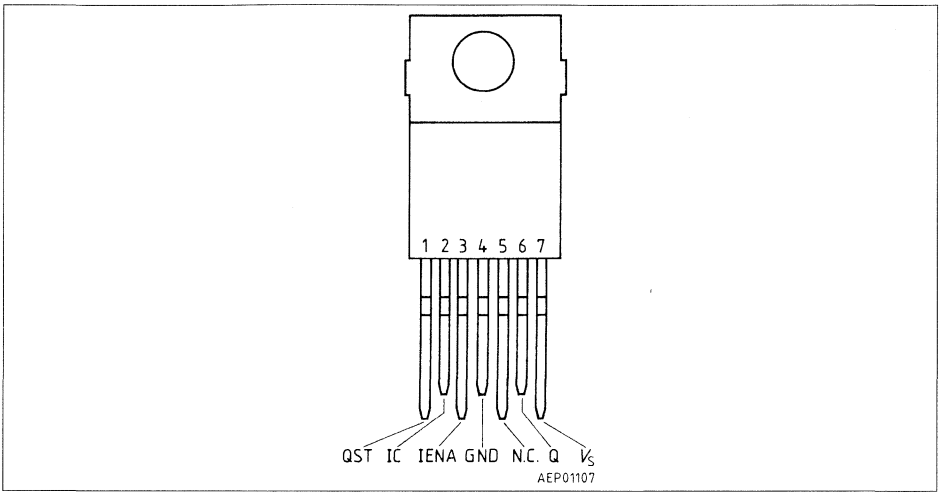
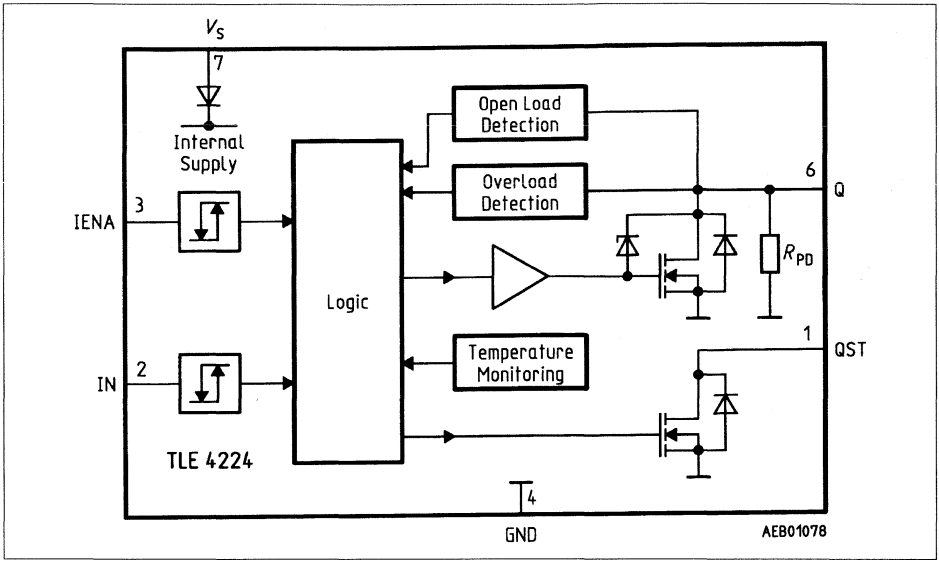


Pin Configuration

Pin Definitions and Functions

Pin	Symbol	Function
1	QST	**Status output** (open collector) for error monitoring; shorted load-protected to $V_{ST} \leq 6.25$ V
2	IN	**Control input,** active high.
3	IENA	**Enable input,** active high.
4	GND	**Ground,** connected internally to cooling lug.
5	N.C.	Not connected
6	Q	**Power output** (open drain) for inductive loads;shortedload protected.
7	V_S	**Supply voltage;** if there is overvoltage on this pin, the major part of the circuitry is shutdown.



Block Diagram

Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). An integrated clamp diode limits output voltage when inductive loads are discharged. For the detection of errors there is a status output, which monitors the following errors by logic level:

- Thermal overload,
- Open and shorted load to ground in active and inactive mode,
- Overload (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, both active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Unconnected inputs are interpreted as "low".

Switching Stages

The power output consists of a DMOS power transistor with open drain. The output stage is shorted-load-protected throughout the operating range. The integrated clamp-diode limits voltage spikes produced when inductive loads are discharged.

Protective Circuits

An integrated diode protects against reverse poling of the supply voltage within the operating range. The load circuit withstands reverse poling within the bounds of the maximum ratings (no shorted load permissible at the same time). A temperature protection guards the IC against thermal overload.

Error Detection

The status output signals the status of the switching stage at normal operation. (Low = OFF; high = ON). In case of any error the status output is set according to the table on the next page.

If current overload occurs, the error condition is stored in an internal register and the output is shut down. To reset this register the control input has to be switched off and then on again.

The status of the error detection circuit is directly dependent of the input state.

Status Monitoring

Operating Condition	Enable Input	Control Input	Power Output	Status Output
Normal Operation	LOW	LOW	OFF	LOW
	LOW	HIGH	OFF	LOW
	HIGH	LOW	OFF	LOW
	HIGH	HIGH	ON	HIGH
Thermal Overload	RANDOM	LOW	OFF	HIGH
	RANDOM	HIGH	OFF	LOW
Open Load or Shorted Load to Ground	LOW	LOW	OFF	HIGH
	LOW	HIGH	OFF	HIGH
	HIGH	LOW	OFF	HIGH
	HIGH	HIGH	ON	LOW
Overload or Shorted Load to V_S	LOW	LOW	OFF	HIGH
	LOW	HIGH	OFF	HIGH
	HIGH	LOW	OFF	HIGH
	HIGH	HIGH	OFF	LOW

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Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 15	60	V	–
Output voltage	V_Q	–	45	V	
Output voltage	V_Q	–	60	V	$t \leq 500$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	$V_{I,F}$	– 1.5	6	V	–
Currents					
Output current	I_Q	5	–	A	limited internally
Current on reverse poling	I_Q; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 5	5	mA	–
Discharging energy for inductive load	E	–	50	mJ	–
Junction temperature Junction temperature	T_j T_j	– 40	150 175	°C °C	 during clamping
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	5.5	45	V	–
Supply voltage slew rate	dV_S/dt	– 1	1	V/µs	–
Output voltage	V_Q V_Q	– 0.3 –	45 60	V V	– during clamping
Output voltage	V_{ST}	– 0.3	45	V	–
Output current	I_{ST}	0	2	mA	–
Ambient temperature	T_A	– 40	125	°C	$T_j \leq 150$ °C
Thermal resistance junction to case junction to ambient	 $R_{th\,JC}$ $R_{th\,JA}$	 – –	 3 65	 K/W K/W	 – –

Characteristics
V_S = 6.5 to 18 V (typ. 12 V)
T_A = – 40 to 125 °C; $T_j \leq$ 150 °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	0.3	1	mA	Output OFF
Supply current	I_S	–	2	5	mA	Output ON
Open load current	I_{Qu}	–	–	250	mA	–
Open load shutdown voltage threshold	V_{Qu}	6	–	7.2	V	Output ON V_S = 12 V
Overload shutdown current threshold	I_{QAB}	5 4	– –	– –	A A	T_j = – 40 to 50 °C T_j = 50 to 150 °C
Overtemperature shutdown threshold	T_{AB}	145	–	175	°C	only a design value
Overtemperature shutdown hysteresis	ΔT_{AB}	–	10	–	°C	only a design value

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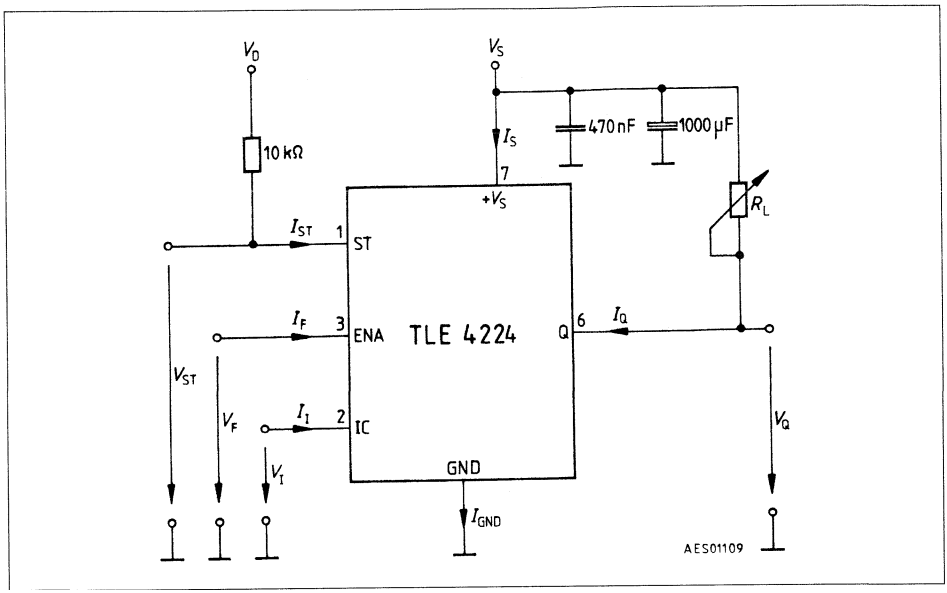
Characteristics

V_S = 6.5 to 18 V (typ. 12 V)
T_A = – 40 to 110 °C; $T_j \leq$ 150 °C (typ. 25 °C)
V_D = 5.1 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Control and Enable Input						
H-input voltage	V_{IH}	2.0	–	6.0	V	–
L-input voltage	V_{IL}	-0.3	–	1.0	V	–
Hysteresis	ΔV_I	0.2	–	–	V	–
H-input current	I_{IH}	50	100	140	µA	V_I = 5 V;
H-input current	I_{FH}	5	15	20	µA	V_F = 5 V;
Status Output						
Low voltage level	V_{ST}	–	–	0.5	V	I_{ST} = 2 mA
Leakage current high	I_{ST}	–	–	2	µA	V_S = 0 V
Power Output						
Static drain source ON-resistance	R_{DSON}	–	0.25	–	Ω	$T_j \leq$ 25 °C
	R_{DSON}	–	–	0.5	Ω	T_j = 150 °C I_Q = 4A, $V_S \geq$ 9.5V
Pull-down Resistance	R_{PD}	14	20	26	k	T_j = 25 °C
Output ON delay time	t_1	–	25	–	µs	I_Q = 0.2A
Output ON fall time	t_2	–	20	–	µs	I_Q = 0.2A
Output OFF rise time	t_3	–	25	–	µs	I_Q = 2A
Output OFF status delay	t_4	–	30	–	µs	I_Q = 2A
Output ON status delay	t_5	–	–	50	µs	1)
Overload OFF delay time	t_{DSO}	50	–	150	µs	design value only
Clamp Diode						
Clamp diode clamping voltage	V_{QZ}	45	–	60	V	–

[1]) Time between status valid and switching on or error detection.



Test Circuit

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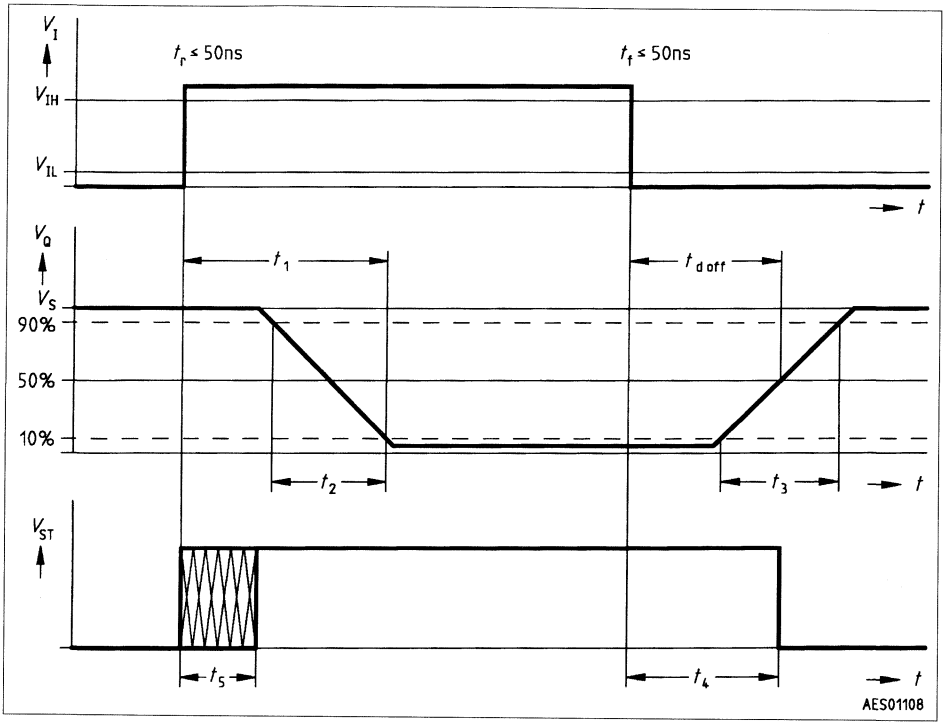
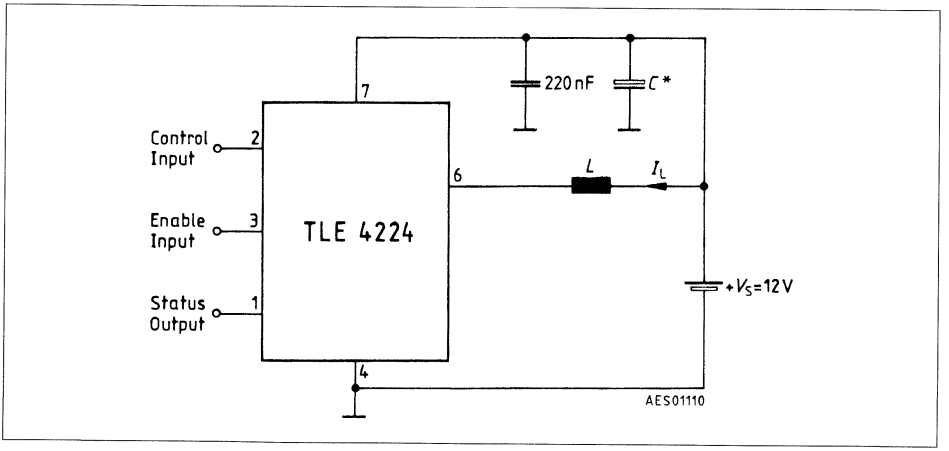


Timing Diagram



Application Circuit

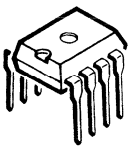
Intelligent Double Low-Side Switch 2 × 0.5 A

TLE 4214

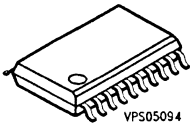
Bipolar IC

Features

- Double low-side switch, 2 × 0.5 A
- Power limitation
- Overtemperature shutdown
- Overvoltage shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp diodes
- Temperature range – 40 to 125 °C



P-DIP-8



P-DSO-20-1

Type	Ordering Code	Package
S TLE 4214	Q67000-A8183	P-DIP-8
S TLE 4214 G	Q67000-A9094	P-DSO-20-1 (SMD)

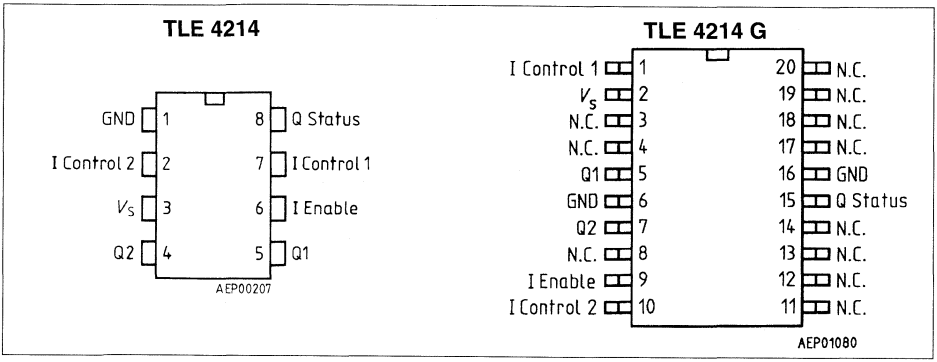
Application

Applications in automotive electronics require intelligent power switches activated by logic signals, which are also shorted-load protected and provide error feedback.

The IC contains two of these power switches (low-side switches). In case of inductive loads the integrated clamp diodes clamp the discharging voltage. If a "high" signal is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The high impedance inputs and must therefore not be left unconnected, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions through high potential:

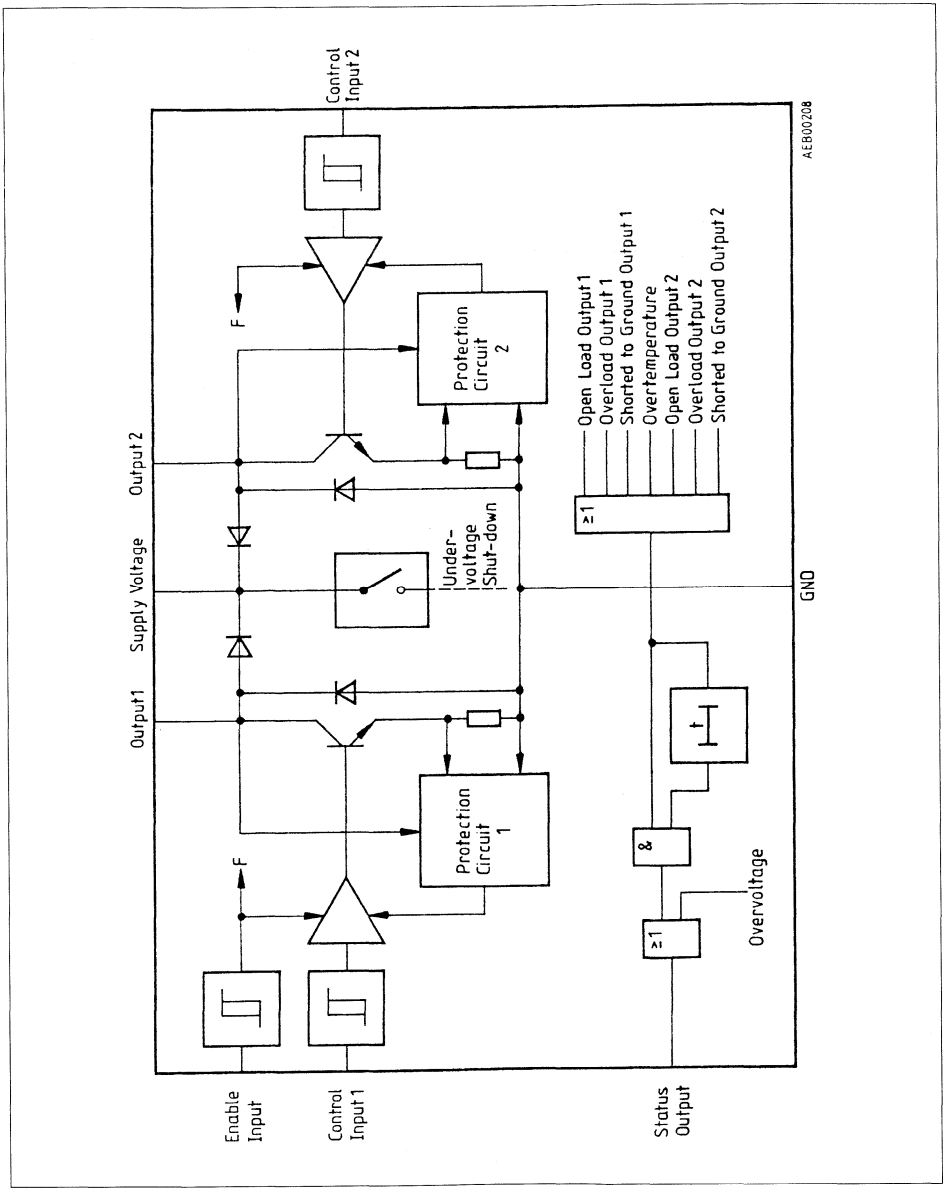
- Overload,
- Open load,
- Shorted load to ground,
- Overvoltage,
- Overtemperature.



Pin Configuration (top view)

Pin Definitions and Functions

TLE 4214 G Pin	TLE 4214 Pin	Symbol	Function
6, 16	1	GND	**Ground** Design wiring for the max. short-circuit current (2 × 1 A)
10	2	IN2	**Control input 2** (TTL compatible) activates the output transistor 2 in case of high potential
2	3	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates this malfunction without delay time.
7	4	Q2	**Output 2** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
5	5	Q1	**Output 1** Shorted load protected, open collector output for currents up to 0.5 A, with clamping diodes to supply voltage.
9	6	ENA	**Enable input**, active high
1	7	IN1	**Control input 1** (TTL compatible) activates output transistor 1 in case of high potential
15	8	STA	**Status output** (open collector) for both outputs; indicates overtemperature, overload, open load and shorted load to ground as well as overvoltage at pin 3. Is switched to high after a defined delay time in case of malfunction (except: overvoltage)
3, 4, 8, 11 ... 14, 17 ... 20		N. C.	Not connected



Block Diagram

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Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

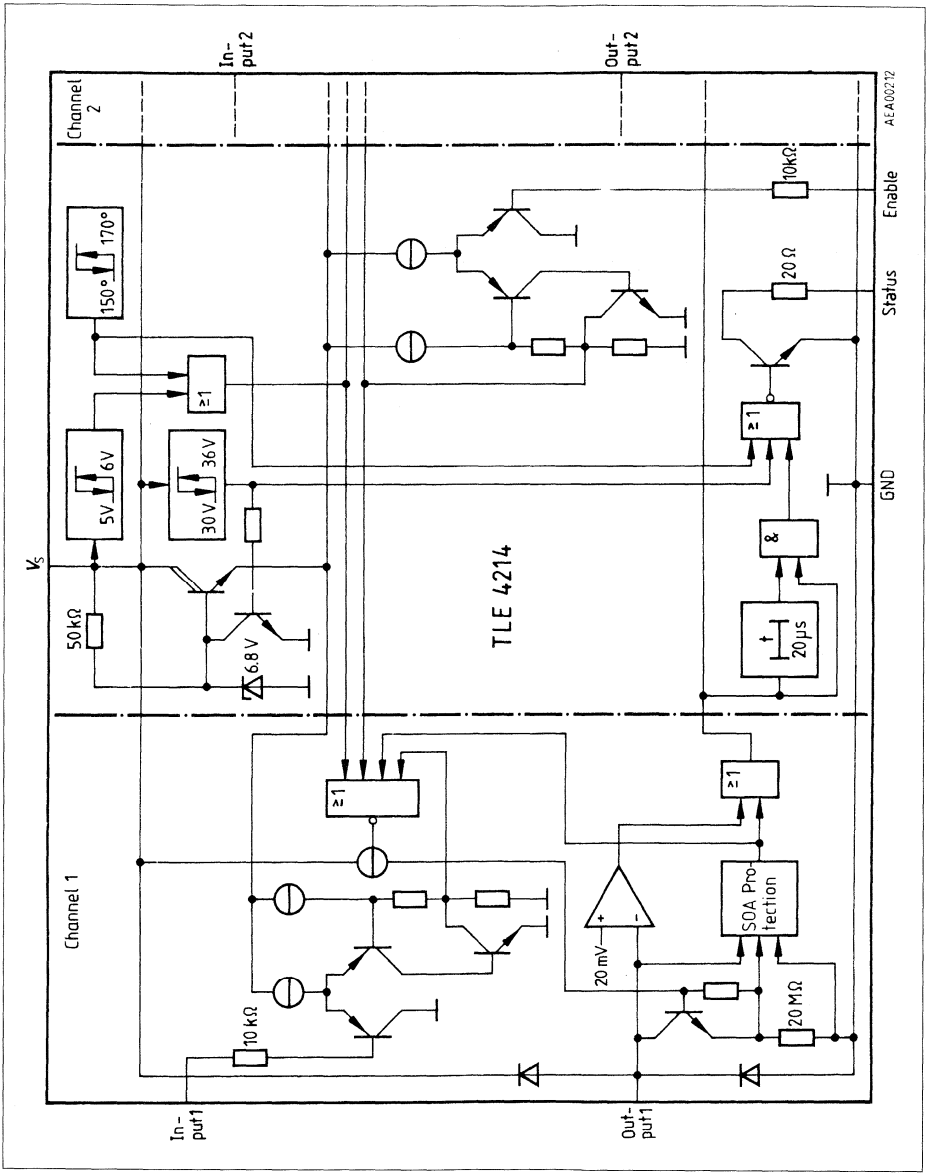
Switching Stages

The output stages consist of NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp diodes.

Monitoring and Protective Functions

During the activated status the outputs are monitored for open load, overload, and shorted load to ground (see table below). In addition, large sections of the circuit are shut down in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active high). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated. At supply voltages below the operating range the output stages are de-activated.

Status Output (H = Error)				
	Undervoltage > 3.5 V	**Operating Range** V_I = L (passive)	V_I = H (active)	**Overvoltage**
Normal function	L	L	L	H
Overload	L	L	H	H
Open load	L	L	H	H
Shorted load to ground	L	H	H	H
Overtemperature	L	H	H	H



Circuit Diagram

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage, t < 0.2 s	V_S	–	70	V
Supply voltage	V_S	– 1.3	40	V
Input voltage	V_I	– 13	40	V
Output voltage (status output)	V_O	– 0.3	40	V
Output voltage (switching stages)	V_Q	– 0.3	+ V_S	V
Currents				
Output current (switching stages)	I_Q	internally limited	–	–
Current with reverse polarity, t < 0.1 s	I_Q	– 0.7	–	A
Output current positive clamp	I_Q	–	0.7	A
Ground current	I_{GND}	– 1.4	2.0	A
Output current (status output)	I_O	–	10	mA
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	6 [1]	25	V
Supply voltage slew rate	dV_S/dt	–1	1	V/µs
Output current (switching stages)	I_Q	– 0.5	0.5	A
Input voltage	V_I, V_F	– 5	32	V
Output current (status output)	I_O	0	5	mA
Ambient temperature	T_A	– 40	125	°C
Supply voltage while shorted load	V_S	–	16	V
Thermal resistance junction to ambient TLE 4214	$R_{th\,JA}$	–	91	K/W
TLE 4214 G	$R_{th\,JA}$	–	77	K/W

[1] Lower limit = 5 V, if previously V_S greater than 6 V (turn-on hysteresis)

Characteristics

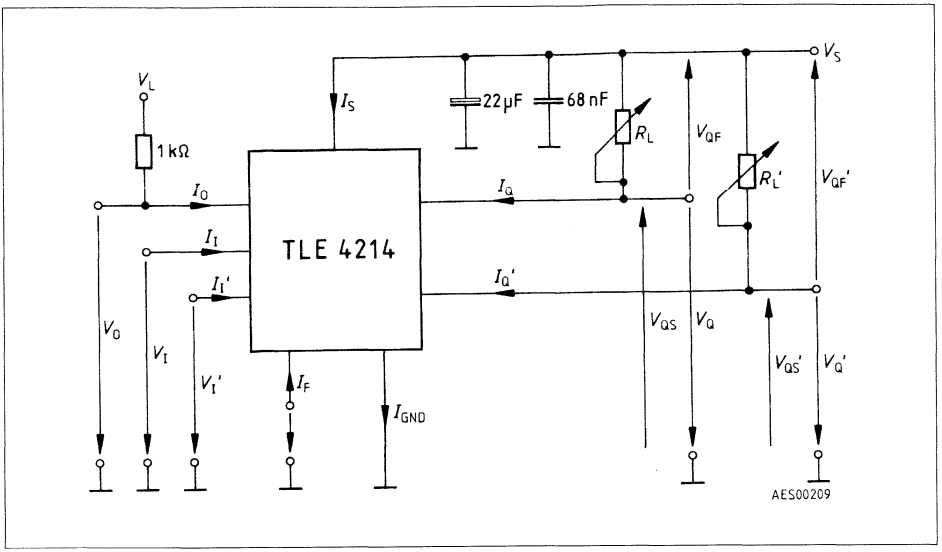
V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Characteristics						
Quiescent current	I_S	–	2	4	mA	$V_F < V_{FL}$
Supply current	I_S	–	35	50	mA	$V_I = V_I > V_{IH}$; $V_F > V_{FH}$
Supply overvoltage shutdown threshold	V_{SO}	30	36	40	V	V_L = 5 V; V_O > 4.5 V
Hysteresis of supply overvoltage shutdown threshold	ΔV_{SO}	4	6	9	V	V_L = 5 V; V_O > 4.5 V
Open load error threshold voltage	V_Q	5	20	50	mV	V_L = 5 V; V_O > 4.5 V
Open load error threshold current	I_{QU}	1	–	20	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	80	mA	$V_{Q1} = V_{Q2} = V_{QU}$
Logic						
Control inputs						
H-input voltage threshold	V_{IH}	1.3	1.8	2.1	V	–
L-input voltage threshold	V_{IL}	0.9	1.2	1.5	V	–
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	–
H-input voltage threshold	V_{FH}	1.6	2.1	2.7	V	–
L-input voltage threshold	V_{FL}	1.4	1.8	2.3	V	–
Hysteresis of input voltage	ΔV_F	0.1	0.3	0.7	V	–
H-input current	I_{IH}	0	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	0	–	10	µA	V_I = 0.5 V
Status Output (open collector)						
L-saturation voltage	V_{QSat}	0.1	0.2	0.4	V	I_O = 5 mA
Status delay time	t_{dS}	8	20	32	µs	[1]

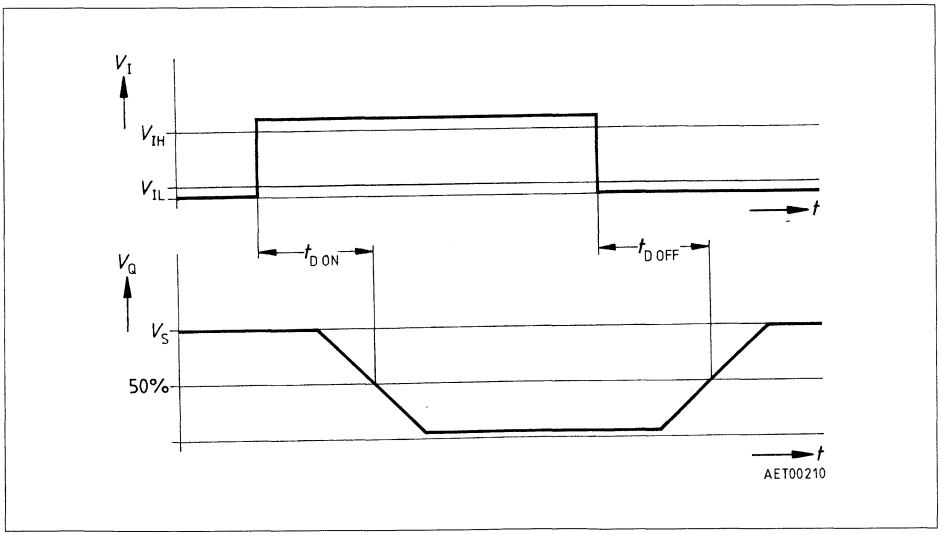
[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

Characteristics (cont'd)
V_S = 6 to 16 V (typ. V_S = 12 V); T_j = – 40 to 150 °C (typ. T_j = 25 °C)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switching Stages						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 0.5 A; $V_I > V_{IH}$; $V_F > V_{FH}$
Saturation voltage	V_{QSat}	–	45	100	mV	I_Q = 50 mA; $V_I > V_{IH}$; $V_F > V_{FH}$
Output current	I_Q	0.5	–		A	V_{QSat} = 0.8 V; $V_I > V_{IH}$
Leakage current	I_Q	– 5	–	50	µA	V_Q = 6 V; $V_I < V_{IL}$
Switch-ON time	$t_{D\,ON}$	0.2	0.5	5	µs	I_Q = 0.5 A **see Timing**
Switch-OFF time	$t_{D\,OFF}$	0.2	2	5	µs	I_Q = 0.5 A **Diagram**
Forward voltage of substrate diode	V_{QS}	–	1.3	1.7	V	I_Q = – 0.5 A t < 0.1 s
Forward voltage of clamp diode	V_{QF}	–	1.3	1.7	V	I_Q = 0.5 A t < 0.1 s
Leakage current of clamp diode	$-I_{QF}$	–	–	5	µA	V_Q = 0 V; $V_I < V_{IL}$



Test Circuit



Timing Diagram

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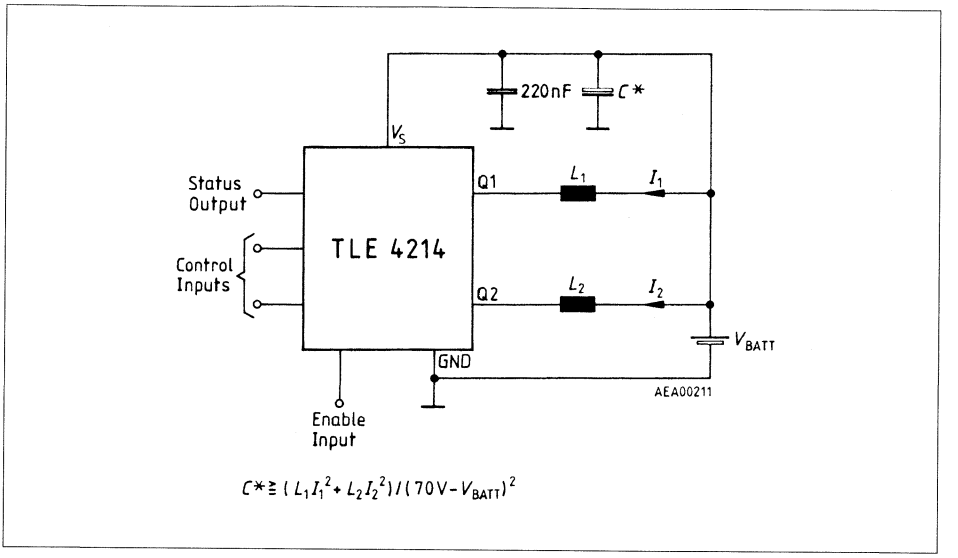
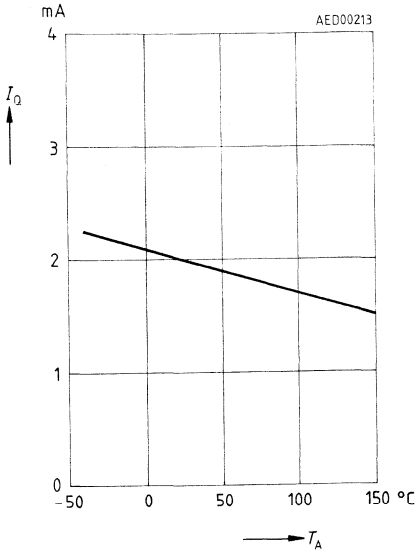
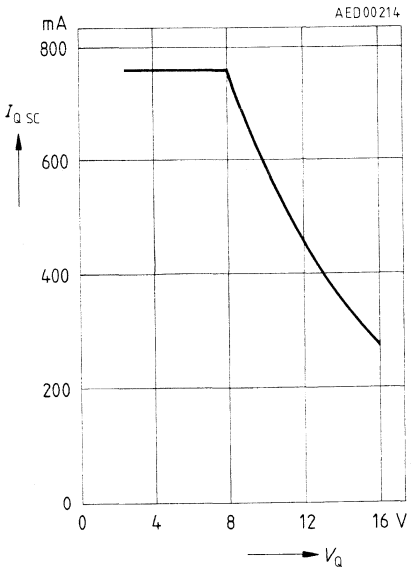


Application Circuit

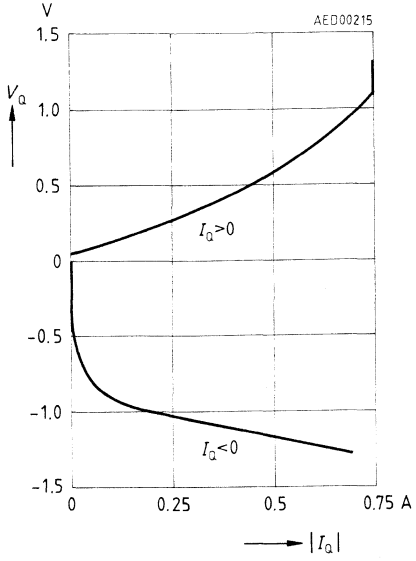
Quiescent Current I_S versus Ambient Temperature T_A in the OFF-Status
V_S = 12 V; $V_F < V_{FL}$



Shorted Load Current I_{Q0} versus Output Voltage V_Q



Output Voltage V_Q versus Output Current V_S = 12 V; $V_I > V_{IH}$



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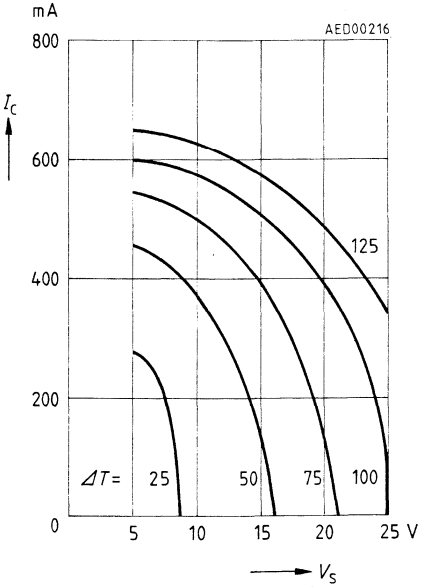
Maximum permissible output currents, being the result of the typical thermal power dissipation in a **P-DIP-8** package, for three operating modes.

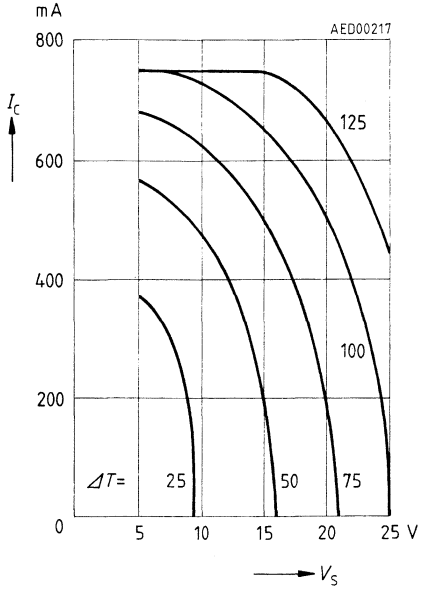
ΔT: Difference between junction and ambient temperature ($T_j - T_A$) [K].

I_Q: Max. output current (steady current) per channel.

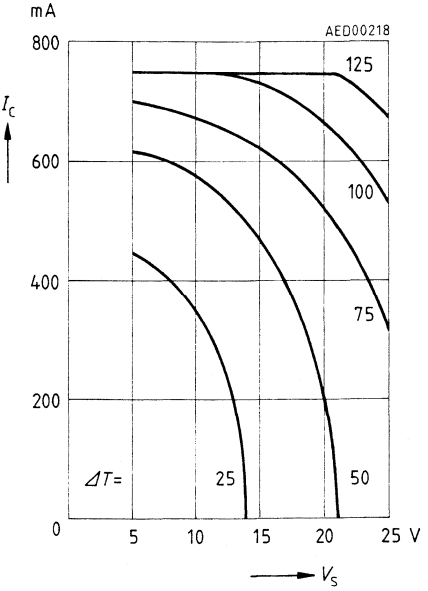
Equal Current at Both Channels



First Channel 50 mA, Second Channel I_Q



Only One Channel in Operation



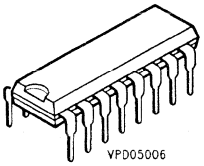
Intelligent Double High-Side Switch 2 × 0.5 A

TLE 4215

Bipolar IC

Features

- Double high-side switch, 2 × 0.5 A
- Power limitation
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp diodes
- Temperature range – 40 to 125 °C



P-DIP-16

Type	Ordering Code	Package
S TLE 4215	Q67000-A8184	P-DIP-16

Applications

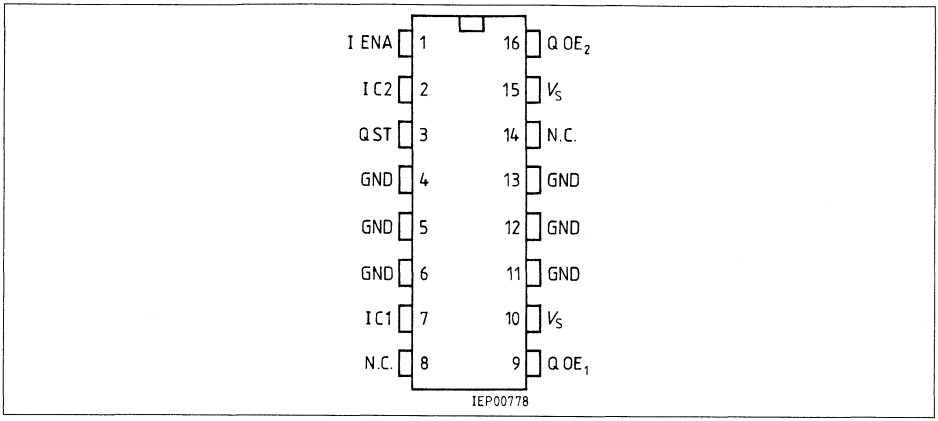
Applications in automotive electronics require intelligent power switches activated by logic signals which are shorted-load protected and provide error feedback.

The IC contains two of these power switches (high-side switches). In case of inductive loads the integrated clamp diodes clamp the discharging voltage.

If a "high" signal is applied to the enable input both switches can be activated independently of one another through TTL signals at the control inputs (active high). The inputs are highly resistive and must therefore not be left unconnected, but should always be connected to a fixed potential (noise immunity).

The status output (open collector) signals the following malfunctions with high potential:

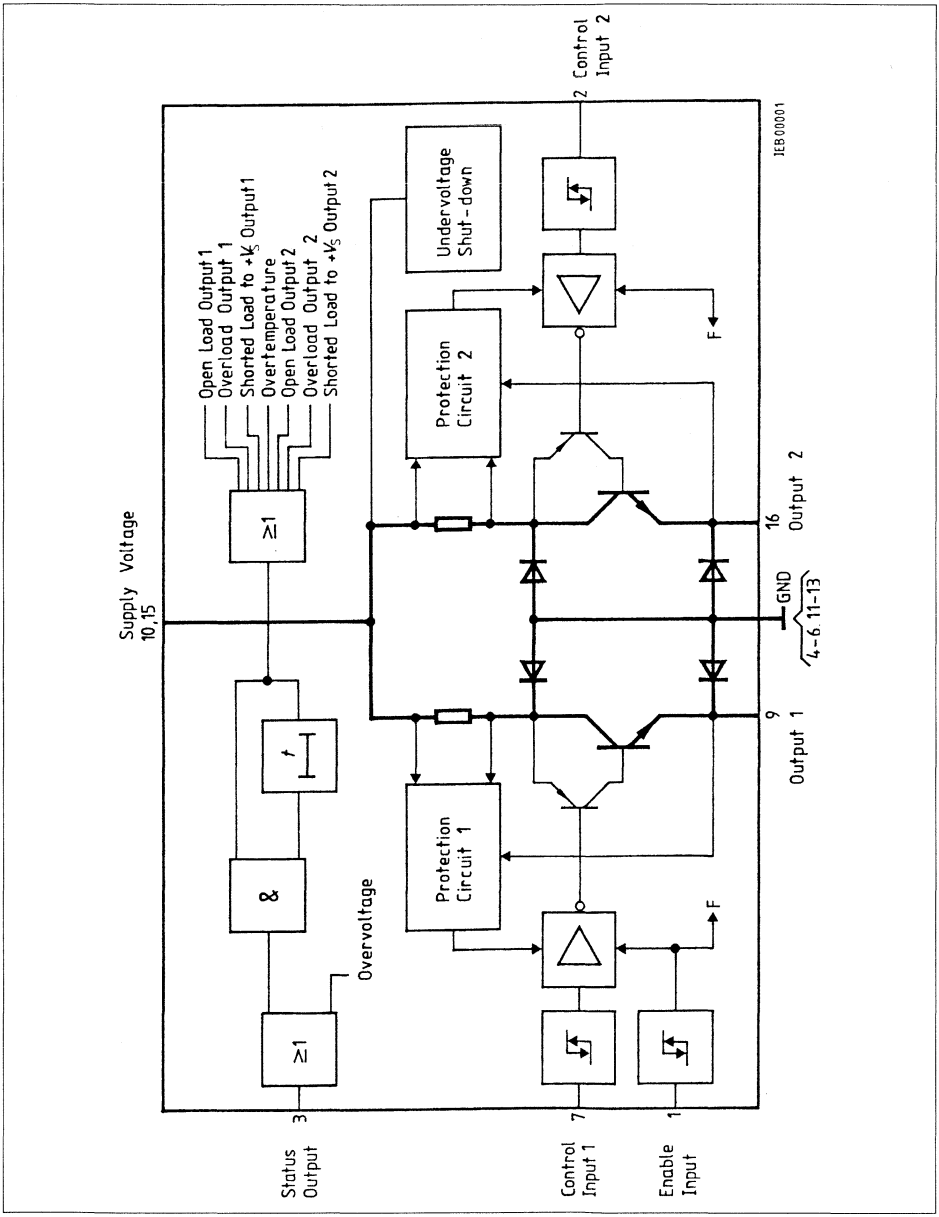
- Overload,
- Open load,
- Short-load to ground and supply,
- Overvoltage,
- Overtemperature.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	ENA	**Enable input,** active high
2	IN2	**Control input 2** activates output transistor 2 (active high)
3	ST	**Status output** (open collector) for both outputs; monitors overtemperature, overload, open load, shorted load and supply overvoltage on pin 10 or 15; is switched off after a delay time in the event of a malfunction (exception: overvoltage).
4, 5, 6, 11, 12, 13	GND	**Ground**
7	IN1	**Control input 1** activates output transistor 1 (active high)
8	N.C.	Not connected
9	Q1	**Output 1,** shorted-load protected open emitter with negative clamp diode
10	V_S	**Supply voltage;** large parts of the circuit are deactivated if overvoltage appears on this pin; the status output will signal this malfunction without a delay time
14	N.C.	Not connected
15	V_S	**Supply voltage,** connected internally to pin 10; both pins should be put on + V_S
16	Q2	**Output 2,** shorted-load protected open emitter with negative clamp diode



Block Diagram

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Circuit Description

Input Circuits

The control inputs and the enable input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with an open emitter. Each stage has its own protective circuit for limiting power dissipation, which makes the outputs shorted-load protected to ground throughout the operating range. Integrated clamp diodes limit the discharging voltage of inductive loads.

Monitoring and Protective Functions

If the supply voltage V_S is too high or there is overtemperature, several parts of the circuit are shut down. Each output is monitored for open load and overload while activated. Furthermore, any shorting to the supply voltage is detected. The ORed information from these malfunctions are flagged on the status output (open collector, active high). An internally defined delay time for all malfunctions, except for overvoltage, prevents short-term faults from being signalled.

If the minimal supply voltage for a function is not maintained, the output stages become inactive.

Status Output (H = Error)

	Undervoltage	**Operating Range**		**Overvoltage**
	> 3.5 V	V_I = L (passive)	V_I = H (active)	
Normal function	L	L	L	H
Overload	L	L	H	H
Open load	L	L	H	H
Shorted load to +V_S	L	H	H	H
Overtemperature	L	H	H	H

Absolute Maximum Ratings

T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage (pin 10, 15)	V_S	–	60	V	t < 0.2 s
Supply voltage (pin 10, 15)	V_S	– 0.3	42	V	–
Input voltage (pin 1, 2, 7)	V_{IN}	– 32	42	V	–
Output voltage (pin 3)	V_O	– 0.3	42	V	–
Output voltage (pin 9, 16)	V_Q	– 0.3	+ V_S	V	–
Currents					
Output current (pin 9, 16)	I_Q	–	–	–	limited internally
Output clamp neg. current	I_Q	–	0.7	A	t < 0.1 s
Ground current (pin 4-6, 11-13)	I_{GND}	– 1.4	0.05	A	–
Output current (pin 3)	I_Q	–	10	mA	–
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	6 [1]	25	V	$T_j \leq 150$ °C
		–	16	V	for shorted load
Supply voltage slew rate	dV_S/dt	–1	1	V/µs	–
Output current	I_Q	–	500	mA	–
Input voltages	V_{IN}	– 10	40	V	–
Output current (pin 3)	I_O	0	5	mA	–
Ambient temperature	T_A	– 40	125	°C	$T_j \leq 150$ °C
Thermal Resistance					
Junction to ambient	$R_{th\,JA}$	–	60	K/W	–
Junction to case	$R_{th\,JC}$	–	15	K/W	–

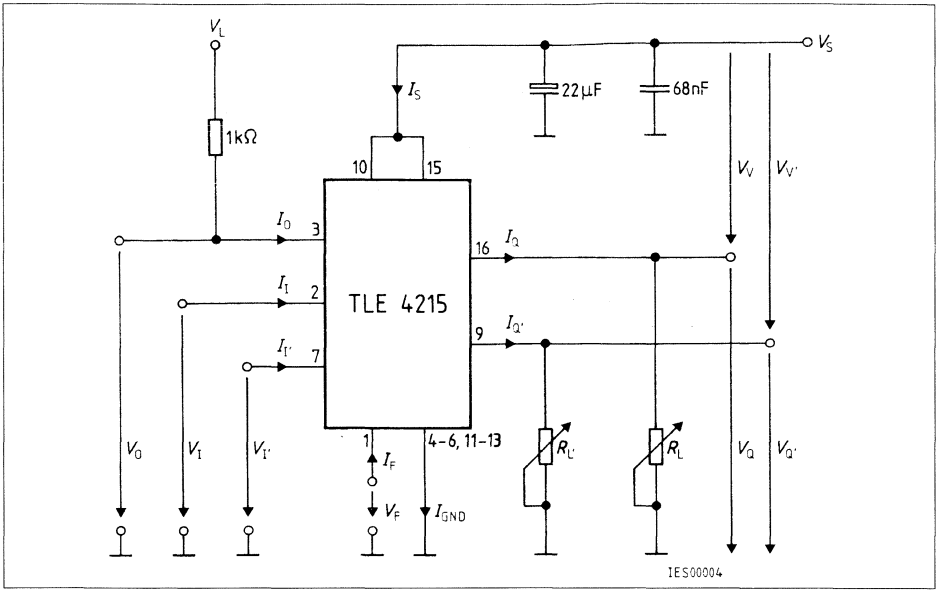
[1] Lower limit = 5.2 V if previously V_S was greater than 6 V (turn-on hysteresis)

Characteristics

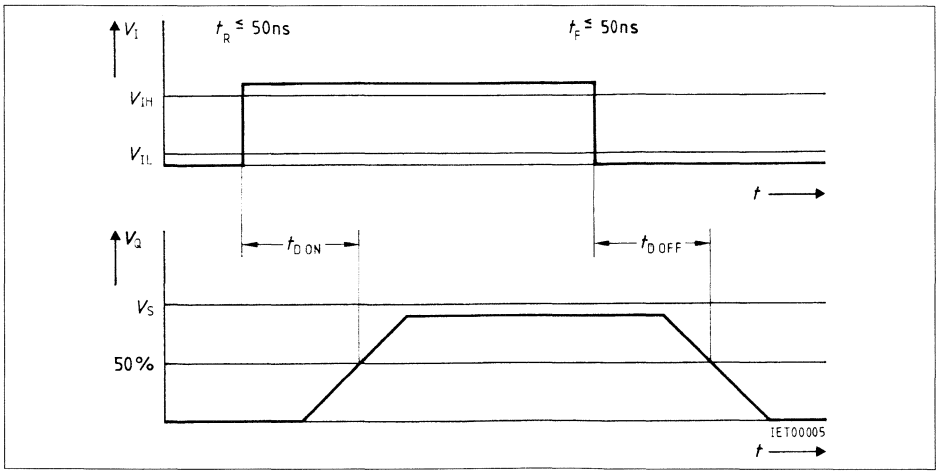
V_S = 6 to 16 V; T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General Data						
Quiescent current	I_S	–	2	5	mA	$V_E < V_{EL}$
Supply current	I_S	–	10	20	mA	$V_I = V_I > V_{IH}$; $V_E > V_{EH}$
Supply overvoltage shutdown threshold	V_{Sov}	30	36	40	V	V_L = 5 V; V_O > 4.5 V
Hysteresis of overvoltage shutdown	ΔV_{Sov}	3	6	9	V	V_L = 5 V; V_O > 4.5 V
Open load voltage switching threshold	V_{Qu}	–	200	800	mV	V_L = 5 V; V_O > 4.5 V
Open load current threshold	I_{Qu}	0.5		5	mA	$V_Q = V_{Qu}$
Logic						
Control inputs						
H-switching threshold	V_{IH}	1.2	1.8	2.2	V	pin 2, 7
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	pin 2, 7
Hysteresis of input voltage	ΔV_I	0.2	0.6	1.0	V	pin 2, 7
H-switching threshold	V_{FH}	1.7	2.1	2.8	V	pin 1
L-switching threshold	V_{FL}	1.4	1.8	2.3	V	pin 1
Hysteresis of input voltage	ΔV_F	0.1	0.3	0.7	V	pin 1
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V; pin 1, 2, 7
L-input current	$-I_{IL}$	–	–	10	µA	V_I = 0.5 V; pin 1, 2, 7
Status Output (open collector)						
L-saturation voltage	V_{OSat}	0.1	0.2	0.4	V	I_O = 5 mA
Status delay time	t_{DS}	8	25	40	µs	[1]
Switching Stages						
L-saturation voltage	V_{Lsat}	0.9	1.2	1.5	V	I_O = 0.5 A; $V_I > V_{IH}$; $V_E > V_{EH}$
Leakage current	I_{QL}	–	–	75	µA	$V_I < V_{IL}$; V_S = 6V; V_Q=0 V
Turn-ON time	t_{DON}	0.2	0.5	5	µs	**see Timing**
Turn-OFF time	t_{DOFF}	0.2	1	5	µs	**Diagram;** I_Q = 0.5 A
Output voltage negative clamp	$-V_Q$	0.8	1.3	1.7	V	I_Q = 0.5 A; t < 0.1 s

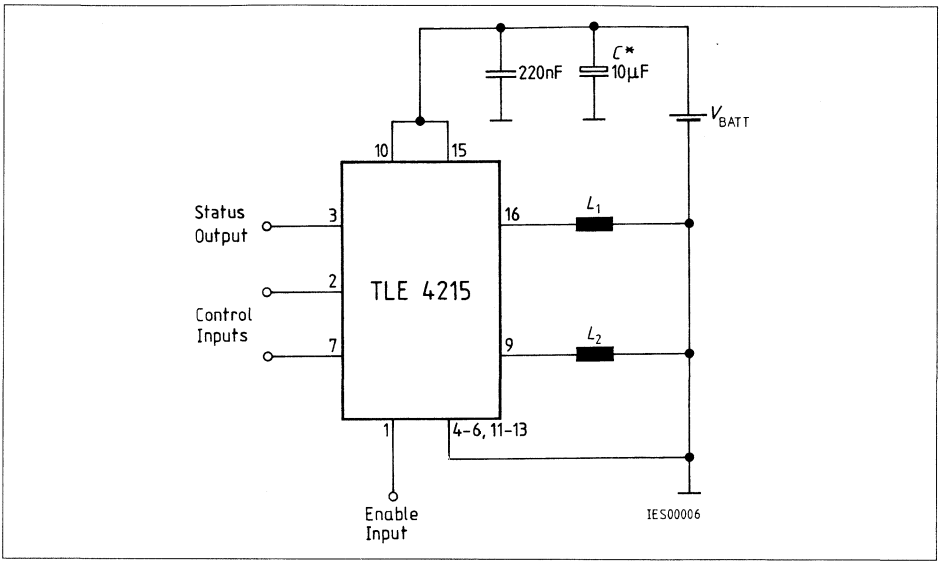
[1] Time from beginning of malfunction on channel (exception: overvoltage) up to 50 % value of status switching edge



Test Circuit

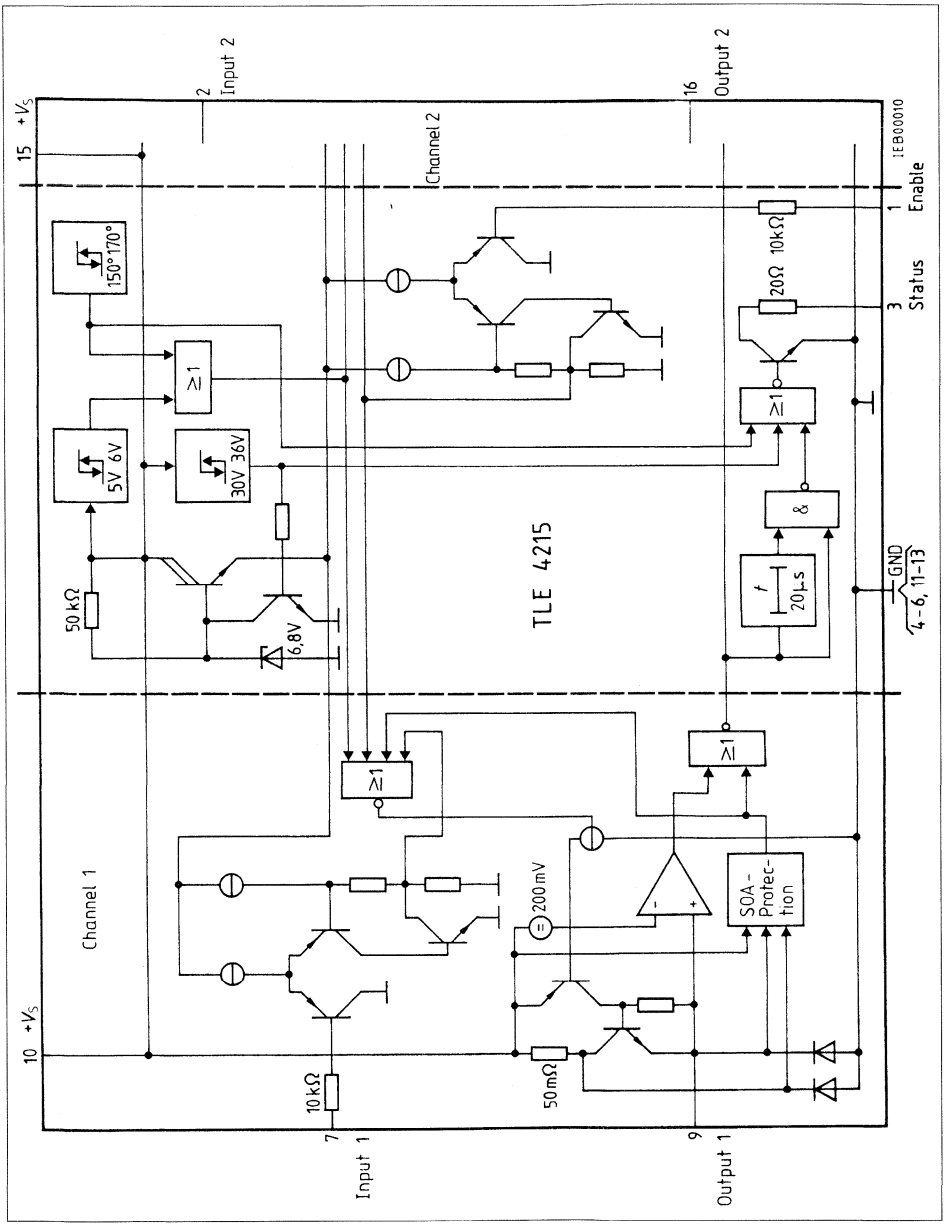


Timing Diagram



Application Circuit

C^* is to be dimensioned such that in case of an incoming-line failure the maximum ratings are not exceeded by the recirculation energy of L_1, L_2.



Circuit Diagram

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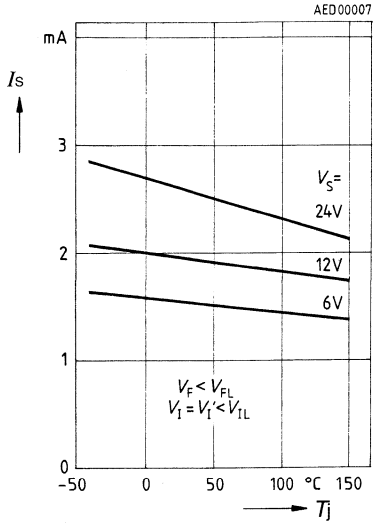
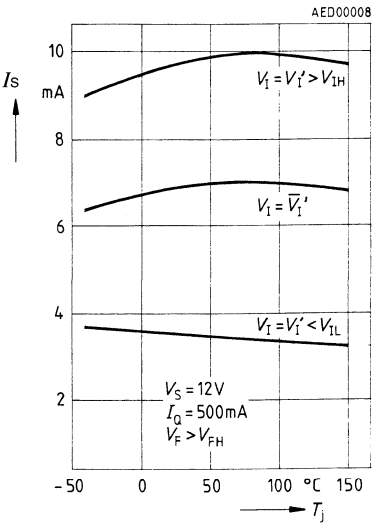
Diagrams

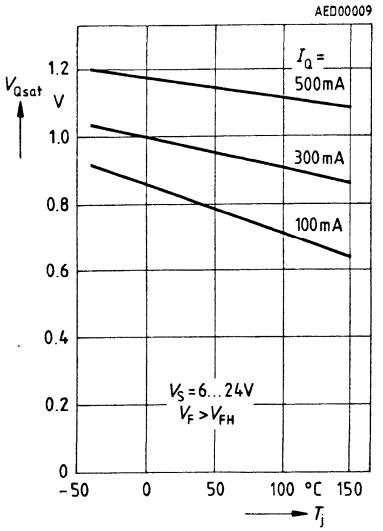
Typ. Quiescent Current I_S versus T_j in the OFF-State



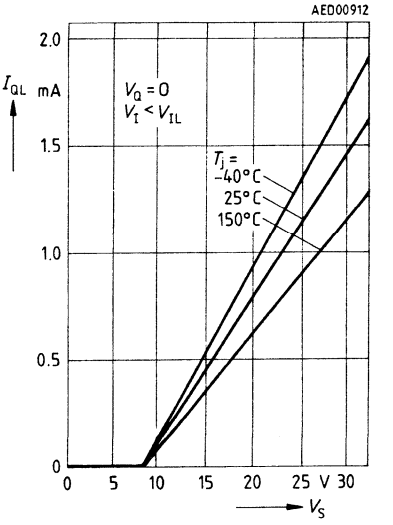
Typ. Supply Current I_{GND} versus Chip Temperature T_j in ON-State



Typ. Output Saturation Voltage V_{Qsat} versus Chip Temperature T_j



Typ. Output Leakage Current I_{QL} versus Supply Voltage V_S



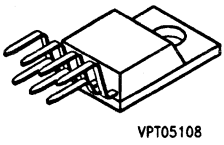
Intelligent Double Low-Side Switch 2 × 2 A

TLE 4211

Bipolar IC

Features

- Double low-side switch, 2 × 2 A
- Power limitation
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Reverse polarity protection
- Integrated clamp Z-diodes
- Voltage proof up to 70 V
- Temperature range – 40 to 125 °C



P-TO220-7-1

Type	Ordering Code	Package
S TLE 4211	Q67000-A8118	P-TO220-7-1

Application

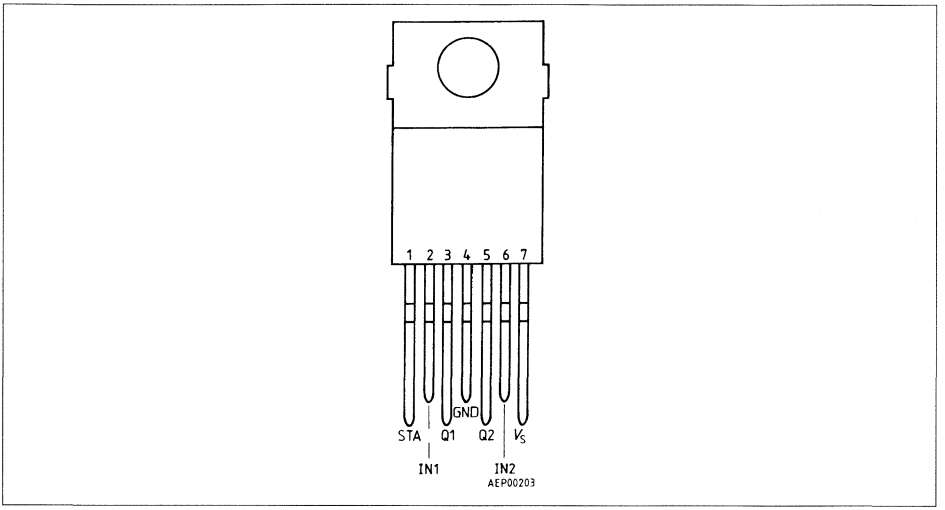
Applications in automotive electronics require intelligent power switches activated by logic signals, which are also shorted-load protected and provide error feedback.

The IC contains two of these power switches (low-side switch). In case of inductive loads the integrated power Z-diodes clamp the discharging voltage.

Through TTL signals at the control inputs (active low) both switches can be activated independently of one another. If one of the inputs is not in use, it must be applied to high potential.

The status output (open collector) signals the following malfunctions through low potential:

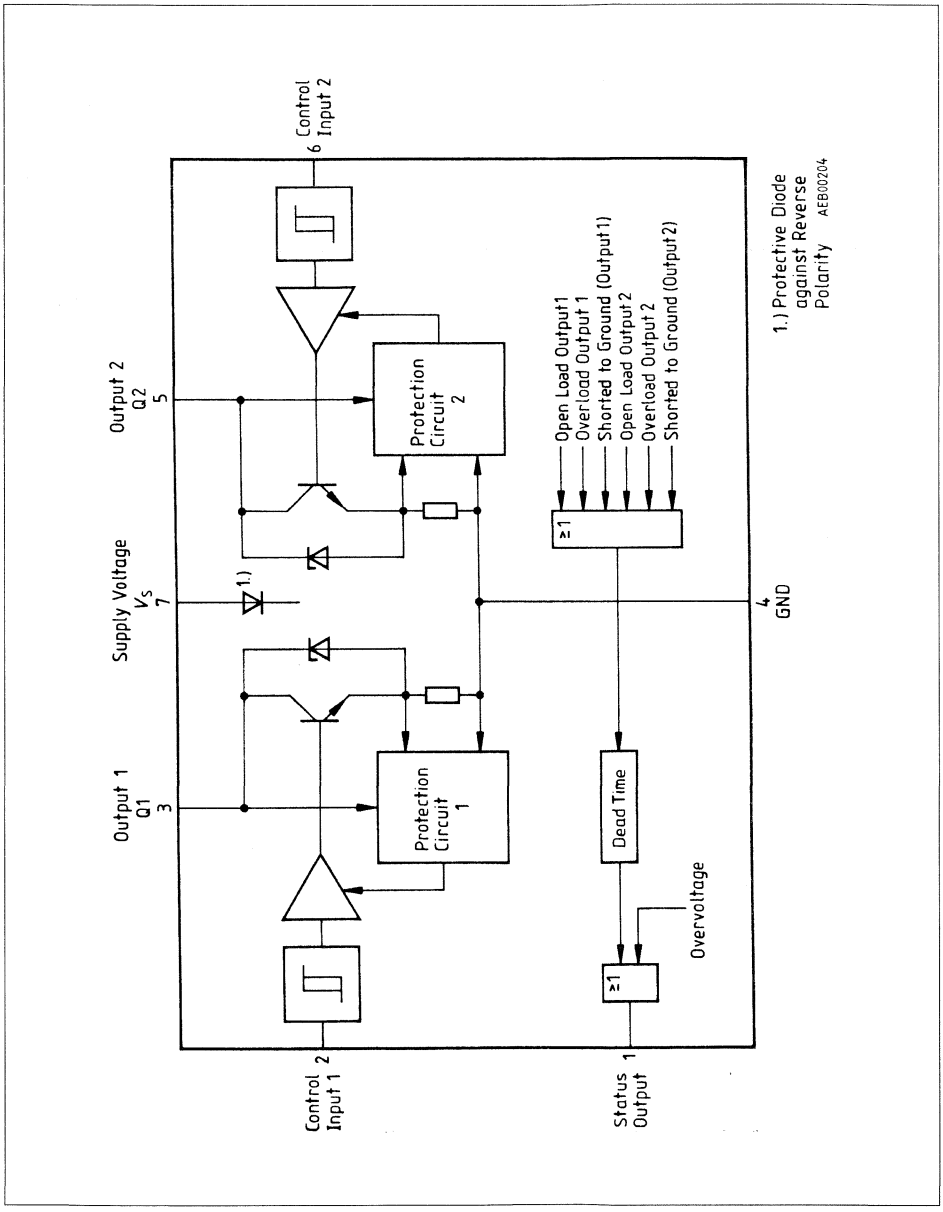
- Overload,
- Open load,
- Shorted load to ground,
- Overvoltage.



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	STA	**Status output (open collector)** for both outputs; indicates overload, open load and shorted load to ground as well as overvoltage at pin 7. In case of malfunction the status output is switched to low after a delay time (except overvoltage).
2	IN1	**Control input 1 (TTL-compatible)** activates output transistor 1 in case of low-potential.
3	Q1	**Output 1** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
4	GND	**Ground** Wiring must be designed for a max. short-circuit current (2 × 3.5 A).
5	Q2	**Output 2** Shorted-load protected, open collector output with 36 V clamp Z-diode to ground.
6	IN2	**Control input 2 (TTL-compatible)** activates output transistor 2 in case of low-potential.
7	V_S	**Supply voltage** In case of overvoltage at this pin large sections of the circuit are de-activated. The status output indicates the malfunction without delay time.



Block Diagram

11

Circuit Description

Input Circuits

The control inputs comprise TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the inverting buffer amplifiers convert the logic signal for driving the NPN power transistors.

Switching Stages

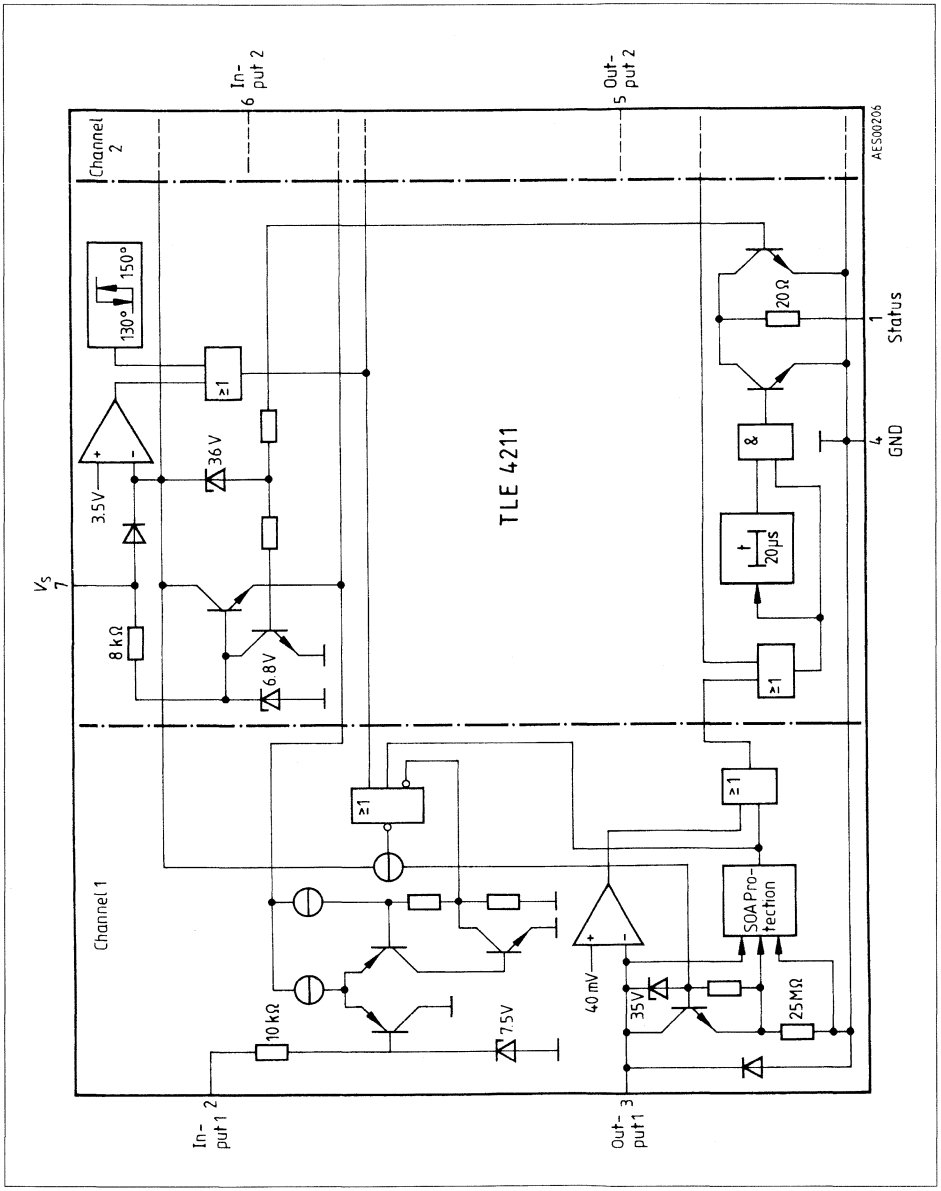
The output stages comprise NPN power transistors with open collectors. Since the protective circuit allocated to each stage limits the power dissipation, the outputs are shorted-load protected to the supply voltage throughout the entire operating range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated clamp Z-diodes.

Monitoring and Protective Functions

The outputs are monitored for open load, overload, and shorted load to ground (see table below). In addition, large sections of the circuit are de-activated in case of excessive supply voltages V_S. Linked via OR gate the information regarding these malfunctions effects the status output (open collector, active low). An internally determined delay time applied to all malfunctions but overvoltage prevents the output of messages in case of short-term malfunctions. Furthermore, a temperature protection circuit prevents thermal overload. An integrated reverse diode protects the supply voltage V_S against reverse polarities. Similarly the load circuit is protected against reverse polarities within the limits established by the maximum ratings (no shorted load at the same time!). At supply voltages below the operating range an undervoltage detector ensures that neither the status nor the outputs are activated.

Status Output (L = Error)

	Undervoltage	**Operating Range**		**Overvoltage**
		V_I = L (active)	V_I = H (passive)	
Normal function	H	H	H	L
Overload	H	L	H	L
Open load	H	L	H	L
Shorted load to ground	H	L	L	L



Circuit Diagram

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Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Voltages				
Supply voltage (pin 7) [1]	V_S	– 45	45	V
Supply voltage (pin 7) $t \leq 500$ ms	V_S	–	70	V
Input voltage (pin 2; pin 6)	V_I	– 5	45	V
Output voltage (pin 1)	V_Q	– 0.3	45	V
Currents				
Switching current (pin 3; pin 5)	I_Q	limited internally		
Current with reverse polarity (pin 3; pin 5) $T_C \leq 85$ °C	I_Q	– 2.2	–	A
Output current (pin 1)	I_Q	–	10	mA
Max. current at inductive load	I_Q	–	**see Diagram**	
Junction temperature	T_j	–	150	°C
Storage temperature	T_{stg}	– 50	150	°C
Operating Range				
Supply voltage	V_S	5.6 [2]	20	V
Supply voltage slew rate	dV_S/dV	–1	1	V/µs
Ambient temperature	T_A	– 40	125	°C
Thermal resistance				
junction to case	$R_{th\ JC}$	–	4	K/W
junction to ambient	$R_{th\ JA}$	–	65	K/W

[1] Refer to monitoring and protective functions

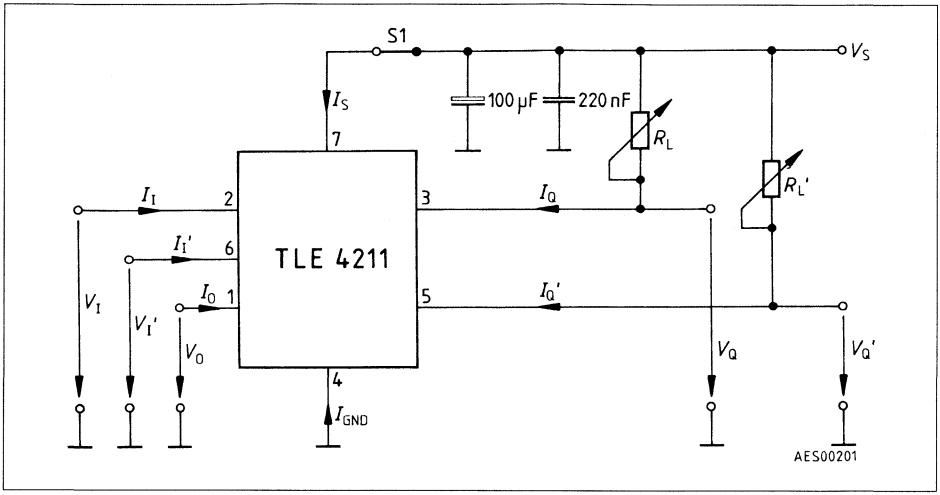
[2] Lower limit = 4.5 V, if previously V_S greater than 5.6 V (turn-on hysteresis)

Characteristics V_S = 6 to 1 V and T_A = – 40 to 125 °C

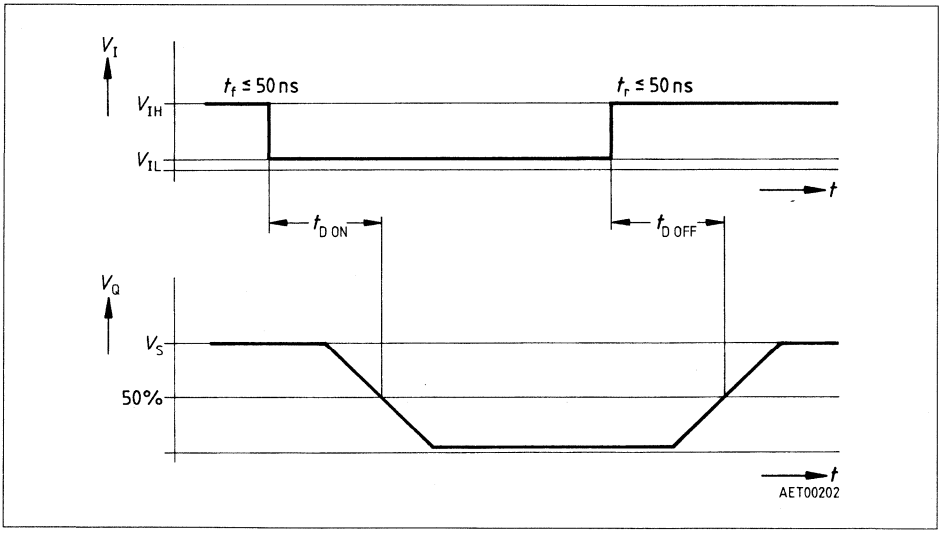
Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Condition
General Characteristics						
Quiescent current	I_S	–	3.5	10	mA	$V_I = V_I > V_{IH}$
Supply current	I_S	–	100	180	mA	$V_I = V_I < V_{IL}$
Supply overvoltage shutdown threshold	V_{SO}	34	36	42	V	I_Q = 5 mA; V_Q < 0.4 V
Open load error threshold voltage	V_{QU}	–	40	–	mV	I_Q = 5 mA; V_Q < 0.4 V
Open load error threshold current	I_{QU}	–	50	80	mA	$V_Q = V_{QU}$
Open load error threshold current for both channels active	I_{QU}	–	–	250	mA	$V_{Q1} = V_{Q2} = V_{QU}$
Logic						
Control input						
H-input voltage	V_{IH}	–	1.7	2.4	V	–
L-input voltage	V_{IL}	0.7	1.1	–	V	–
Hysteresis of input voltage	ΔV_I	–	0.6	–	V	–
H-input current	I_{IH}	–	–	10	µA	V_I = 5 V
L-input current	$-I_{IL}$	–	–	10	µA	V_I = 0.5 V
Status output (open coll.) L-saturation voltage	V_{OSat}	–	–	0.4	V	I_Q = 5 mA
Status delay time	t_{dS}	12	20	30	µs	[1]
Power Output						
Saturation voltage	V_{QSat}	–	0.6	0.8	V	I_Q = 1.6 A; $V_I < V_{IL}$; T_j = 25°C
Leakage current	I_Q	–	–	300	µA	V_Q = 6 V; $V_I > V_{IH}$
Switch-ON time	$t_{D\,ON}$	–	0.5	5	µs	**see Timing Diagram**;
Switch-OFF time	$t_{D\,OFF}$	–	2.5	10	µs	I_Q = 1 A
Output voltage Negative clamp	$-V_{QF}$	–	1.4	1.8	V	I_Q = – 2.0 A
Power Clamp Diode (V_S = 42 V; S_1 open)						
Output voltage positive clamp	V_{QZ}	34	36	40	V	I_Q = 0.1 A
Serial resistance	r_Z	–	2	–	Ω	0 A < I_Q < 2 A

[1] Period from the beginning of the disturbance at one channel (exception: overvoltage) until the 50 % value of the status switching edge is reached.

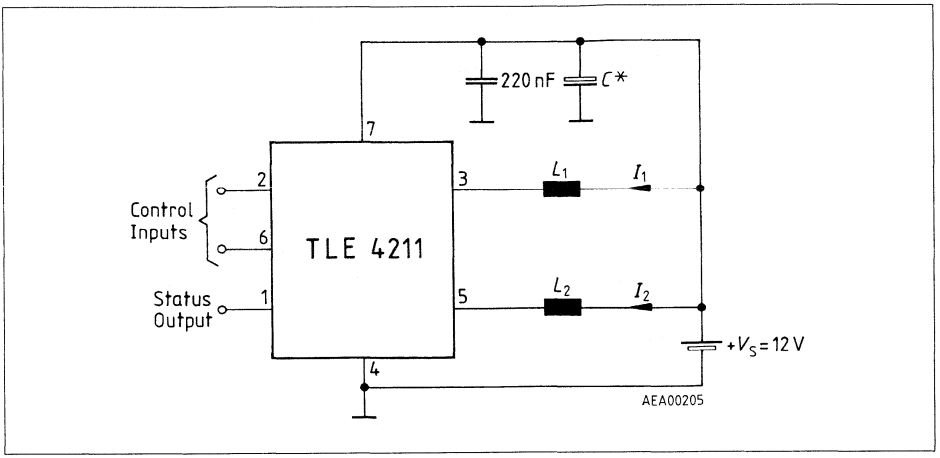
11



Test Circuit



Timing Diagram

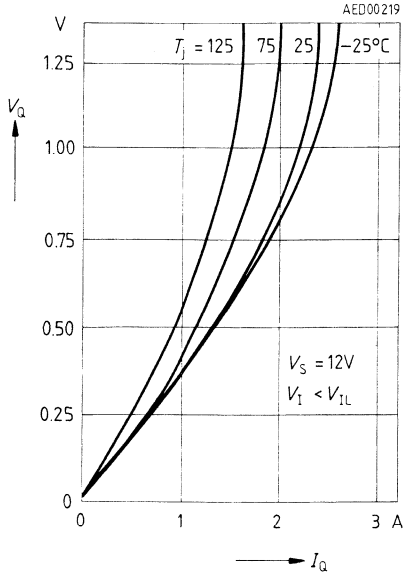


Application Circuit

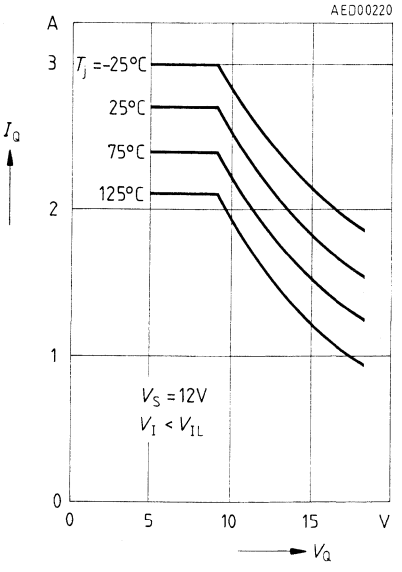
C^* is to be dimensioned such that e.g. in case of a battery voltage failure the maximum ratings of the IC are not exceeded by the recirculation energy L_1, L_2.

11

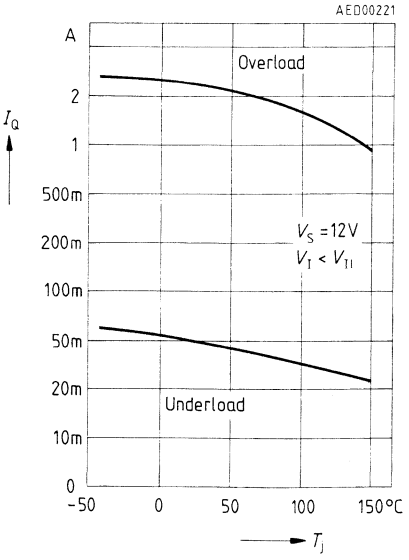
Output Voltage V_Q versus Output Current I_Q



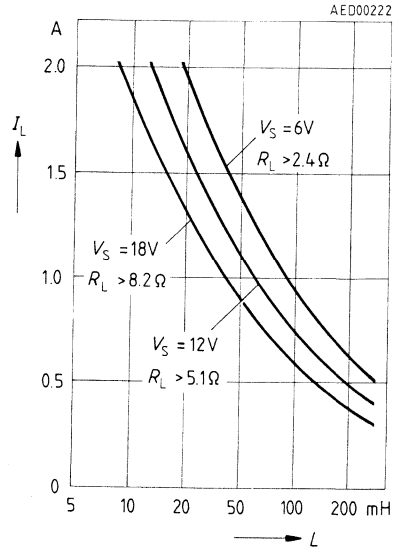
Shorted Load Current I_{Q0} versus Output Voltage V_Q



Status Signal Threshold versus Chip Temperature T_j



Maximum Load Current I_L versus Load Inductance L



SIEMENS

Intelligent Double 4-A Low-Side Switch

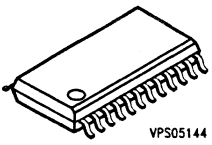
TLE 5224

Preliminary Data

SPT-IC

Features

- Double low-side switch (2 x 4 A)
- Low ON-resistance (typical 0.25 Ω)
- Power limitation
- Overtemperature shutdown
- Overload shutdown
- Status monitoring
- Integrated clamp Z-diode
- Shorted load protecting
- Temperature range: – 40 to 85 °C



P-DSO-24-1

Type	Ordering Code	Package
▼ TLE 5224 G	Q67000-A9116	P-DSO-24-1 (SMD)

▼ New type

The TLE 5224 G is an integrated double low-side power switch with power limitation, load interrupt and shorted load detection, temperature monitoring, error signaling via two status outputs and integrated Z-diodes for output clamping. The TLE 5224 G is designed for automotive applications.

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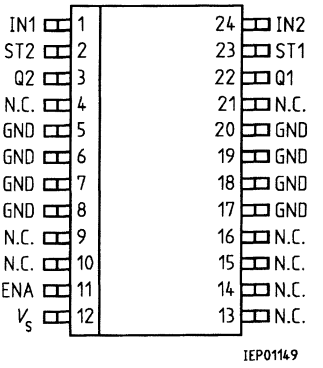
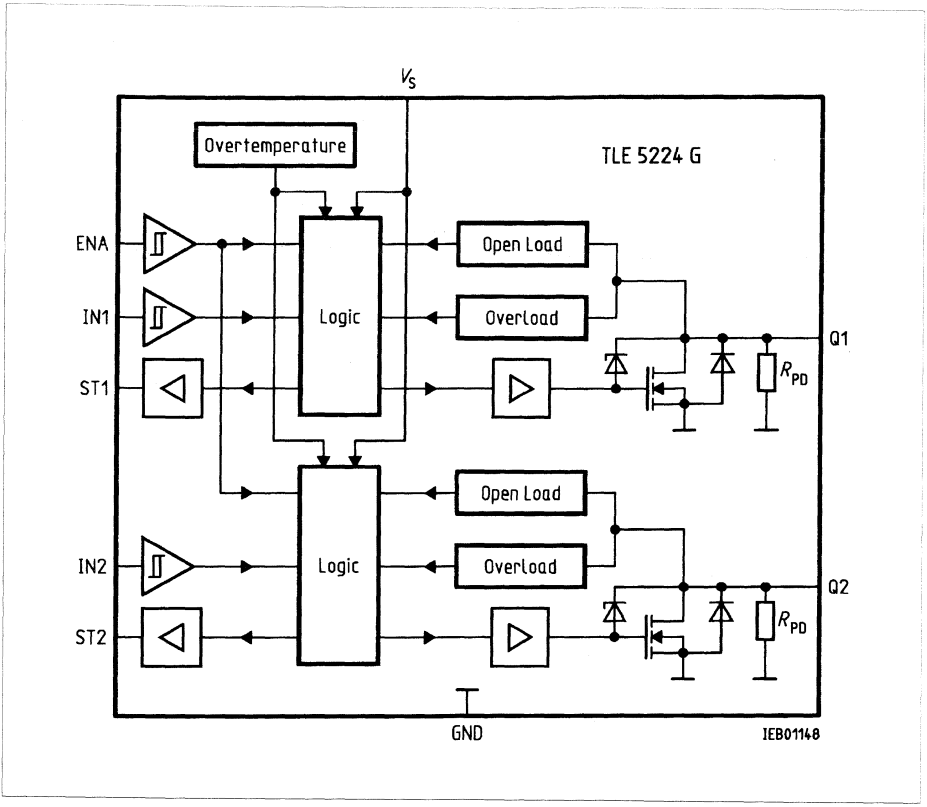


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Control input channel 1
2	ST2	Status output channel 2
3	Q2	Power output channel 2
4	N.C.	Not connected, cooling
5, 6, 7, 8	GND	Ground, cooling
9, 10	N.C.	Not connected, cooling
11	ENA	Enable input for both channels
12	V_S	Supply voltage
13, 14, 15, 16	N.C.	Not connected, cooling
17, 18, 19, 20	GND	Ground, cooling
21	N.C.	Not connected, cooling
22	Q1	Power output channel 1
23	ST1	Status output channel 1
24	IN2	Control input channel 2



Block Diagram

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Application Description

This IC is specially designed to drive inductive loads (relays, electromagnetic valves). Integrated clamp-diodes limit the discharging EMF during switch off when inductive loads are turned off.

For the detection of errors there are two status outputs, which monitor the following errors by logic levels:

- thermal overload,
- open and shorted load to ground in active and inactive mode,
- overloading of output (also shorted load to supply) in active mode.

Circuit Description

Input Circuits

The control and enable inputs, all active high, consist of Schmitt triggers with hysteresis. All inputs are connected with pull-down current sources. Not connected inputs are interpreted as "low".

Switching Stages

The power outputs consist of a DMOS power transistor with open drain. The output stages are shorted-load-protected throughout the operating range. Integrated clamp diodes limit voltage spikes produced when inductive loads are discharged.

Protective Circuit

The outputs are protected against current overload and thermal overload. There is no protection against reverse polarity of the supply voltage.

Error Detection

The status outputs signal the status of the switching stages at normal operation (LOW = OFF; HIGH = ON). In case of any error the status outputs are set according to the table below.

If current overload occurs, the error condition is stored in an internal register and the output is shutdown. To reset this register the control input of the affected channel has to be switched off and then on again.

The state of the error detection circuit is directly dependent on the input status.

In case of thermal overload both channels will be shutdown. In any other error condition, only the affected channel will be switched off (not influencing the power or status output of the second non-affected channel).

Diagnostic Table

Operating Condition	Inputs			Power Outputs		Status Outputs	
	ENA	IN1	IN2	Q1	Q2	ST1	ST2
Normal Function	L	X	X	OFF	OFF	L	L
	H	L	L	OFF	OFF	L	L
	H	H	L	ON	OFF	H	L
	H	L	H	OFF	ON	L	H
	H	H	H	ON	ON	H	H
Overtemperature	X	L	L	OFF	OFF	H	H
	X	H	L	OFF	OFF	L	H
	X	L	H	OFF	OFF	H	L
	X	H	H	OFF	OFF	L	L
Open Load Channel 1	X	L	X	OFF	1)	H	1)
	L	H	X	OFF		H	
	H	H	X	ON		L	
Open Load Channel 2	X	X	L	1)	OFF	1)	H
	L	X	H		OFF		H
	H	X	H		ON		L
Overload Channel 1	L	X	X	OFF	1)	L	1)
	H	L	X	OFF		L	
	H	H	X	OFF		L	
Overload Channel 2	L	X	X	1)	OFF	1)	L
	H	X	L		OFF		L
	H	X	H		OFF		L

1) Power and status outputs according to normal function

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Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	60	V	–
Output voltage	$V_{Q1,2}$	–	45	V	–
Output voltage	$V_{Q1,2}$	–	65	V	$t \leq 1$ ms
Output voltage	V_{ST}	– 0.3	45	V	–
Input voltage	$V_{IN1, IN2, ENA}$	– 1.5	6	V	$I_I < 10$ mA
Currents					
Output current	$I_{Q1,2}$	5	–	A	limited internally;
Current at reverse poling	$I_{Q1,2}$; I_{GND}	– 4	–	A	–
Output current, status pin	I_{ST}	– 5	5	mA	–
Discharging energy of inductive load per channel	E	–	50	mJ	$T_j \leq 25$ °C
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	–	175	°C	during clamping
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	4.8	45	V	–
Supply voltage rise	dV_S/d_t	– 1	1	V/µs	–
Output voltage	$V_{QI,2}$	– 0.3	45	V	–
	$V_{QI,2}$	–	65	V	during clamping
Reverse current into inputs	$I_{IN1, IN2, ENA}$	– 10	–	mA	–
Output voltage	V_{ST}	– 0.3	45	V	–
Output current	I_{ST}	0	2	mA	–
Ambient temperature	T_A	– 40	85	°C	$T_j \leq 150$ °C
Chip temperature	T_j	–	175	°C	during clamping
Thermal resistance					
junction to case	$R_{th\,JC}$	–	12	K/W	1)
junction to ambient	$R_{th\,JA}$	–	75	K/W	–

1) Pins 4 to 10 and 13 to 21 have to be connected to the ground-plane used as thermal heatsink to achieve the optimum thermal resistance.

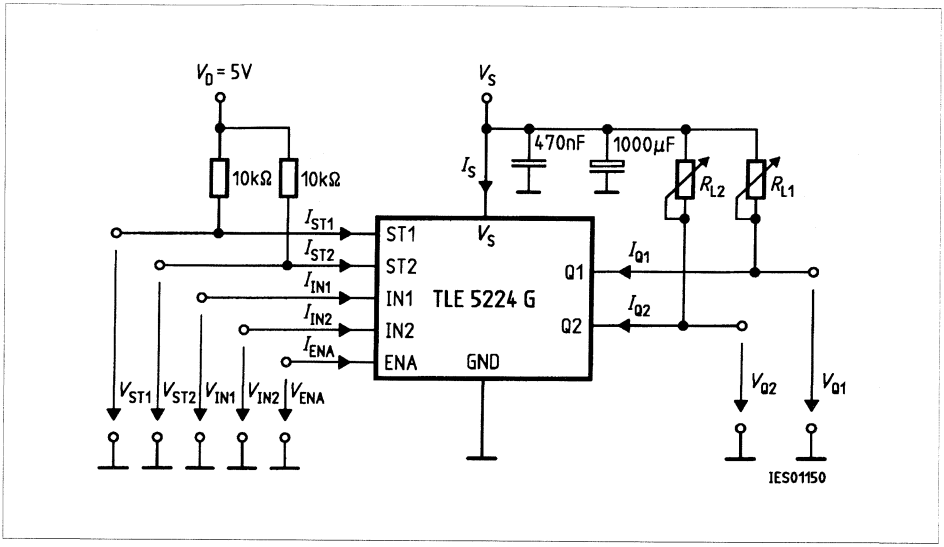
Characteristics

V_S = 5.5 to 45 V; typ. V_S = 12 V; T_A = – 40 to 125 °C; $T_j \leq$ 150 °C, V_D = 5.1 V

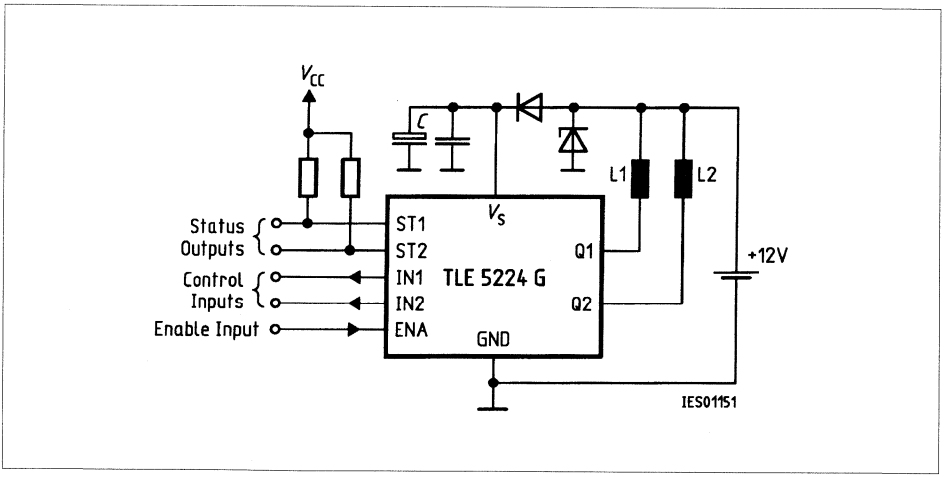
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Quiescent current	I_S	–	0.6	1	mA	Outputs OFF
Supply current	I_S	–	1.8	4	mA	Outputs ON
Open load current	I_{Qu}	–	–	250	mA	Output on, V_{ST} < 0.5 V
Open load shutdown voltage threshold	V_{Qu}	0.5 * V_S	– –	0.6 * V_S	V	Outputs on, V_{ST} > 5 V
Overload shutdown current threshold	I_{QO}	5	–	–	A	Outputs ON; V_{ST} < 0.5 V T_j = – 40 to 50 °C
	I_{QO}	4	–	–	A	T_j = 50 to 150 °C
Overtemperature shutdown threshold	T_{th}	155	–	185	°C	only a design value
hysteresis	ΔT_{th}	–	10	–	°C	only a design value
Power Output						
Static drain source ON-resistance	R_{DSON}	–	0.25	–	Ω	T_j = 25 °C
	R_{DSON}	–	–	0.5	Ω	T_j = 150 °C; I_Q = 4 A
Pull-down resistance	R_{PD}	14	20	26	kΩ	T_j = 25 °C
Clamping Voltage	V_{QZ}	45	–	65	V	–
Input (IN1; IN2; ENA)						
H-Input voltage	V_{IH}	2.0	–	6.0	V	–
L-Input voltage	V_{IL}	– 0.3	–	1.0	V	–
Hysteresis	ΔV_I	0.2	–	0.6	V	–
H-input current	$I_{IN1\,;\,IN2}$	50	100	140	µA	$V_{IN1;\,IN2}$ = 5 V; T_j = 25 °C
H-input current	I_{ENAH}	15	30	40	µA	V_{ENA} = 5 V; T_j = 25 °C
Status Output						
L-output voltage	V_{ST}	–	–	0.5	V	I_{ST} = 2 mA
H-leakage current	I_{STH}	–	–	2	µA	–
Output ON delay time	t_1	10	25	40	µs	I_Q = 0.2 A
Output ON fall time	t_2	–	20	–	µs	I_Q = 0.2 A
Output OFF rise time	t_3	–	25	–	µs	I_Q = 2 A
Output OFF status delay	t_4	20	40	60	µs	I_Q = 2 A
Output ON status rise	t_5	–	–	50	µs	1)
Overload OFF delay time	t_{dSO}	50	–	150	µs	only a design value

1) Time between status valid and switching on or error detection.

11

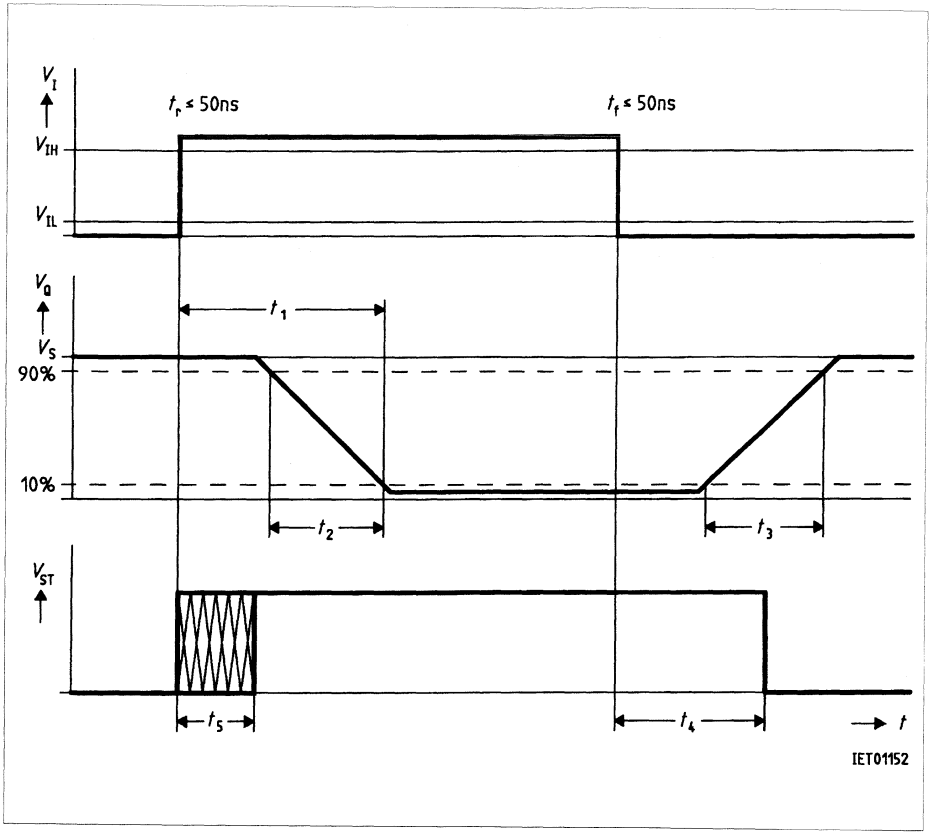


Test Circuit



Application Circuit

The blocking capacitor C is recommended to avoid critical negative voltage spikes on V_S in case of battery interruption during off-communicating.



Timing Diagram

11

SIEMENS

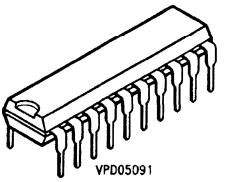
Intelligent Sixfold Low-Side Switch

TLE 4216

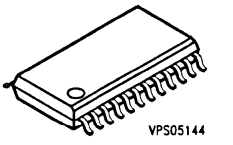
Bipolar IC

Features

- Double low-side switch, 2 x 0.5A
- Quad low-side switch, 4 x 50 mA
- Power limitation
- Open-collector outputs
- Overtemperature shutdown
- Status monitoring
- Shorted-load protection
- Integrated clamp Z-diodes
- Temperature range – 40 to 110 °C



P-DIP-20-1



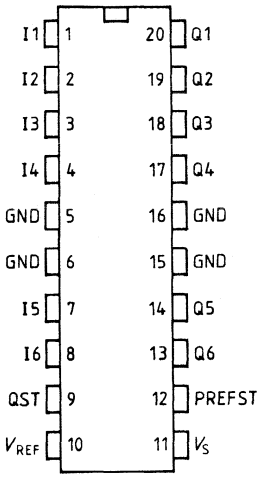
P-DSO-24-1

	Type	Ordering Code	Package
S	TLE 4216	Q67000-A8237	P-DIP-20-1
S ▼	TLE 4216 G	Q67000-A9108	P-DSO-24-1 (SMD)

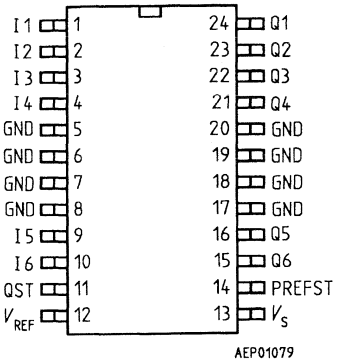
▼ New type

TLE 4216 is an integrated, sixfold low-side power switch with power limiting of the 0.5 A outputs, shorted load protection of the 50 mA switches and Z-diodes on all switches from output to ground. TLE 4216 is particularly suitable for automotive and industrial applications.

TLE 4216



TLE 4216 G



Pin Configuration
(top view)

Pin Definitions and Functions

TLE 4216 G Pin	TLE 4216 Pin	Symbol	Function
1, 2, 3, 4	1, 2, 3, 4	I1, I2, I3, I4	Inputs of 50-mA switches 1, 2, 3, 4
5, 6, 7, 8	5, 6	GND	Ground, cooling
9, 10	7, 8	I5, I6	Inputs of 0.5 A switches 5, 6
11	9	Q_{ST}	Status analog output
12	10	V_{REF}	Reference voltage; a higher reference voltage than the internal one can be applied from the exterior as a voltage reference for the status output (A/D converter).
13	11	V_S	Supply voltage
14	12	PREFST	Preferred state (low = preferred state of all outputs regardless of inputs)
15, 16	13, 14	Q6, Q5	Outputs 6, 5 (0.5 A), open collector
17, 18, 19, 20	15, 16	GND	Ground, cooling
21, 22, 23, 24	17, 18, 19, 20	Q4, Q3, Q2, Q1	Outputs 4, 3, 2, 1 (50 mA), open collector

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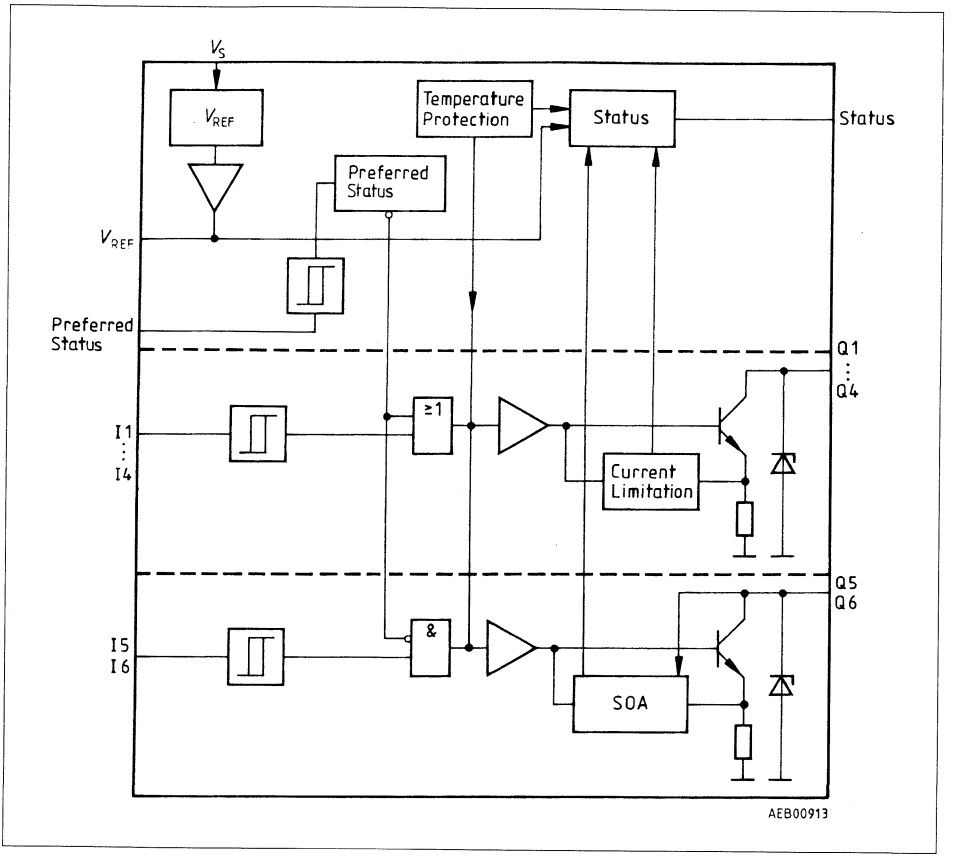

Block Diagram

Circuit Description

Input Circuits

The control inputs and the preferred-state input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with open collectors. Each stage has its own protective circuit for limiting power dissipation and shorted-load current, which makes the outputs shorted-load protected to the supply voltage throughout the operating range. Integrated Z-diodes limit positive voltage spikes that occur when inductive loads are discharged.

Monitoring and Protective Functions

Each output is monitored in its activated status for overload. Furthermore, large parts of the circuitry are shutdown (control, output stages). The information from these malfunctions is ORed and applied to the status output. If several malfunctions appear simultaneously, the highest voltage level will dominate. The IC is also protected against thermal overload. If a chip temperature of typically 160 °C is reached, overtemperature is signalled on the status output. If the temperature continues to increase, all outputs are turned off at 170 °C.

If the minimum supply voltage for functioning is not maintained, the output stages become inactive. At a supply voltage of 2 to 4 V, the outputs are switched to a preferred state regardless of the level on pin PREFST. If the preferred state is to be maintained beyond this range, pin PREFST must be switched to low potential. Above a supply voltage of typical 3 V (max. 4 V) the preferred state is controlled by pin PREFST. From 4 to 5.2 V the logic operation of the outputs is guaranteed, but the status output cannot be evaluated. At a supply voltage of 5.2 to 30 V the full function is guaranteed.

Application Description

Applications in automotive electronics require intelligent power switches activated by logic signals, which are shorted-load protected and provide error feedback.

The IC contains six power switches connected to ground (low-side switch). On inductive loads the integrated Z-diodes clamp the discharging voltage.

By means of TTL signals on the control inputs (active high) all six switches can be activated independently of one another when a high level appears on the preferred-state input. When there is a low level on the preferred-state input, switches 1 to 4 are switched on, switches 5 and 6 are switched off regardless of the input level. The inputs are highly resistive and therefore must not be left unconnected, but should always be on fixed potential (noise immunity).

The status output signals the following malfunctions by analog voltage levels:

- Overload
- Overtemperature

Possible Input and Output Levels

Supply Voltage V_S	PREFST	I_1 ... I_6	Q1 ... Q4	Q5, Q6
2 to 4 V	L	X	L	H
4 to 30 V	H	L	H	H
4 to 30 V	H	H	L	L

Absolute Maximum Ratings
T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 1	40	V	–
Supply voltage, load circuit	V_{Q1-6}	– 0.7	25	V	–
Input voltage	$V_{I1-6}, V_{\overline{PRESET}}$	0	V_S	V	–
Input voltage	$V_{REF\ ext}$	– 0.7	7	V	–
Currents					
Switching current	I_{Q1}-I_{Q6}	–	–	–	limited internally
Current on reverse poling in load circuit	$I_{Q5, Q6}$	– 0.5	–	A	–
Current on reverse poling in load circuit	I_{Q1-Q4}	– 50	–	mA	–
Output current positive clamp	I_{Z5-Z6}	–	0.7	A	–
Output current positive clamp	I_{Z1-Z4}	–	70	mA	–
Junction temperature	T_j	– 40	150	°C	Temp. protection shutdown at 170 °C
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Supply voltage	V_S	5.2	30	V	$V_{REF} \leq V_S$, functioning is guaranteed at V_S = 4 – 5.2 V but status output cannot be evaluated.
Supply voltage in load circuit	V_{Q1-6}	– 0.3	24	V	–
Ambient temperature	T_A	– 40	110	°C	–
Supply voltage for load short-circuit	V_S	–	16	V	–
Input current (high)	I_{IH}	–	100	µA	–
Thermal resistance Junction-ambient	$R_{th\ JA}$	–	65	K/W	P-DSO-24-1
Junction-ambient	$R_{th\ JA}$	–	55	K/W	P-DIP-20-1

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Characteristics

V_S = 5 to 12 V; T_j = – 25 to 140 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
General						
Supply current	I_S	–	50	70	mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$
Supply current	I_S	–	36	50	mA	$V_I > V_{IH}$; $V_{IP} > V_{IH}$; V_S = 5 V
Quiescent current	I_S	–	8	11	mA	$V_I < V_{IL}$; $V_{IP} > V_{IH}$
Logic (Control inputs + preferred state)						
H-switching threshold	V_{IH}	1.3	1.8	2.1	V	–
L-switching threshold	V_{IL}	0.9	1.2	1.5	V	–
Hysteresis	ΔV_I	0.3	0.6	1.0	V	–
Input current						
H-input current	I_{IH}	0	–	20	µA	$V_I < 6$ V
L-input current	$-I_{IL}$	0	–	20	µA	0.5 V < V_I < 6 V
Switching Stages						
Load current	$I_{Q1\text{-}Q4}$	50	–	–	mA	V_S = 2 V (preferred state)
Saturation voltage	$V_{Qsat\ 5,\ 6}$	–	0.5	0.8	V	I_Q = 0.4 A; $V_I > V_{IH}$
Saturation voltage	$V_{Qsat\ 1\text{-}4}$	–	0.4	0.6	V	I_Q = 50 mA: $V_I > V_{IH}$
Saturation voltage	$V_{Qsat\ 1\text{-}4}$	–	–	0.22	V	I_Q = 20 mA: $V_I > V_{IH}$
Turn-ON time	$t_{D\text{-}ON}$	0.2	1	1.5	µs	**see Diagrams**
Turn-OFF time	$t_{D\text{-}OFF}$	0.2	1	1.5	µs	**see Diagrams**; $I_L = I_{max}$
Temperature Protection						
Overtemperature (signaled on status output)	–	–	160	–	°C	–
Overtemperature (outputs shut down)	–	–	170	–	°C	–

Characteristics (cont'd)
V_S = 5 to 12V; T_j = – 25 to 140 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs						
Output voltage pos. clamp	V_{Q1-4}	25.5	–	33	V	I = 50 mA
Output voltage pos. clamp	V_{Q5-6}	25.5	–	33	V	I = 0.5 A
Shorted-load current	$I_{Q1max-Q4max}$	50	–	120	mA	V_Q < 16 V
Leakage current	I_{Q1-4}	–	–	200	nA	V_Q = 24V; T_j = 125°C
Leakage current	$I_{Q5;6}$	–	–	300	µA	V_Q = 24V
Shorted-load current	$I_{Q5max-Q6max}$	–	–	–	–	**see Diagrams**
Status output						
No error	V_{St}	–	–	0.5	V	V_{REF} = 5 V [1]
Overload output 6	V_{St}	1.0	–	1.3	V	V_{REF} = 5 V [1]
Overload output 5	V_{St}	1.4	–	1.7	V	V_{REF} = 5 V [1]
Overload output 4	V_{St}	1.8	–	2.1	V	V_{REF} = 5 V [1]
Overload output 3	V_{St}	2.2	–	2.5	V	V_{REF} = 5 V [1]
Overload output 2	V_{St}	2.6	–	2.9	V	V_{REF} = 5 V [1]
Overload output 1	V_{St}	3.0	–	3.3	V	V_{REF} = 5 V [1]
Overtemperature	V_{St}	3.5	–		V	V_{REF} = 5 V [1]
Source resistance of status output	R_{QSt}	100	–	550	Ω	–
Delay time of status	t_{dst}	–	–	10	µs	Shorted load
Reference voltage (internal)	V_{REF}	–	2.5		V	–
Input resistance of reference pin	$R_{REF\ in}$	8	10	14.5	Ω	V_{REF} = 2.6 – 6.5 V

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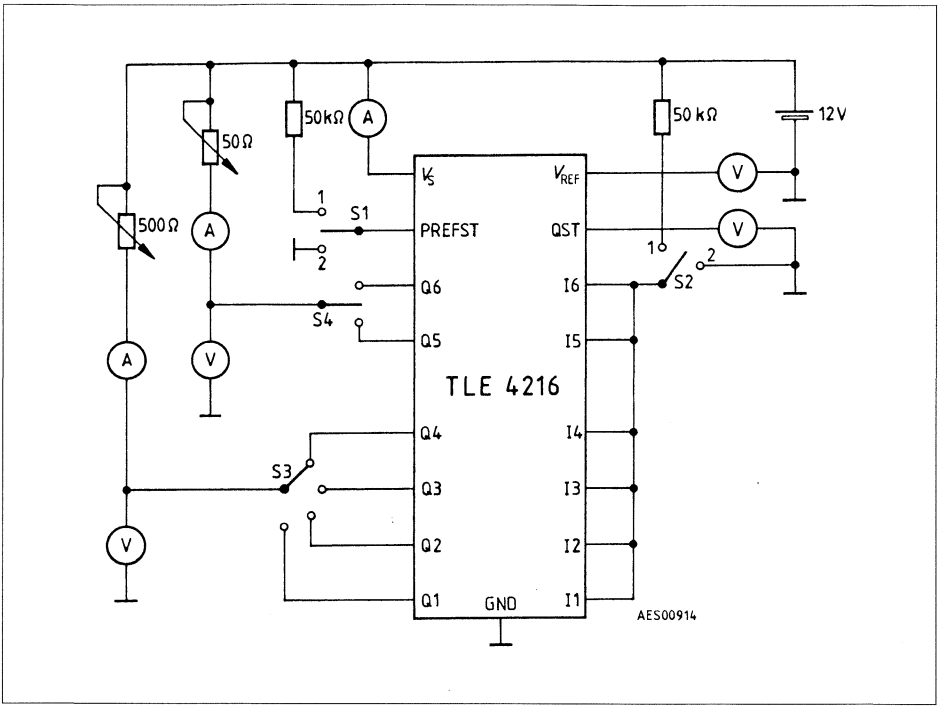
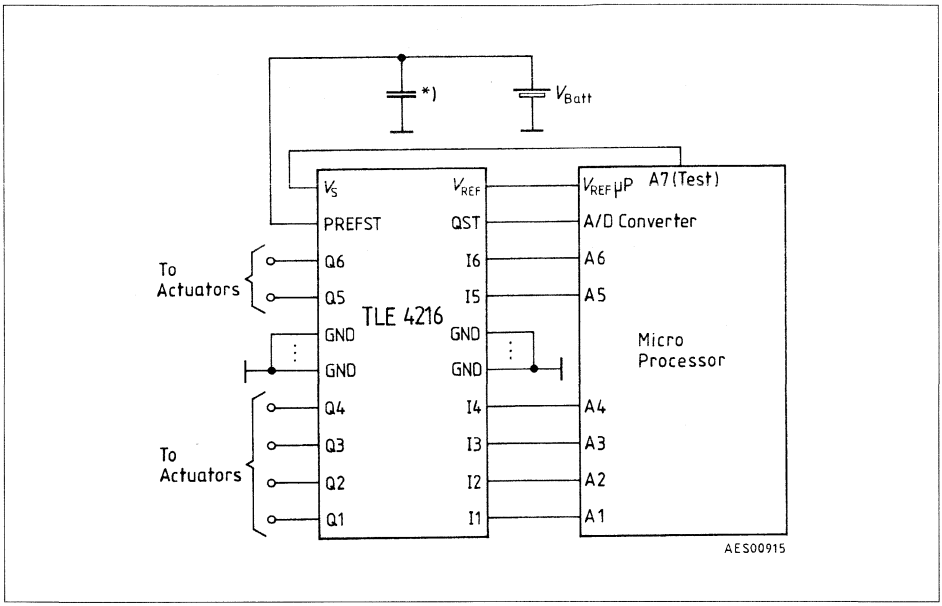
[1] The limits shift proportionally for a higher value of reference voltage.



Test Circuit

S1 in position 1: all switches can be activated by S2 (position 1) or deactivated (position 2)

S1 in position 2: preferred state



Application Circuit

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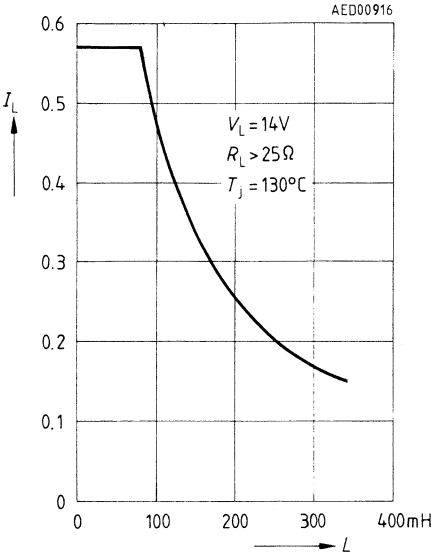
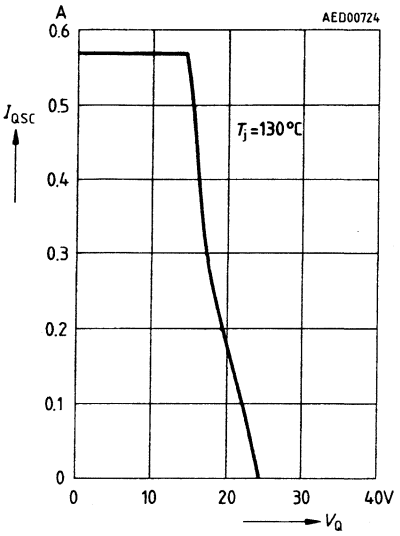
*) The capacitance depends on the inductance and current load of the supply.

Diagrams

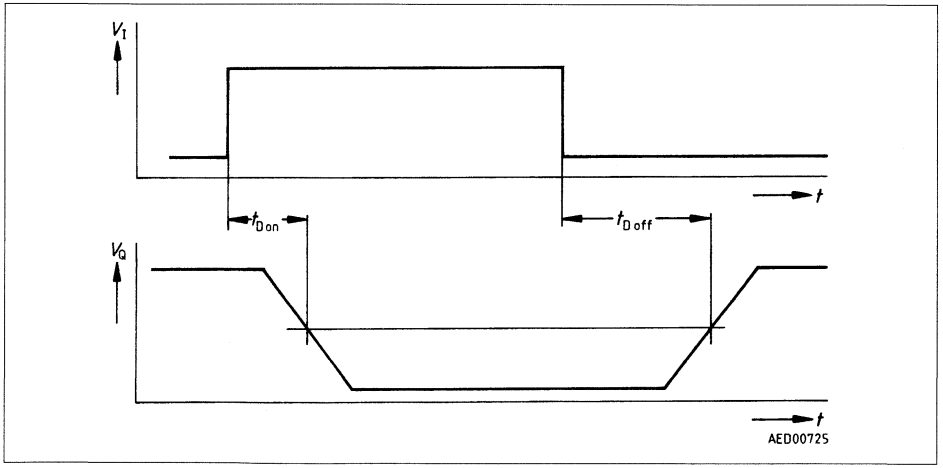
Permissible Load Inductance versus Load Current



Short-Circuit Current I_{QO} versus Output Voltage V_Q (0.5 A outputs)



When switching the maximum inductive loads, the maximum temperature T_j of 150 °C may be briefly exceeded. The IC will not be destroyed by this, but the restrictions concerning useful life should be observed.



SIEMENS

Intelligent Sixfold Low-Side Switch

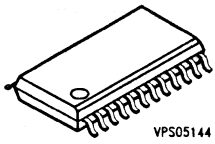
TLE 4226

Preliminary Data

Bipolar-IC

Features

- Quad 50 mA outputs
- Dual 500 mA outputs
- Output stages with power limiting
- Open-collector outputs
- Shorted load protected in operating range
- Clamp-diode to ground
- Status signaling
- TTL-compatible control inputs
- Temperature monitoring
- Temperature range – 40 to 125 °C



P-DSO-24-1

Type	Ordering Code	Package
▼ TLE 4226 G	Q67000-A9118	P-DSO-24-1 (SMD)

▼ New type

TLE 4226 G is an integrated, sixfold low-side power switch with power limiting of the 0.5 A outputs, shorted-load protection of the 50 mA switches and Z-diodes on all switches from output to ground. TLE 4226 G is particularly suitable for automotive and industrial applications.

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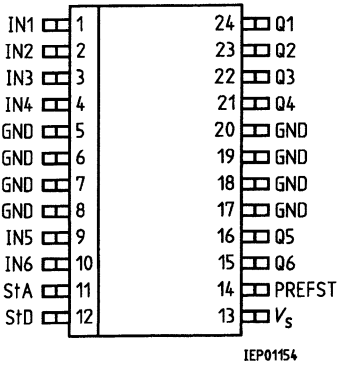
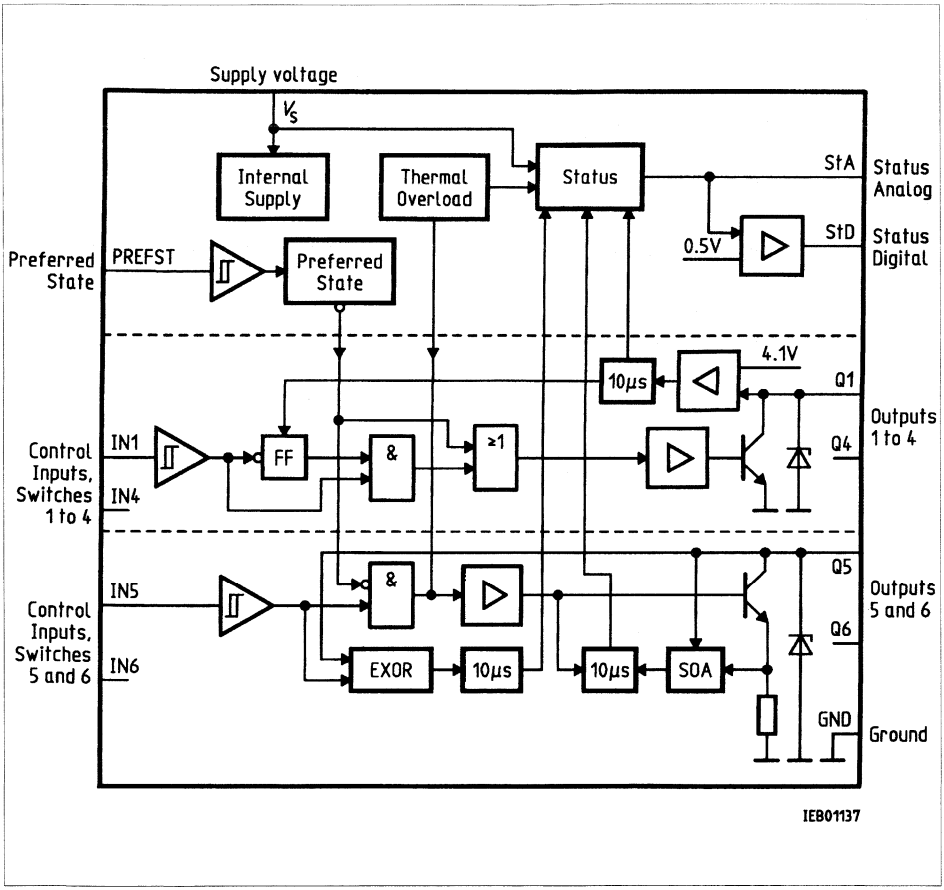


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Input switch 1, active high (50 mA)
2	IN2	Input switch 2, active high (50 mA)
3	IN3	Input switch 3, active high (50 mA)
4	IN4	Input switch 4, active high (50 mA)
5, 6, 7, 8	GND	Ground, cooling
9	IN5	Input switch 5, active high (500 mA)
10	IN6	Input switch 6, active high (500 mA)
11	StA	Status output analog
12	StD	Status output digital
13	V_S	Supply voltage
14	PREFST	Preferred state input, active low
15	Q6	Output switch 6 (500 mA)
16	Q5	Output switch 5 (500 mA)
17, 18, 19, 20	GND	Ground, cooling
21	Q4	Output switch 4 (50 mA)
22	Q3	Output switch 3 (50 mA)
23	Q2	Output switch 2 (50 mA)
24	Q1	Output switch 1 (50 mA)



Block Diagram

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Application Description

Applications in automotive electronics call for intelligent power switches that can be activated by logic signals, which have to be shorted load protected and which provide error feedback.

This IC contains six power switches connected to ground (low-side switches). On inductive loads the integrated Z-diodes clamp the discharging voltage.

By means of TTL signals on the control inputs (active high) all six switches can be activated independently of one another when a high level appears on the preferred-state input. When there is a low level on the preferred-state input, switches 1 to 4 are switched on, switches 5 and 6 are switched off regardless of the control-input levels. The inputs are highly resistive and therefore must not be left unconnected but should always be on fixed potential (noise immunity). Inputs that are not used, should be connected to low level to reduce the power consumption.

The analog status output signals the following errors by analog voltage levels:

- Overload
- Thermal overload
- Openload or shorted load to ground (only switches 5 and 6)

The following levels signal errors at the analog and digital status outputs.

Errors	Analog Status	Digital Status
Normal function	Low	High
Overload	High	Low
Openload or shorted load to ground (only switches 5 and 6)	High	Low
Thermal overload	> 3.5 V	Low

Possible Input and Output Levels

Supply Voltage V_S	PREFST	IN1-6	Q1-Q4	Q5, Q6
2 to 5 V	Low	Random	Low	High
5 V	High	Low	High	High
5 V	High	High	Low	Low

Circuit Description

Input Circuits

The control inputs and the preferred-state input consist of TTL-compatible Schmitt triggers with hysteresis. Driven by these stages the buffer amplifiers convert the logic signal necessary for driving the NPN power transistors.

Switching Stages

The output stages consist of NPN power transistors with open collectors. Each stage has its own protective circuit for limiting power dissipation and shorted load current, which makes the outputs shorted load protected to the supply voltage throughout the operating range. Integrated clamp-diodes limit positive voltage spikes that occur when inductive loads are discharged. Current, caused through negative voltages at the outputs, are compensated up to 50 mA for all outputs in total.

Monitoring and Protective Functions

Each output is monitored (for overload) in its activated status. For the switches 1 to 4 overload is detected, if the switches are activated and the output voltage is higher than 4.1 V for more than 10 µs. The concerned output will be shutdown and both status outputs will be set. The switch can only be activated again if the corresponding input is switched off and then on again. If the output voltage does not exide 4.1 V, the output is not shutdown and the status outputs are not set, although an overload may occur. The switches 5 and 6 are protected through a SOA-circuit, which is suppressed for at least 10 µs before it can start limiting the overload. The status outputs also monitor openload or shorted load to ground at the switches 5 and 6 in deactivated mode.

All malfunctions have to last longer than 10 µs before an analog signal is applied to the analog status output. If several malfunctions appear simultaniously, the highest voltage level will dominate. In parallel the digital status output will be set.

The IC is also protected against thermal overload. If a chip temperature of typically 155 °C is reached, the status outputs monitor overtemperature. If the temperature continues to increase, the inputs and outputs of the switches 5 and 6 are shutdown. The switches 1 to 4 will not be shutdown, so precaution have to be taken in the application to prevent a further increase of the chiptemperature, which may destroy the IC. After cooling down below 140 °C the overtemperature monitoring will be reseted and the outputs of the switches 5 and 6 can be activated again.

If the minimum supply voltage for function is not maintained, the outputs are deactivated. At a supply voltage of higher than 2 V, the outputs are switched to a preferred state regardless of the level of the preferred state input (PREFST) at pin14. Above a supply voltage of typically 3 V (max. 4 V) the preferred state is controlled only by pin 14. For supply voltage of 5 V ± 5 % the full function is guaranteed.

Absolute Maximum Ratings

T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 1	10	V	–
Supply voltage load circuit	V_{Q1-6}	– 0.7	25	V	–
Input voltage	V_{IN1-6}, V_{PREFST}	0	20	V	–
Currents					
Output current	I_{Q1-6}	–	–	–	limited internally
Current at reverse poling	I_{Q5-6}	– 500	–	mA	–
Current at reverse poling	I_{Q1-4}	– 50	–	mA	–
Clamping current	I_{QZ5-6}	–	700	mA	see diagram
Clamping current	I_{QZ1-4}	–	70	mA	–
Junction temperature	T_j	– 40	150	°C	Temperature protection shuts down at 165 °C
Storage temperature	T_{stg}	– 55	125	°C	–
Operating Range					
Supply voltage	V_S	4.72	5.25	V	–
	V_S	4	–	–	full function, but status outputs cannot be evaluated
Output voltage	V_Q	– 0.3	24	V	–
Ambient temperature	T_A	– 40	110	°C	$T_j \leq 150$ °C
Invert current for Q_{1-6} in total	I_{sup}	50	–	mA	–
Input voltage	V_{IN}	– 5	15	V	–
Thermal resistance					
junction to case	$R_{th\ JC}$	–	15	K/W	1)
junction to ambient	$R_{th\ JA}$	–	55	K/W	–

1) Pins 5 to 8 and 17 to 20 have to be connected to the ground-plane used as thermal heatsink to achieve the optimum thermal resistance.

Characteristics

V_S = 5 V, unless stated otherwise; T_A = – 25 to 140 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Voltage (V_S)						
Quiescent current	I_S	–	8	11	mA	Outputs OFF
Supply Current	I_S	–	50	60	mA	Outputs ON
Inputs (IN1-4, PREFST)						
H-input voltage	V_{IH}	1.3	1.8	2.1	V	pin 1, 2, 3, 4, 9, 10, 14
L-input voltage	V_{IL}	0.9	1.2	1.5	V	pin 1, 2, 3, 4, 9, 10, 14
Hysteresis	ΔV_I	0.3	0.6	1.0	V	pin 1, 2, 3, 4, 9, 10, 14
H-input current	I_{IH}	– 10	–	3	µA	0.2 V < V_I < 2.5 V
L-input current	$-I_{IL}$	– 1	–	3	µA	0 V < V_I < 2.5 V; V_S = 0 V
Power Outputs (Q1-6)						
Load Current	I_{Q1-4}	50	–	–	mA	V_S = 2 V (preferred state)
Saturation voltage	$V_{QSat5,6}$	–	0.5	0.8	V	I_Q = 0.4 A; output ON
Saturation voltage	$V_{QSat1-4}$	–	0.5	0.8	V	I_Q = 60 mA; output ON
Saturation voltage	$V_{QSat1-4}$	–	0.4	0.6	V	I_Q = 50 mA; output ON
Saturation voltage	$V_{QSat1-4}$	–	–	0.22	V	I_Q = 20 mA; output ON
Compare voltage	V_{com}	4.1	–	4.7	V	V_S – 0.9 V
Turn-ON delay time	t_{DON}	0.2	1	1.5	µs	see diagrams
Turn-OFFdelay time	t_{DOFF}	0.2	1	1.5	µs	see diagrams; $I_Q = I_{max}$
Turn-OFF delay time	t_{DOFF}	–	2	3.5	µs	I_{Q1-4} = 20 mA
Overtemp. Protection						
Monitoring threshold	T_{thSt}	150	155	–	°C	–
Shutdown threshold	T_{tho}	5	10	–	K	–
hysteresis only switches 5 and 6						
Reset threshold	T_{thRes}	140	–	150	°C	after shutdown

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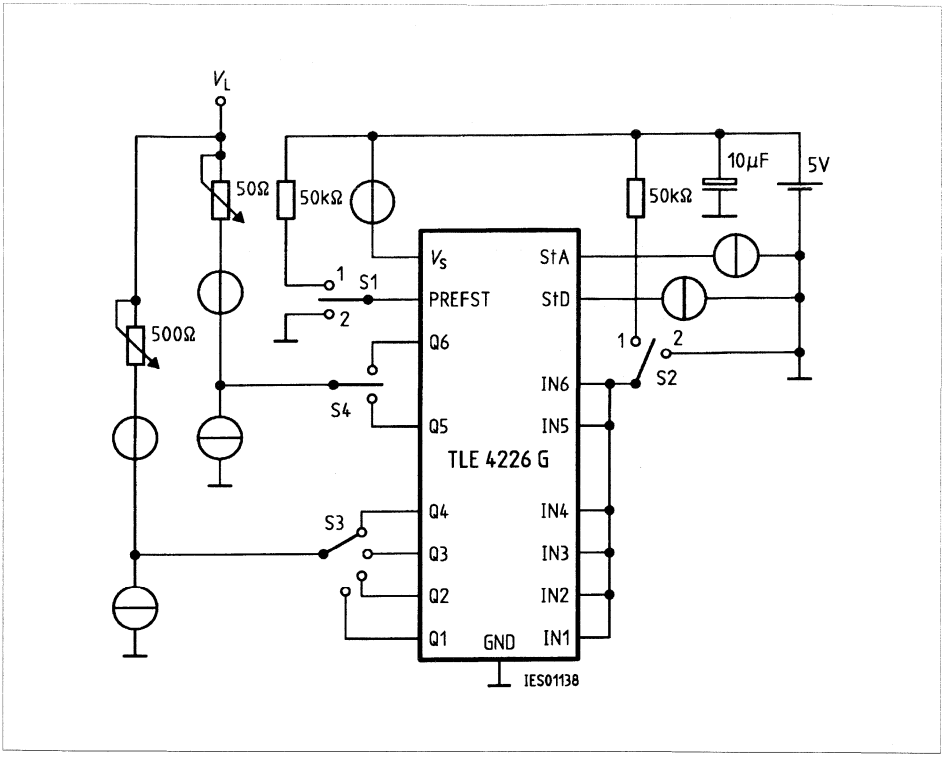
Characteristics (cont'd)

V_S = 5 V, unless stated otherwise; T_A = – 25 to 140 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Outputs (Q1-6)						
Clamping voltage	$V_{Q1\text{-}4}$	25.5	–	33	V	I_Q = 50 mA
Clamping voltage	$V_{Q5,\,6}$	25.5	–	35	V	I_Q = 500 mA
Shorted load current	$I_{Q1\text{-}4\ max}$	60	–	100	mA	V_Q < 16.5 V
Shorted load current	$I_{Q5,\,6}$	500	–	–	mA	$V_Q \leq$ 10 V; $T_j \leq$ 130 °C
Leakage current	$I_{Q1\text{-}4}$	–	–	1	µA	switches off, V_Q = 24 V T_j = 125 °C, $V_i \leq$ 0.9 V
	$I_{Q5,\,6}$	–	–	200	µA	switches off, V_Q = 16.5 V T_j = 125 °C, $V_i \leq$ 0.9 V
Status Output Analog (StA)						
Normal function	V_{StA}	–	–	0.5	V	–
Overload output 6	V_{StA}	1.0	–	1.3	V	–
Overload output 5	V_{StA}	1.4	–	1.7	V	–
Overload output 4	V_{StA}	1.8	–	2.1	V	–
Overload output 3	V_{StA}	2.2	–	2.5	V	–
Overload output 2	V_{StA}	2.6	–	2.9	V	–
Overload output 1	V_{StA}	3.0	–	3.3	V	–
Thermal overload	V_{StA}	3.5	–	–	V	–
Sorce resistance of analog status output	R_{QStA}	50	–	150	Ω	– I_{QStA} = 50 ... 100 µA
Delay time of status	t_{dStA}	10	–	20	µs	overload at switches 5 and 6
Delay time of protection	$t_{dSQ1\text{-}6}$	10	–	20	µs	–
Status Output Digital (StD)						
Pull-up resistance	R_{StD}	–	20	–	kΩ	–
Saturation voltage	V_{SatStD}	–	–	0.4	V	I_{StD} = 5 mA



Test Circuit

S1 in position 1: all outputs can be activated (position 1) or deactivated (position 2) by S2

S1 in position 2: preferred state

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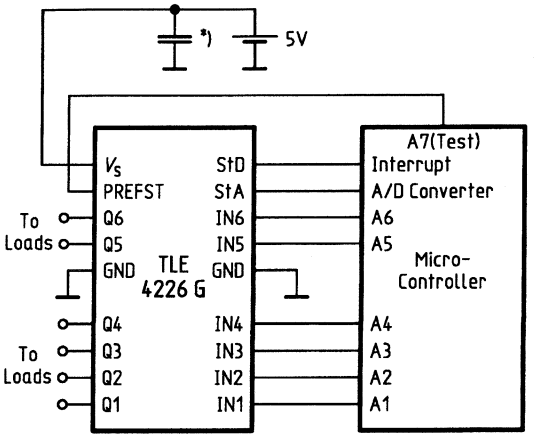
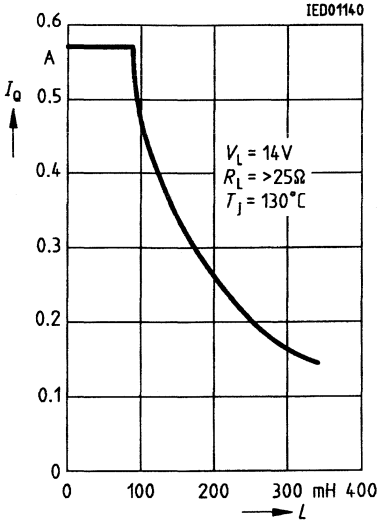


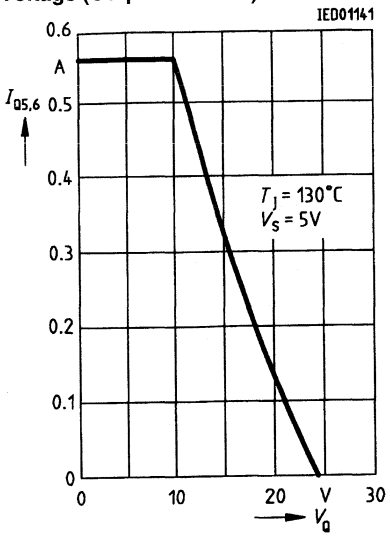
Application Circuit

*) The capacitance depends on the inductance and current load of the supply.

Permissible Load Inductance versus Load Current



Shorted Load Current $I_{Q5,6}$ versus Output Voltage (Outputs 5 and 6)



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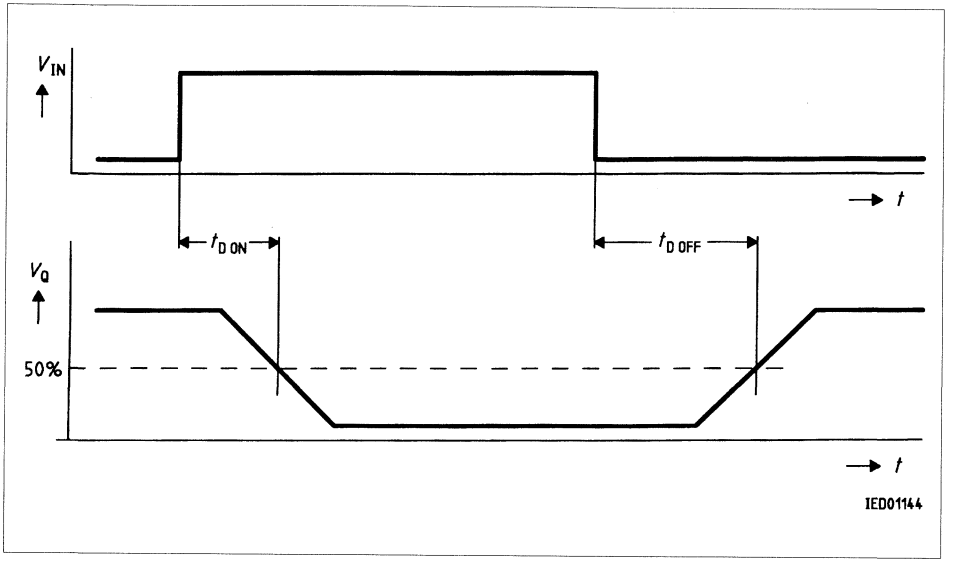
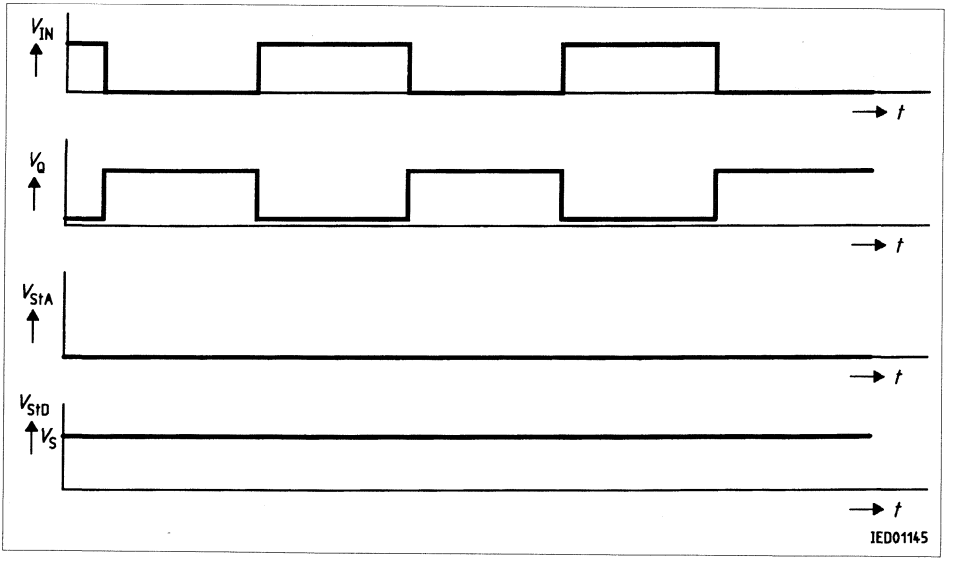
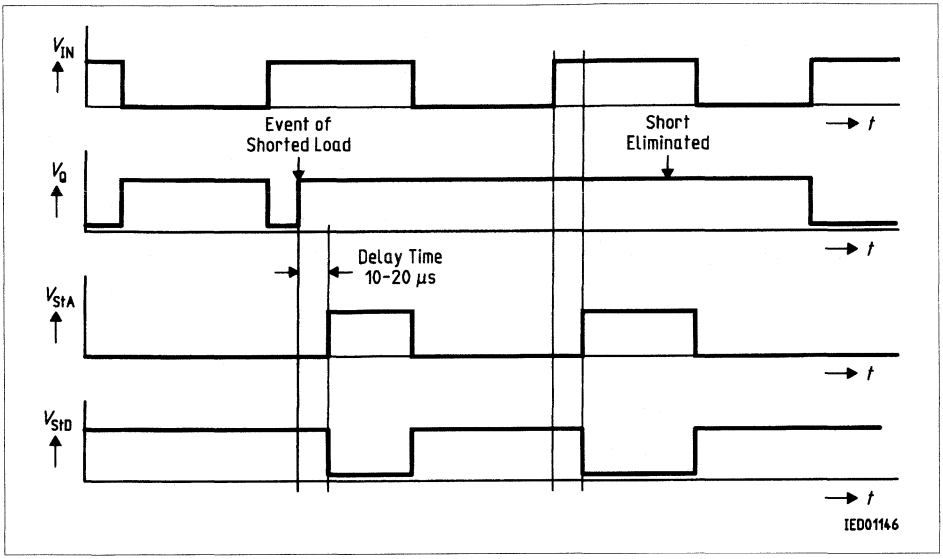
Note:
While switching the maximum inductive loads, the maximum temperature T_j of 150 °C may be briefly exceeded. The IC will not be destroyed by this, but the restrictions concerning useful life should be observed.



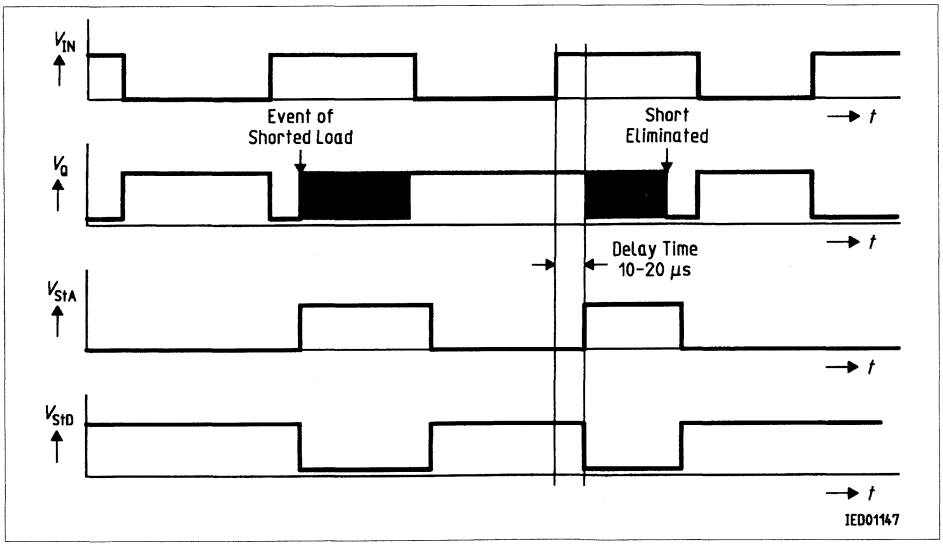
Timing Diagrams



Signals of Inputs and Outputs of Switches 1 to 6
Normal Function (no Error)



Signals of Inputs and Outputs of Switches 1 to 4
Shorted Load to Supply Voltage of Load Circuit



Signals of Inputs and Outputs of Switches 5 and 6
Shorted Load to Supply Voltage of Load Circuit

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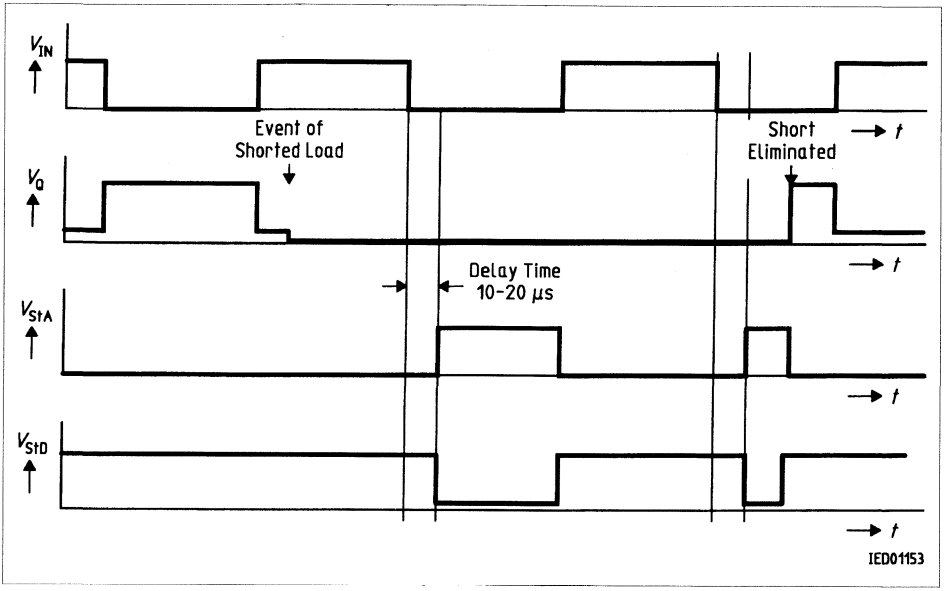


Signals of Inputs and Outputs of Switches 5 and 6
Shorted Load to Ground

ICs für Sensoranwendungen:
Hall-ICs, Näherungsschalter-ICs

ICs for Sensors: Hall-Effect ICs,
ICs for Proximity Switches

Type	Description	Main Application
TLE 4904 F	Unipolar magnetic field	Contactless ignition, limit switch, position detection
TLE 4905 L	Unipolar magnetic field	Low cost applications
TLE 4934 F	Alternating magnetic field	Speed measurement, position detection
TLE 4944 F	Alternating magnetic field	Speed measurement, position detection
TLE 4935 L	Alternating magnetic field	Low cost applications, electr. communication
TLE 4920 G	Differential Hall IC, dynamic	Toothed wheel sensor for rotation and position detection (i.e. ABS, Transmission, Crankshaft)
TLE 4921 U	Differential Hall IC, dynamic	
TLE 4922 U	Differential Hall IC, dynamic	
TLE 4971 U	Differential Hall IC, static	Position switch and toothed wheel sensor (limit switch, camshaft, ABS)
HKZ 121	Hall-Effect-Vane-Switch	Position, timing

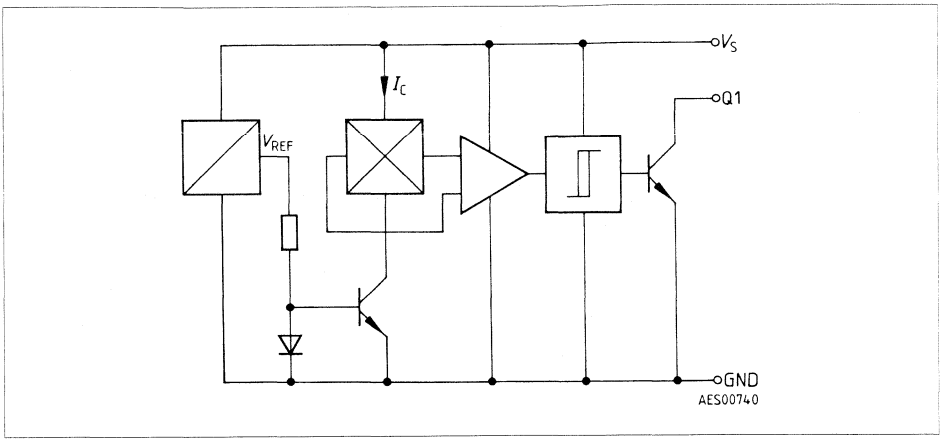
Selector Guide

Type	Package	Temperature Range °C	Supply Voltage V	Output Current mA	Magnetic Switching Thresholds B OPmax / B RP min [mT]	Page
TLE 4904 F	P-SSO-3-4	– 40 ... 150	4.3 ... 24	50	39 / 23	777
TLE 4905 L	P-SSO-3-2	– 40 ... 150	3.5 ... 24	50	20 / 5	788
TLE 4934 F	P-SSO-3-4	– 40 ... 150	4.3 ... 24	50	15 / – 15	777
TLE 4944 F	P-SSO-3-4	– 40 ... 150	4.3 ... 24	50	8 / – 8	777
TLE 4935 L/ LS	P-SSO-3-2/ 3-3	– 40 ... 150	3.5 ... 24	50	20 / – 20	788
TLE 4920 G	P-DSO-8-1	– 40 ... 150	4.5 ... 24	50	0 / 1.5 [1]	795
TLE 4921 U	P-SSO-4	– 40 ... 150	4.5 ... 24	50	0 / 1.5 [1]	795
TLE 4922 U	P-SSO-4	– 40 ... 150	4.5 ... 24	50	1.5 / 0 [1]	795
TLE 4971 U	P-SSO-4	– 40 ... 150	4.5 ... 24	50	7.5 / 5 [1]	813
HKZ 121	Special	– 40 ... 130	4.5 ... 24	40		829

[1] delta B typ. [mT]

= SMD

Schematic Circuit Diagrams



Digital Hall-Effect IC

On a semiconductor crystal the contactless, magnetically controlled switches contain a constant voltage regulator, a regulated voltage source for the Hall generator, a differential amplifier, a Schmitt trigger, two driver stages, and an end transistor with open collector. Their use is of advantage when high reliability, no bounce pulses, insensitivity to dirt and corrosion, and a long service life are required.

Selector Guide

Type	Package	Output Current mA	Current Consumption mA	Supply Voltage V	Feature	Page
TCA 305 A	P-DIP-14-1	50	1.0	5 to 30	Temporarily short-circuit proof	835
TCA 305 G	P-DSO-14-1	50	1.0	5 to 30	Temporarily short-circuit proof	835
TCA 355 B	P-DIP-8	50	1.0	5 to 30	Temporarily short-circuit proof	835
TCA 355 G	P-DSO-8-1	50	1.0	5 to 30	Temporarily short-circuit proof	835
TCA 505 B	P-DIP-16	60	0.75	3.1 to 4.5/ 4 to 40	Short-circuit protection	842
TCA 505 BG	P-DSO-16-1	60	0.75	3.1 to 4.5/ 4 to 40	Short-circuit protection	842
TCA 705 G	P-DSO-16-1	500	0.75	7.5 to 65	High-power output	860

= SMD

Integrated Hall-Effect Switches for Unipolar and Alternating Magnetic Fields

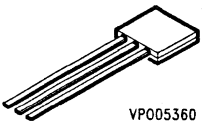
TLE 4904, TLE 4934
TLE 4944

Preliminary Data

Bipolar-IC

Features

- Digital output signal
- For unipolar and bipolar magnetic fields
- Large temperature range
- High temperature stability
- High switching accuracy
- Protection against overvoltage
- Protection against reversed polarity
- Output protection against electrical disturbances



P-SSO- 3-4

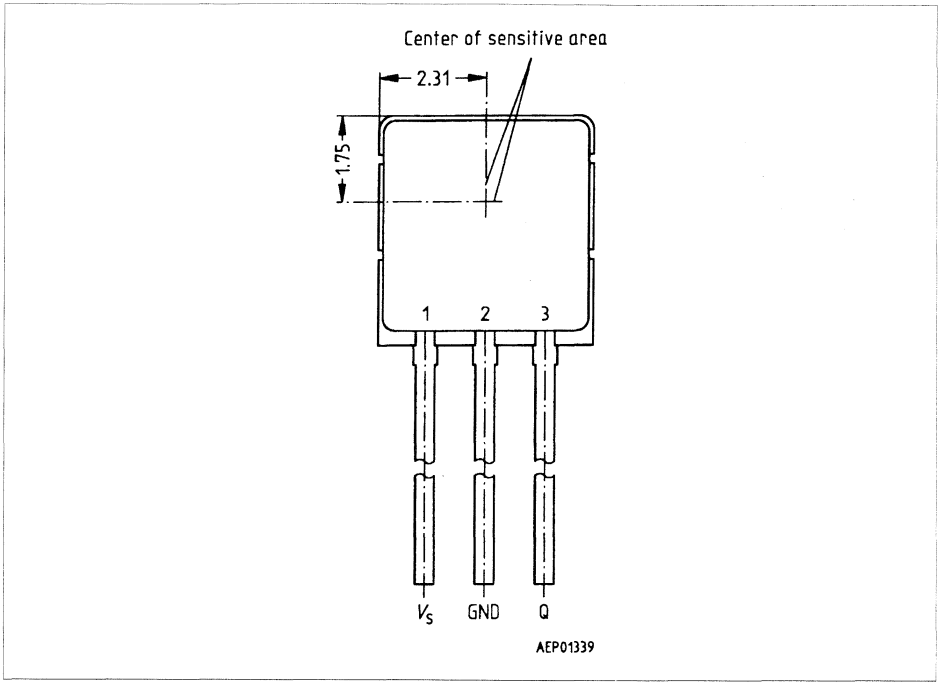
	Type	Ordering Code	Package
▼	TLE 4904 F	Q67006-A9011	P-SSO-3-4
▼	TLE 4934 F	Q67006-A9027	P-SSO-3-4
▼	TLE 4944 F	Q67006-A9028	P-SSO-3-4

▼ New type

TLE 4904 F (Unipolar Magnetic Fields - Switch) and the TLE 4934 F, TLE 4944 F (Bipolar Magnetic Fields - Latch/Switch) are integrated circuit Hall sensors designed specifically for automotive and industrial electronics. Precise switching points and high temperature stability are achieved by adjustment and compensation on chip.

These Hall effect integrated circuits include protection for overvoltage, reversed polarity and electrical overstress such as load dump, etc., in accordance with ISO-TR 7637 and DIN 40 839.

12



Pin Configuration

Pin Definition and Functions

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

Circuit Description

The circuit includes Hall generator, amplifier and Schmitt trigger on one chip.

The internal reference provides the supply voltage for the components. A magnetic field perpendicular to the chip surface induces a voltage at the hall probe. This voltage is amplified and switches a Schmitt-trigger with open-collector output.

The switching points are adjusted to achieve high accuracy. To increase temperature influence, compensation circuitry is integrated.

Protection is provided at the input/supply (pin 1) for overvoltage and reverse polarity and against overstress such as load dump, etc., in accordance with ISO-TR 7637 (DIN 40839). The output (pin 3) is protected against voltage peaks and electrical disturbances.

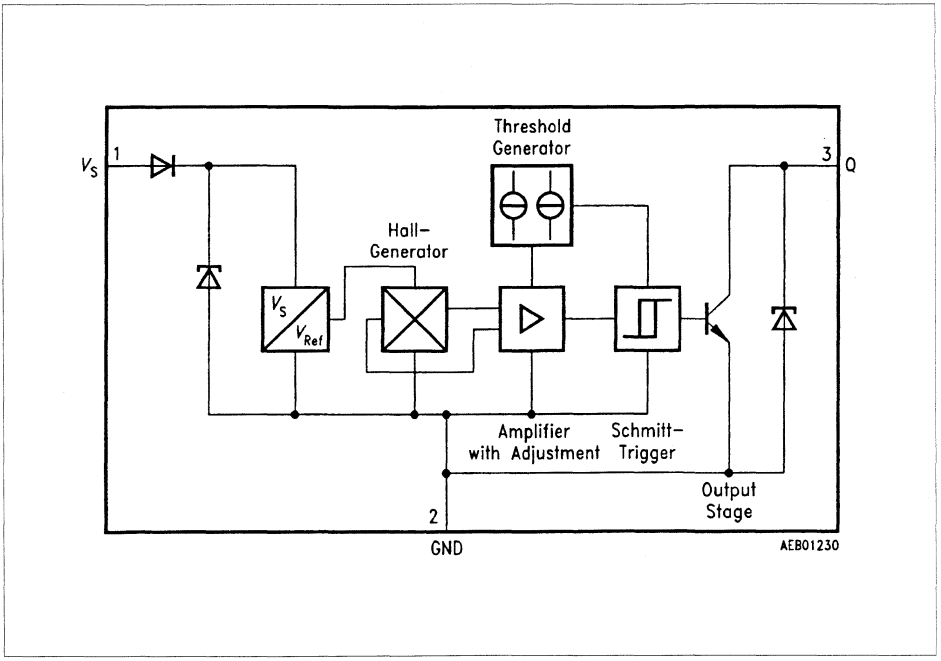


Figure 1
Block Diagram

12

Functional Description

When a positive magnetic field is applied in the indicated direction (**figure 2**) and the turn-ON magnetic induction B_{OP} is exceeded, the output of the Hall-effect IC will conduct (Operate Point). When the current is reduced (TLE 4904 F) or a reverse magnetic field is generated (TLE 4934 F, TLE 4944 F), the output of the IC turns OFF (Release Point) (**figures 3 and 4**).

B_{RP} and B_{OP} are the critical parameters in most unipolar and bipolar Hall-switch applications. For this reason the switching points are adjusted.

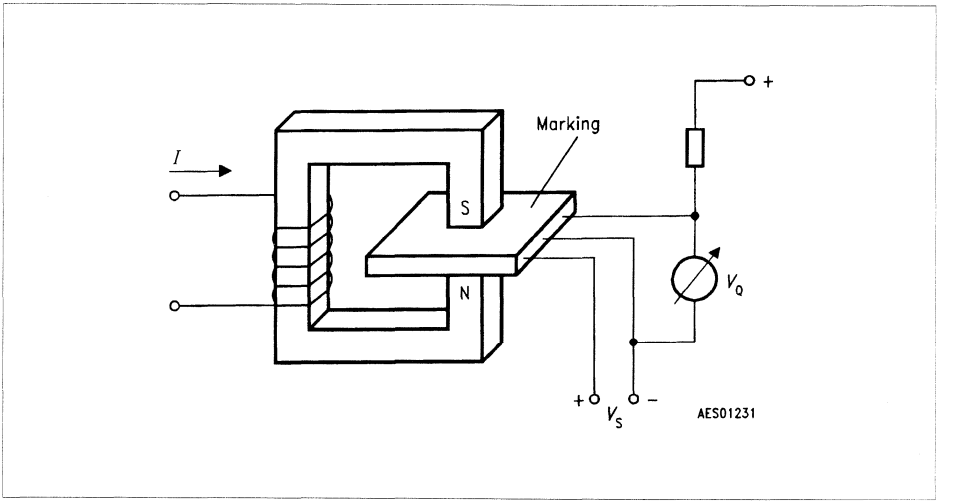


Figure 2
Sensor/Magnetic-Field Configuration

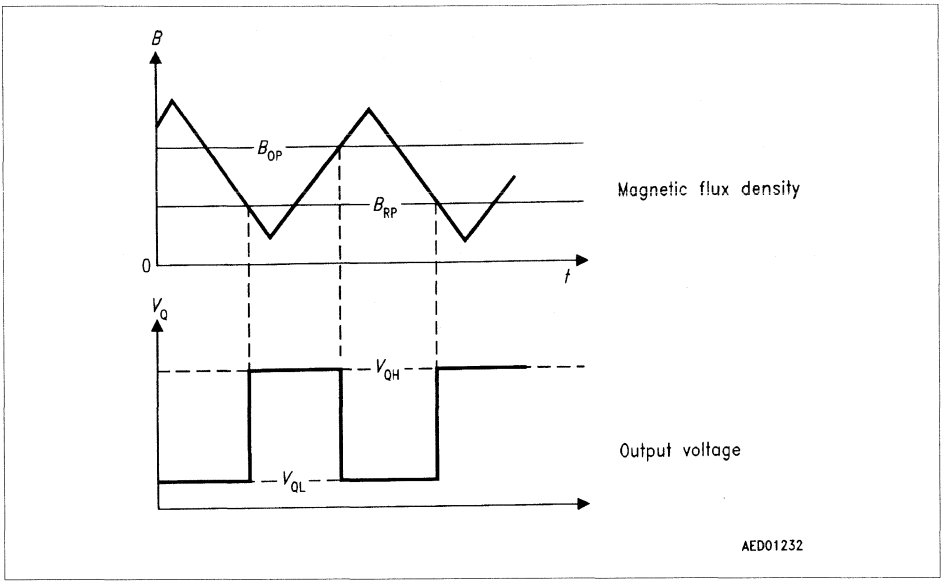


Figure 3
Switching Characteristics TLE 4904 F

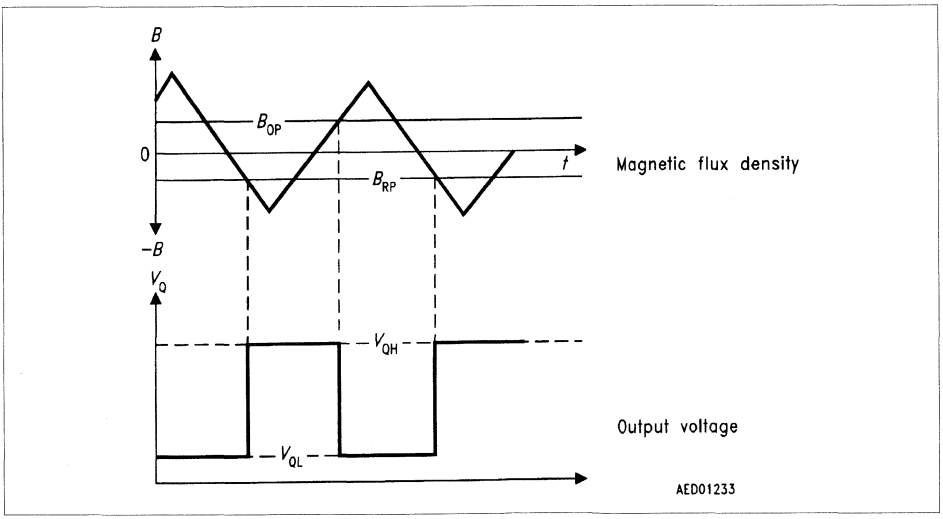


Figure 4
Switching Characteristics TLE 4934 F, TLE 4944 F

12

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 40	27	V	–
Output voltage	V_Q	–	27	V	–
Output current	I_Q	–	50	mA	–
Output reverse current	$-I_Q$	–	50	mA	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	–	170	°C	1000 h
Junction temperature	T_j	–	210	°C	40 h
Storage temperature	T_{stg}	– 40	150	°C	–
Thermal resistance	$R_{th\,JA}$	–	240	K/W	–
Current through input-protection device	I_{SZ}	– 200	200	mA	t < 2 ms; v = 0.1
Current through output-protection device	I_{QZ}	– 200	200	mA	t < 2 ms; v = 0.1

Electro Magnetic Compatibility

ref. DIN 40839 part 1;
test circuit 1

Testpulse 1	V_{LD}	– 100	–	V	t_d = 2 ms
Testpulse 2	V_{LD}	–	100	V	t_d = 0.05 ms
Testpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testpulse 4	V_{LD}	– 7	–	V	$t_d \leq$ 20 s
Testpulse 5	V_{LD}	–	120	V	t_d = 400 ms

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	4.3	24	V	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	– 40	170	°C	1000 h
Junction temperature	T_j	– 40	210	°C	40 h

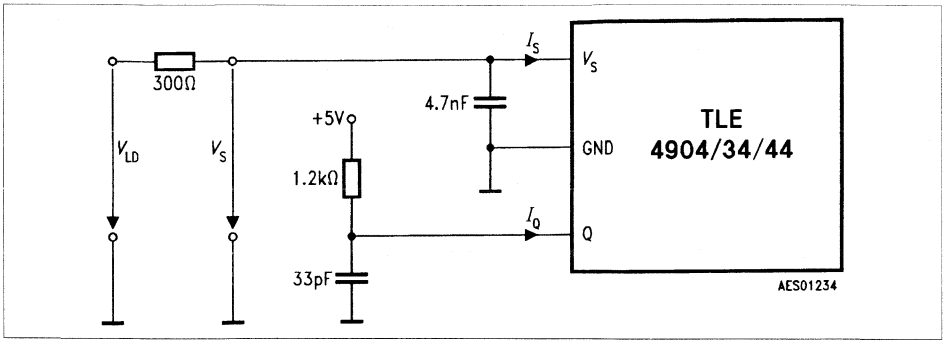
Electro Magnetic Compatibility
ref. DIN 40839 part 1;
test circuit 1

Testpulse 2	V_{LD}	–	100	V	t_d = 0.05 ms
Testpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testpulse 4	V_{LD}	– 7	–	V	t_d = 130 ms
Testpulse 5	V_{LD}	–	120	V	t_d = 400 ms

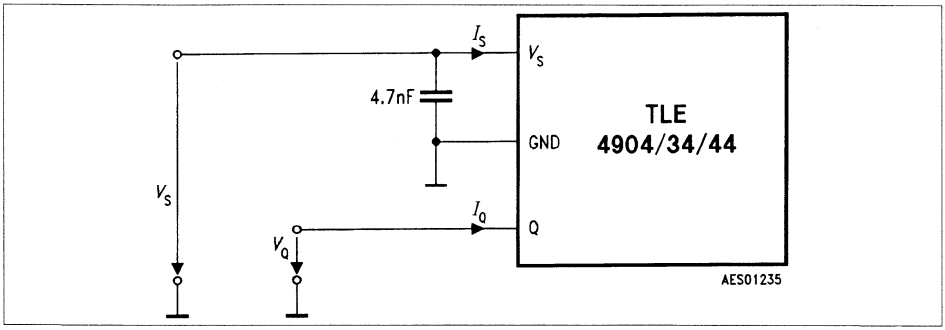
AC/DC Characteristics

4.5 V ≤ V_S ≤ 24 V; – 40 °C ≤ T_j ≤ 150 °C

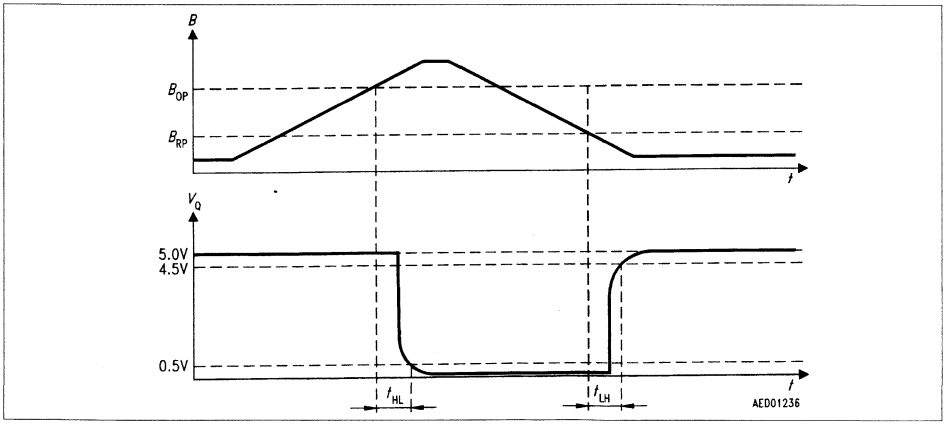
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current	I_S	–	–	9.5	mA	B < B_{RP}	1
	I_S	–	–	10	mA	B > B_{OP}	1
Output saturation voltage	V_{QSat}	–	0.2	0.6	V	I_Q = 40 mA	2
Output leakage current	I_{QL}	–	–	10	µA	V_Q = 24 V	2
Overvoltage protection							
– at supply voltage	V_{SZ}	27	–	35	V	I_S = 16 mA	2
– at output	V_{QZ}	27	–	35	V	I_Q = 16 mA	2
Delay time	t_{HL} / t_{LH}	–	–	15	µs	–	1
Magnetic Parameters							
TLE 4904 F							
Turn-ON induction	B_{OP}	33	36	39	mT	–	1
Turn-OFF induction	B_{RP}	23	26	29	mT	–	1
Hysteresis (B_{OP} - B_{RP})	B_{Hy}	7	10	14	mT	–	1
TLE 4934 F							
Turn-ON induction	B_{OP}	10	12.5	15	mT	–	1
Turn-OFF induction	B_{RP}	– 15	– 12.5	– 10	mT	–	1
Hysteresis (B_{OP} - B_{RP})	B_{Hy}	20	25	30	mT	–	1
TLE 4944 F							
Turn-ON induction	B_{OP}	– 1	3.5	8	mT	–	1
Turn-OFF induction	B_{RP}	– 8	– 3.5	1	mT	–	1
Hysteresis (B_{OP} - B_{RP})	B_{Hy}	4	7	10	mT	–	1
Drift of switching points							
After temp. storage	ΔB	–	–	± 3	mT	–	–
After temp. cycling	ΔB	–	–	± 3	mT	–	–
After humidity	ΔB	–	–	± 3	mt	–	–



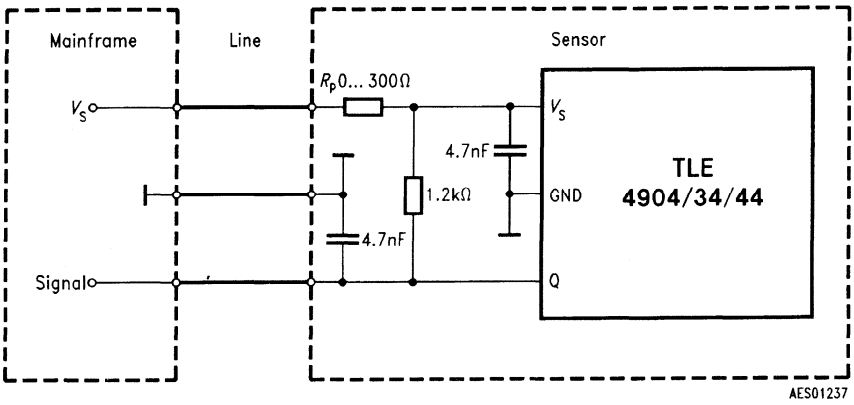
Test Circuit 1



Test Circuit 2

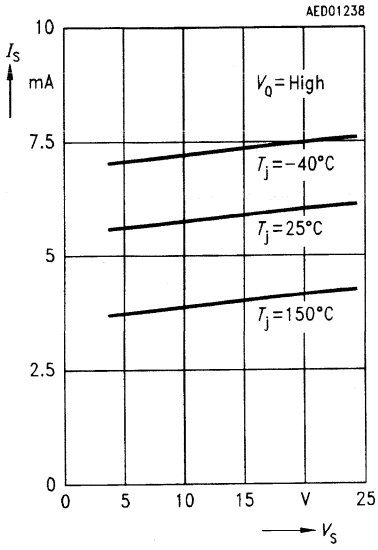


Diagram

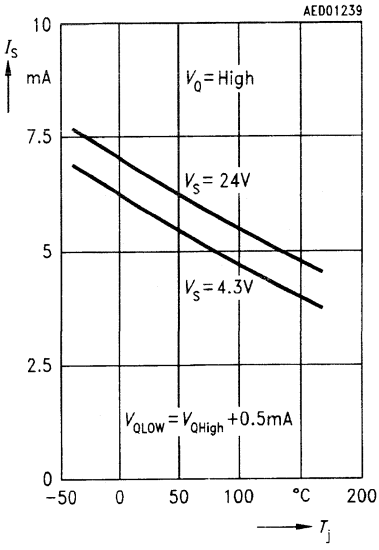


Application Circuit

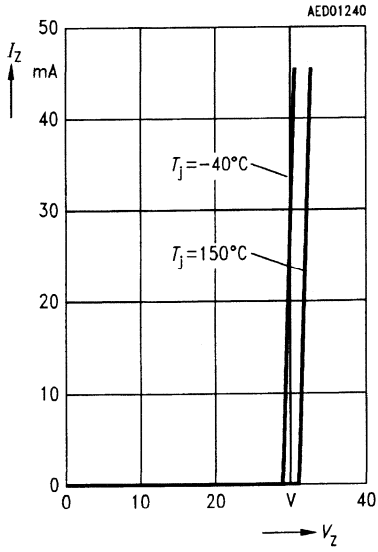
Quiescent Current versus Supply Voltage



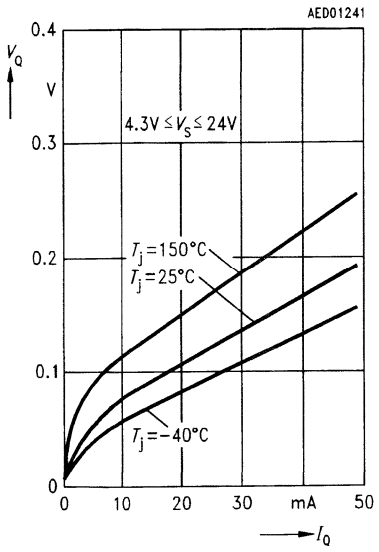
Quiescent Current versus Junction temperature



Current through Protection Device versus Voltage



Saturation Voltage versus Output Current



12

SIEMENS

Special Economic Hall-Effect IC for Low-Cost Magnetic Field Applications

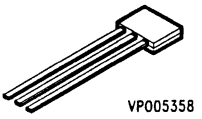
TLE 4905
TLE 4935

Preliminary Data

Bipolar-IC

Features

- Low price
- Digital output signal
- For unipolar and alternating magnetic fields
- Large temperature range
- Protection against reversed polarity
- Output protection against electrical disturbances



P-SSO-3-2

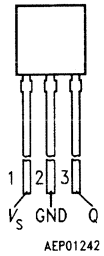
	Type	Ordering Code	Package
▼	TLE 4905 L	Q67006-A9120	P-SSO-3-2
▼	TLE 4935 L/LS	Q67006-A9112	P-SSO-3-2/3-3

▼ = New type

TLE 4904 F (Unipolar/Bipolar Magnetic Fields Switches) have been designed specifically for low cost automotive and industrial applications which do not require overvoltage protection. reverse polarity protection is included on-chip as is output protection against negative voltage transients.

These devices are ideal for systems where low cost and high reliability are the key factors.

Typical applications are position/proximity indicators, brushless DC motor commutation, rotational indexing etc.



Pin Configuration

Pin Definitions and Funtions

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output

Circuit Description

The circuit includes Hall generator, amplifier and Schmitt-Trigger on one chip. The internal reference provides the supply voltage for the components. A magnetic field perpendicular to the chip surface induces a voltage at the hall probe. This voltage is amplified and switches a Schmitt-trigger with open-collector output. A protection diode against reverse power supply is integrated. The output is protected against electrical disturbances.

For critical applications requiring higher switching accuracy, fully protected Hall ICs the Siemens TLE 4904 (switch) and TLE 4934/44 (latch/switch) are recommended.

12

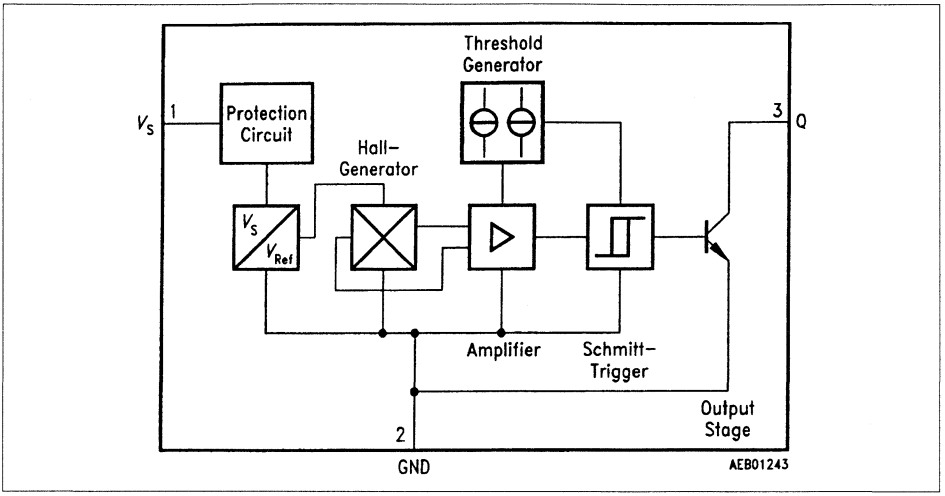


Figure 1
Block Diagram

Absolute Maximum Ratings

T_A = – 40 to 125 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 40	28	V	–
Output voltage	V_Q	–	28	V	–
Output current	I_Q	–	50	mA	–
Output reverse current	$-I_Q$	–	50	mA	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	–	170	°C	1000 h
Junction temperature	T_j	–	210	°C	40 h
Storage temperature	T_{stg}	– 50	150	°C	–
Thermal resistance	$R_{th\ JA}$	–	240	K/W	–

Operating Range

Supply voltage	V_S	3.5	24	V	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	– 40	170	°C	1000 h
Junction temperature	T_j	– 40	210	°C	40 h

AC/DC Characteristics

3.5 V ≤ V_S ≤ 24 V; – 40 °C ≤ T_j ≤ 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current	I_{SHigh}	–	3	7	mA	B < B_{RP}	1
	I_{SLow}	–	4	8	mA	B > B_{OP}	1
Output saturation voltage	V_{QSat}	–	0.25	0.5	V	I_Q = 40 mA	1
Output leakage current	I_{QL}	–	–	10	µA	V_Q = 24 V	1
Rise/fall time	t_r/t_f	–	–	1	µs	R_L = 1,2 kΩ C_L ≤ 33 pF	1
Magnetic Parameters							
TLE 4905 L							
Turn-ON induction	B_{OP}	–	–	20	mT	–	1
Turn-OFF induction	B_{RP}	5	–	–	mT	–	1
Hysteresis (B_{OP}-B_{RP})	ΔB_{Hy}	2	3	–	mT	–	1
TLE 4935 L							
Turn-ON induction	B_{OP}	10	–	20	mT	–	1
Turn-OFF induction	B_{RP}	– 20	–	– 10	mT	–	1
Hysteresis (B_{OP}-B_{RP})	ΔB_{Hy}	20	30	–	mT	–	1

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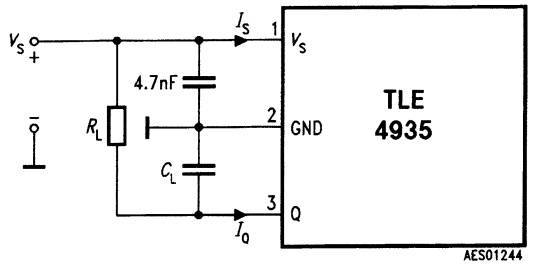
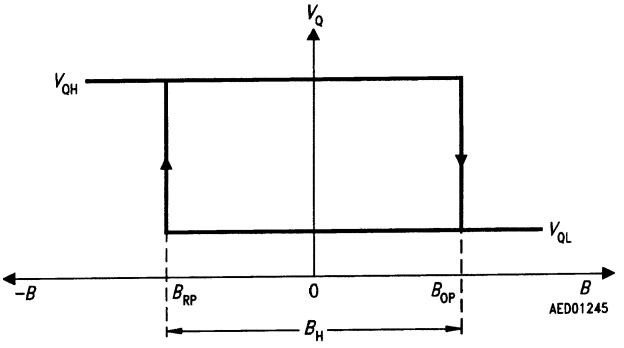
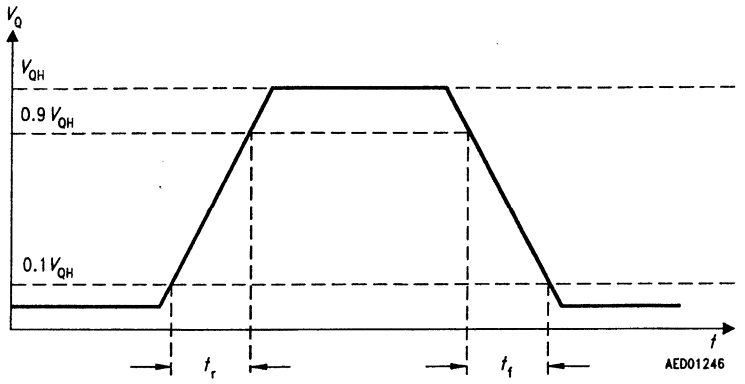
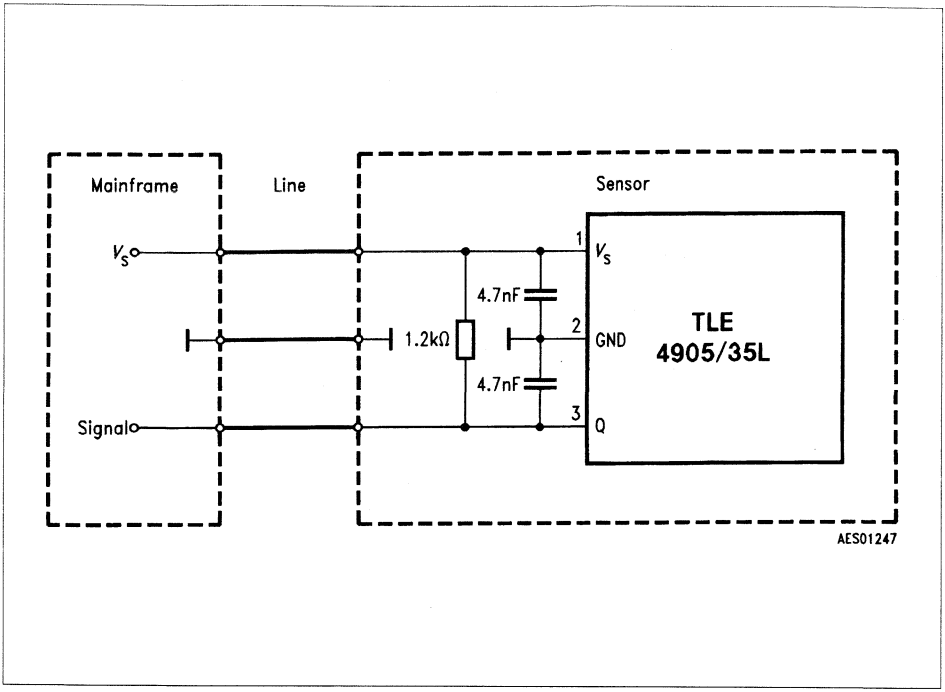






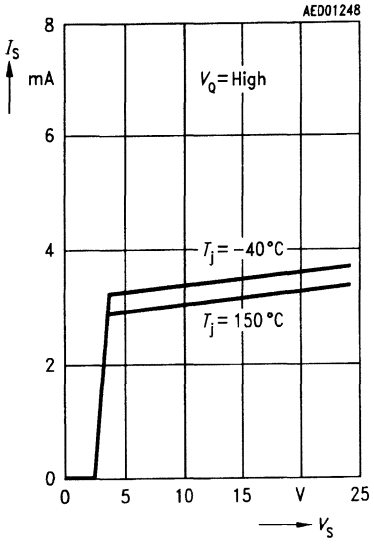
Test Circuit 1



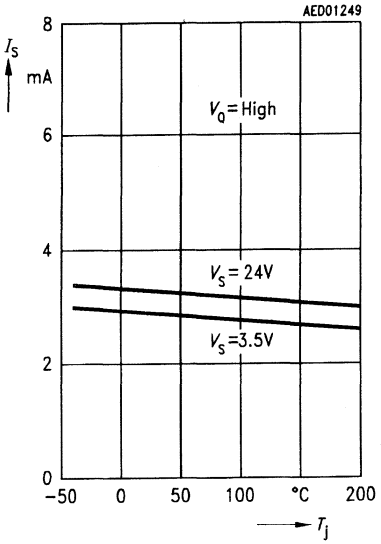
Application Circuit

12

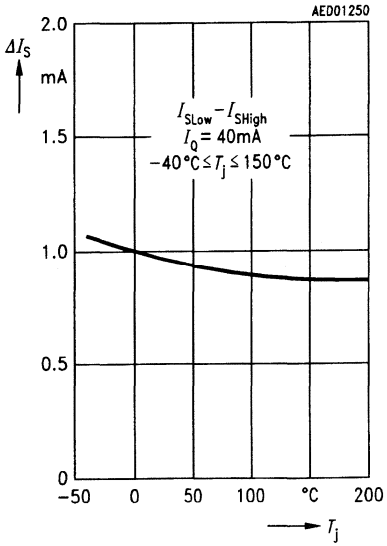
Quiescent Current versus Supply Voltage



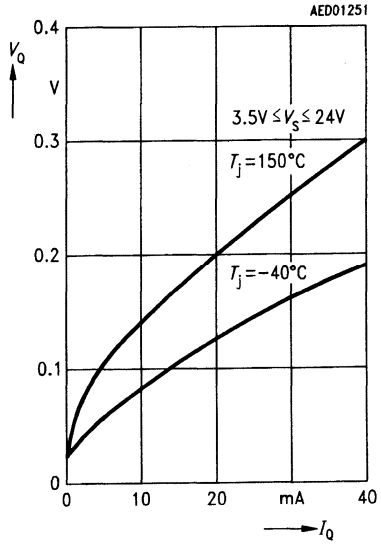
Quiescent Current versus Junction Temperature



Quiescent Current Difference versus Temperature



Saturation Voltage versus Output Current



SIEMENS

Differential Hall Effect Sensor ICs

TLE 4920, TLE 4921 TLE 4922

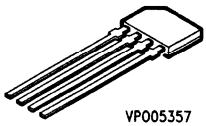
Preliminary Data

Bipolar IC

Features

- AC coupled
- Digital output signal
- Two-wire and three-wire configuration possible
- Large temperature range
- Large distance, low frequency cut-off
- Protection against overvoltage
- Protection against reversed polarity
- Output protection against electrical disturbances

P-DSO-8-1



P-SSO-4

Type	Ordering Code	Package
TLE 4920 G	Q67000-A9000	P-DSO-8-1 (SMD)
▼ TLE 4921 U	Q67006-A9055	P-SSO-4
▼ TLE 4922 U	Q67006-A9122	P-SSO-4

▼ New type

The differential Hall Effect sensors TLE 4920 G/TLE 4921 U/TLE 4922 U are particularly suitable for rotational speed detection and timing applications of ferromagnetic toothed wheels such as anti-lock braking systems, transmissions, crankshafts, etc. The integrated circuit (based on Hall effect) provides a digital signal output with frequency proportional to the speed of rotation. Unlike other rotational sensors differential Hall ICs are not influenced by radial vibration within the effective airgap of the sensor and require no external signal processing.

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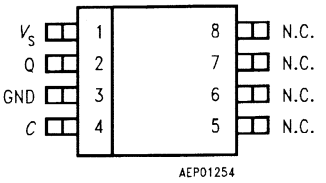
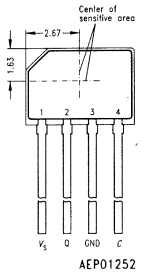
TLE 4920



*) Center of sensitive area is toleranced ±0.10 mm to the center of pin outline

TLE 4921, TLE 4922



Pin Configuration

Pin Definitions and Functions

Pin	Symbol TLE 4920 G	Function
1	V_S	Supply voltage
2	Q	Output
3	GND	Ground
4	C	Capacitor
5	N.C.	Not connected
6	N.C.	Not connected
7	N.C.	Not connected
8	N.C.	Not connected

Pin Definitions and Functions

Pin	Symbol TLE 4921 U	Symbol TLE 4922 U	Function
1	V_S	V_S	Supply voltage
2	Q	$\overline{Q}$	Output
3	GND	GND	Ground
4	C	C	Capacitor

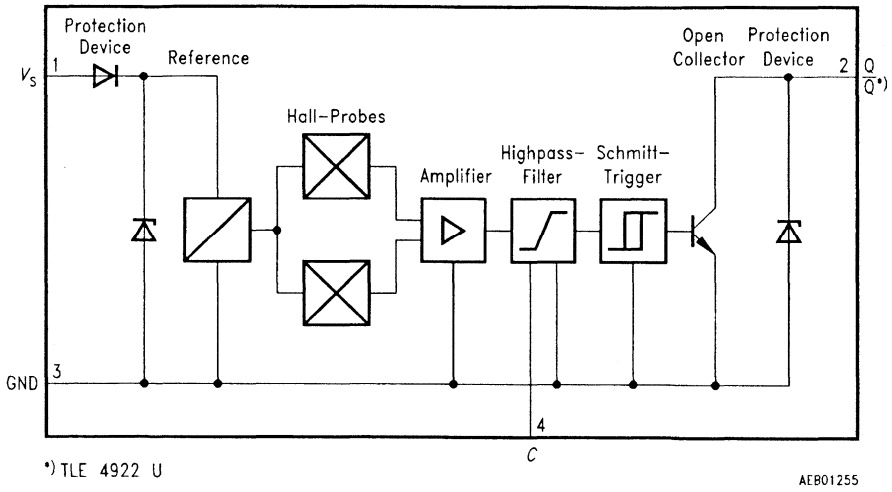


Figure 1
Block Diagram 1

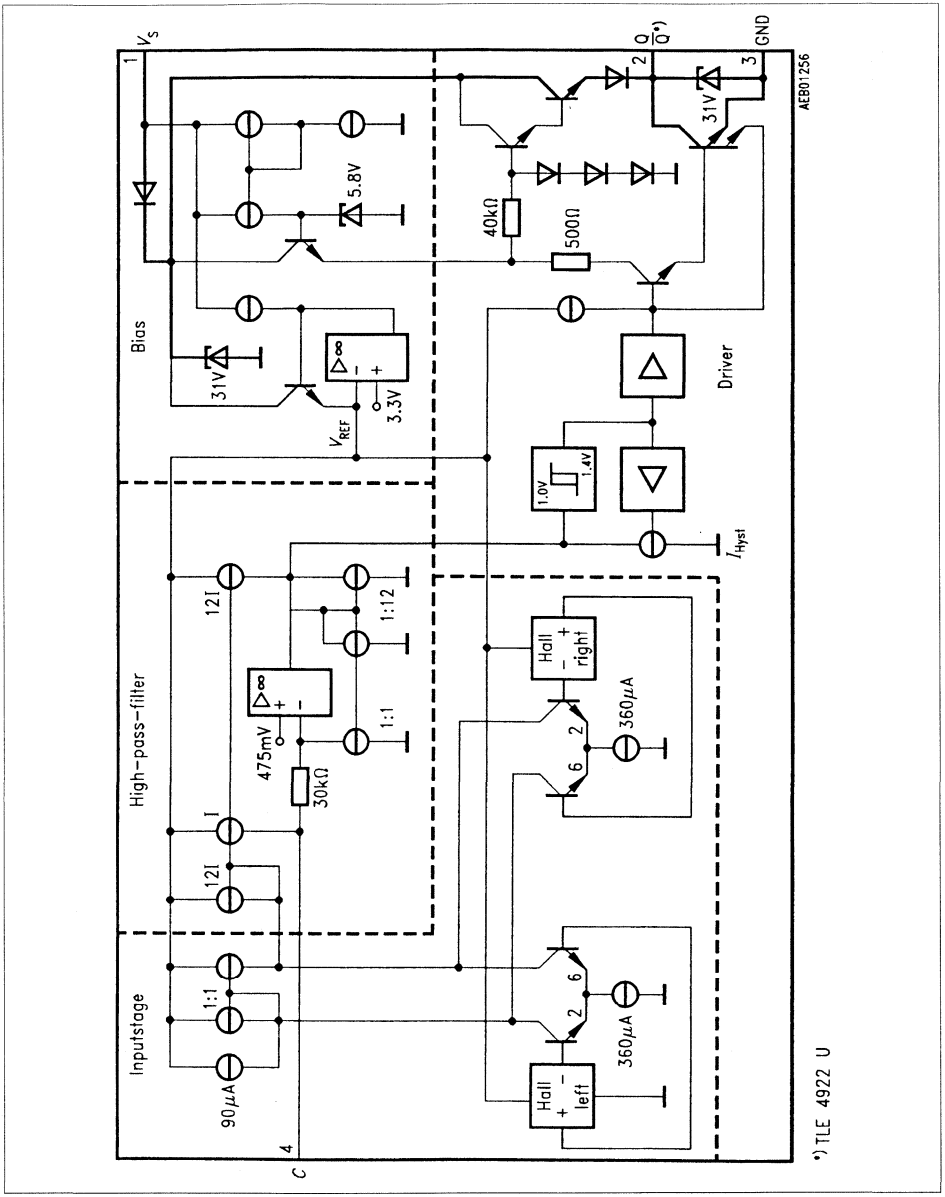


Figure 2
Block Diagram 2

Functional Description

The Differential Hall Sensor IC detects the motion of, and static position of, ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet (southpole of the magnet attached to the back, unmarked, side of the IC package).

Using an external capacitor the generated Hall-voltage signal is slowly adjusted via an active high pass filter with low frequency cutoff. This causes the output to switch into a biased mode after a time constant is elapsed. The time constant is determined by the external capacitor. Filtering avoids aging and temperature influence from Schmitt-trigger input and eliminates device and magnetic offset.

The TLE 4920 G/TLE 4921 U/TLE 4922 U can be exploited to detect toothed wheel rotation in a rough environment. Jolts against the toothed wheel and ripple have no influence on the output signal. Furthermore the TLE 4920 G/TLE 4921 U/TLE 4922 U can be operated in a two-wire - as well as in a three-wire-configuration.

The output is logic compatible by high/low levels regarding on and off.

TLE 4922 U provides an inverted output signal.

Circuit Description

The TLE 4920 G/TLE 4921 U/TLE 4922 U is comprised of a supply voltage reference, a pair of Hall probes spaced at 2.5 mm, differential amplifier, Schmitt trigger, and open collector output.

Protection is provided at the input/supply (pin 1) for overvoltage and reverse polarity and against overstress such as load dump, etc., in accordance with ISO-TR 7637 and DIN 40839. The output (pin 2) is protected against voltage peaks and electrical disturbances.

Absolute Maximum Ratings

T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Units	Remarks
		min.	max.		
Supply voltage	V_S	– 40	30	V	–
Output voltage	V_Q	– 0.7	30	V	–
Output current	I_Q	–	50	mA	–
Output revers current	$-I_Q$	–	50	mA	–
Capacitor voltage	V_C	– 0.3	3	V	
Junction temperature	T_j	–	150	°C	–
Junction temperature	T_j	–	170	°C	1000 h
Junction temperature	T_j	–	210	°C	40 h
Storage temperature	T_s	– 40	150	°C	–
Thermal resistance					
P-DSO-8-1	$R_{th\,JA}$	–	125	K/W	–
PSSO-4	$R_{th\,JA}$	–	240	K/W	–
Current through input-protection device	I_{SZ}	–	200	mA	t < 2 ms ; ν = 0.1
Current through output-protection device	I_{QZ}	–	200	mA	t < 2 ms ; ν = 0.1

Electro Magnetic Compatibility

ref. DIN 40839 part 1;
test circuit 1

Testpulse 1	V_{LD}	– 100	–	V	t_d = 2 ms
Testpulse 2	V_{LD}	–	100	V	t_d = 0.05 ms
Testpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testpulse 4	V_{LD}	– 7	–	V	$t_d \leq$ 20 s
Testpulse 5	V_{LD}	–	120	V	t_d = 400 ms

Operating Range

Parameter	Symbol	Limit Values		Units	Remarks
		min.	max.		
Supply voltage	V_S	4.5	24	V	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	– 40	170	°C	1000 h
Junction temperature	T_j	– 40	210	°C	40 h
Pre-induction	B_0	0	200	mT	Southpole at the backside of IC

Electro Magnetic Compatibility
ref. DIN 40839 part 1;
test circuit 1

Testimpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testimpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testimpulse 4	V_{LD}	– 7	–	V	$t_d \leq$ 20 s
Testimpulse 5	V_{LD}	–	80	V	t_d = 400 ms

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AC/DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply voltage	–	–	–	–	–	4.5 V ≤ V_S ≤ 24 V	–
Junction temperature	–	–	–	–	–	– 40 °C ≤ T_j ≤ 150 °C	–
Supply current	I_S	3.5	8.5	14	mA	V_Q = high I_Q = 0 mA	1
		4.0	9	14.5	mA	V_Q = low I_Q = 40 mA	1
Output saturation voltage	V_{QSat}	–	0.25	0.6	V	I_Q = 40 mA	1
Output leakage current	I_{QL}	–	–	10	µA	V_Q = 24 V	1
Switching frequency	f	5	–	20000	Hz	C = 470 nF ΔB = 5 mT	2
Switching flux density	ΔB_{OP} [1]	– 1	0	1	mT	f = 100 Hz C = 470 nF	2
Hysteresis	ΔB_{Hy}	0.5	1.5	2.5	mT	f = 100 Hz C = 470 nF	2
Overvoltage protection at supply voltage at output	 V_{SZ} V_{QZ}	 27 27	 – –	 35 35	 V V	 I_S = 16 mA I_S = 16 mA	 2 2

1) is equivalent to ΔB_{RP} of TLE 4922 U

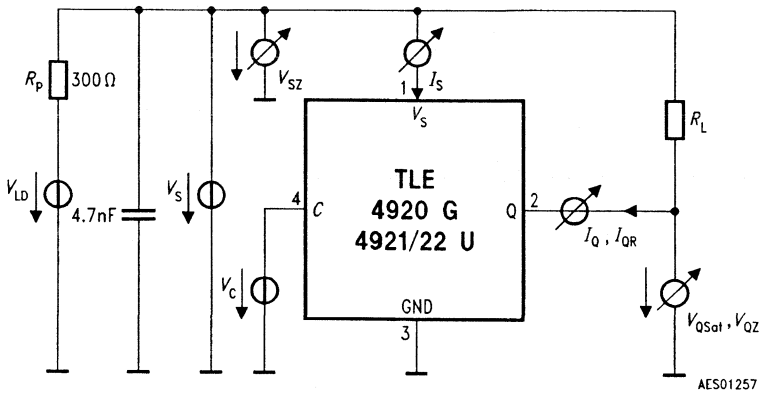
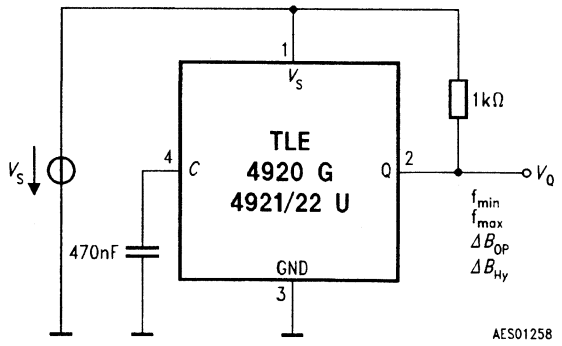


Figure 3
Test Circuit 1



– B_0 = 100 mT; southpole at the back of IC
– tooth wheel with module m = 2 mm
– Distance IC-object L = 1 mm

Figure 4
Test Circuit 2

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Application Notes

Two possible applications are shown in **figure 5 and 6** (Toothed and Magnet Wheel).

The differences between two-wire and three-wire application is shown in **figure 7**.

Gear Tooth Sensing

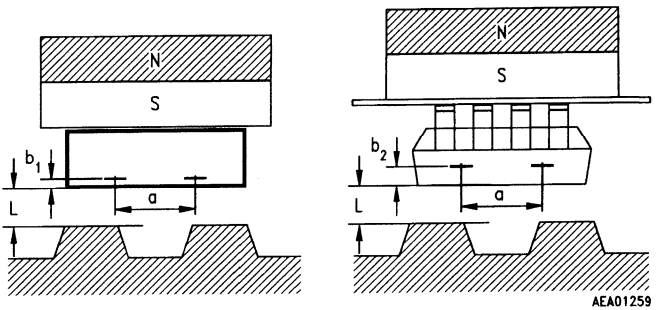
In the case of ferromagnetic toothed wheel application the IC has to be biased by the southpole of a permanent magnet (e.g. SEC_{05} (Vacuumschmelze VX145) with the dimensions 8 mm x 5 mm x 3 mm) which should cover both hall-probes.

The maximum air gap depends on

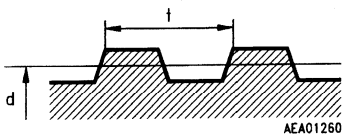
- the magnetic field strength (magnet used),
- the tooth wheel that is used (dimensions, material, etc.),
- the ambient temperature,
- the connected capacitor

a centred distance of hall-probes
b hall-probes to IC surface
L IC surface to tooth wheel

a = 2.5 mm
b_1 = 0.25 mm
b_2 = 0.5 mm



Sensor Spacing



Conversion DIN – ASA
m = 25.4 mm/p
t = 25.4 mm x CP

DIN
d diameter (mm)
z number of teeth
m module m = d/z (mm)
t pitch t = π x m (mm)

ASA
p diametral pitch p = z/d (inch)
PD pitch diameter PD = z/p (inch)
CP circular pitch CP = 1 inch x π/p

Tooth Wheel Dimensions

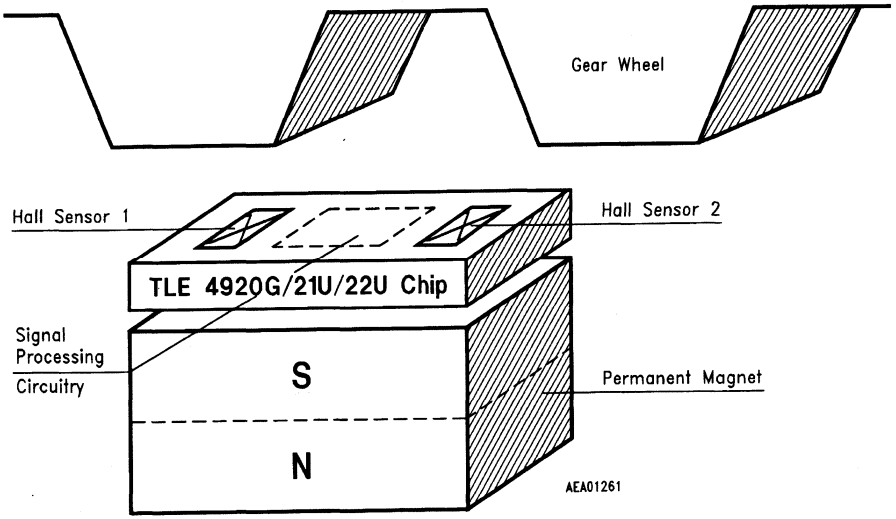


Figure 5
TLE 4920G/4921U/4922U, with Ferromagnetic Toothed Wheel

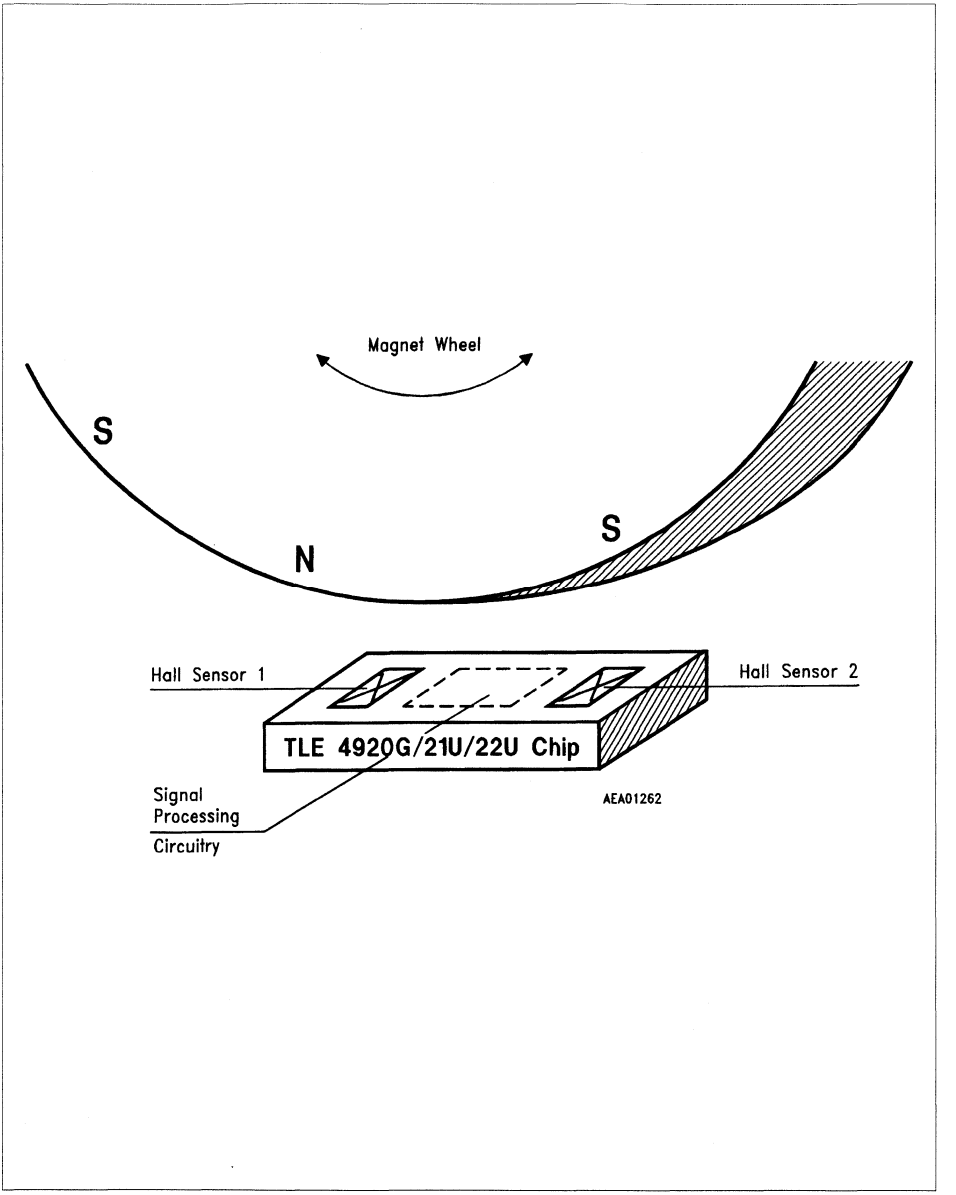


Figure 6
TLE 4920G/4921U/4922U, with Magnet Wheel

Two-wire-application

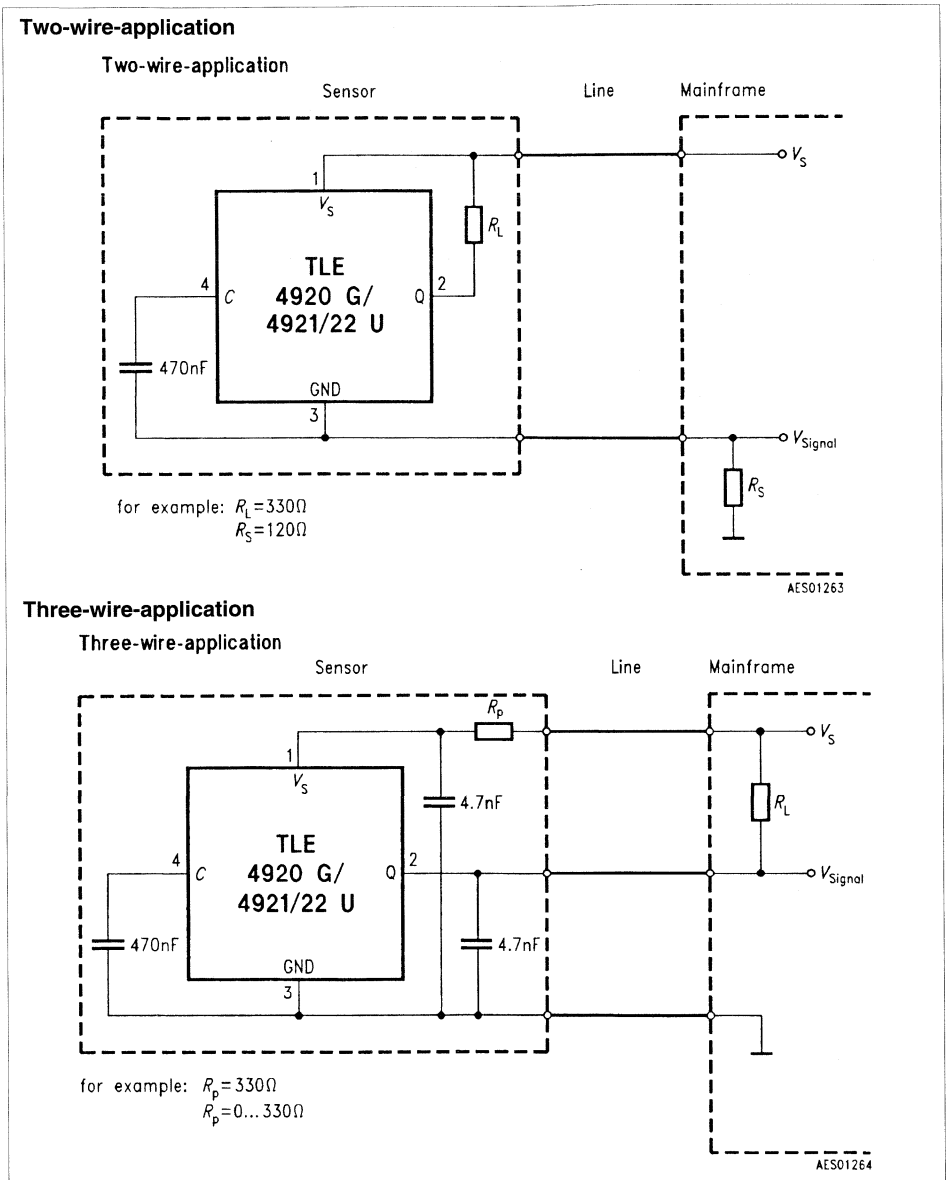


Figure 7
Application Circuits

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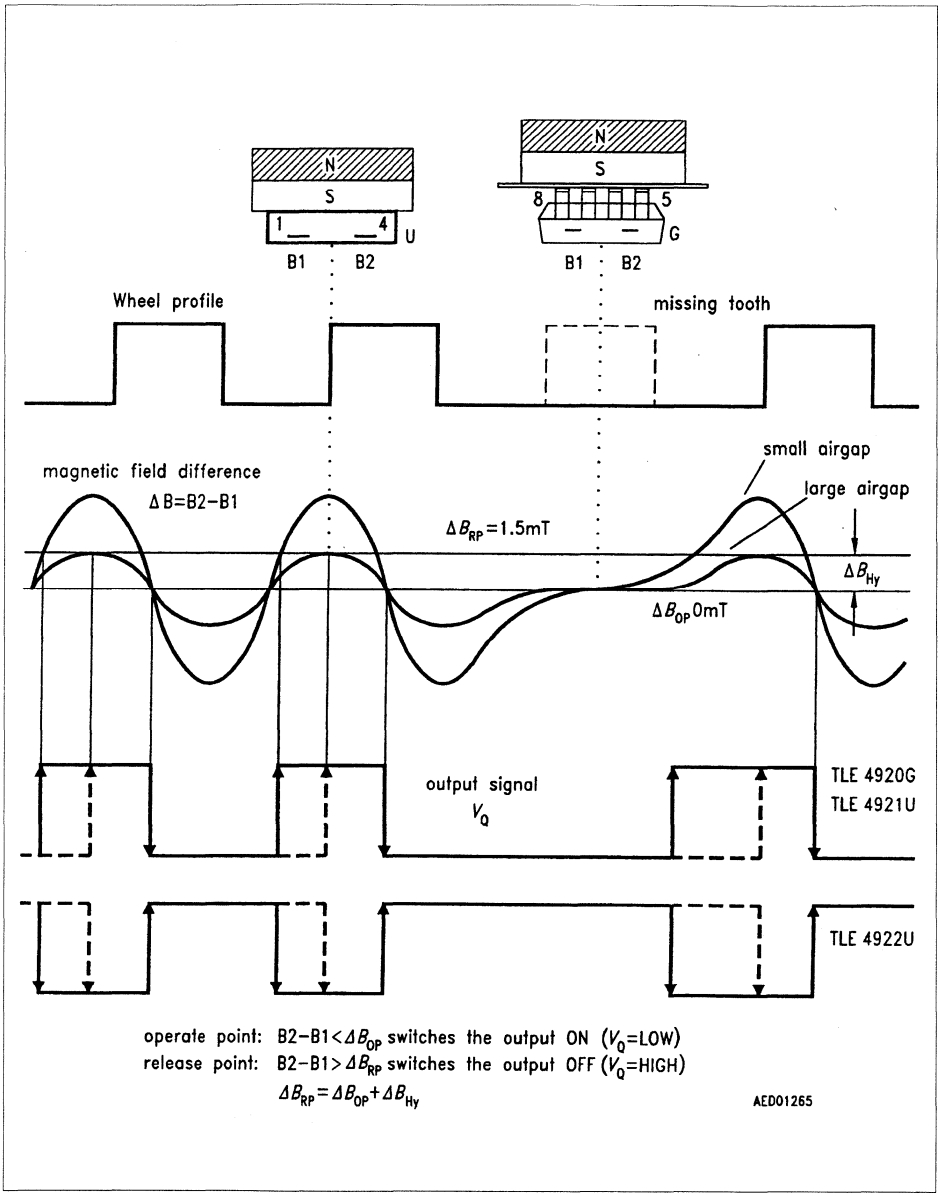
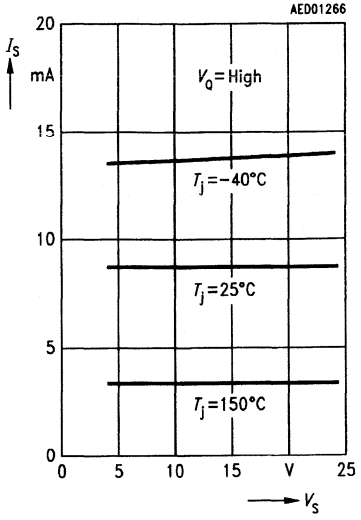
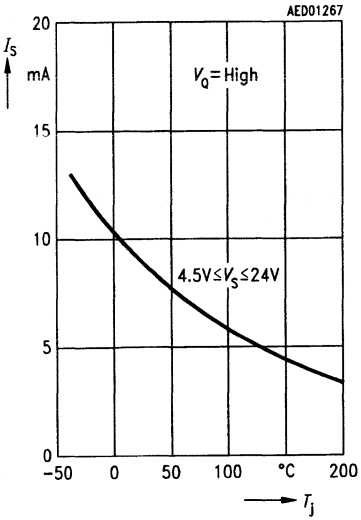


Figure 8
System Operation

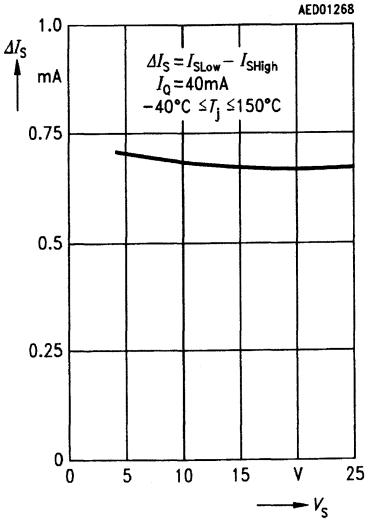
Quiescent Current versus Supply Voltage



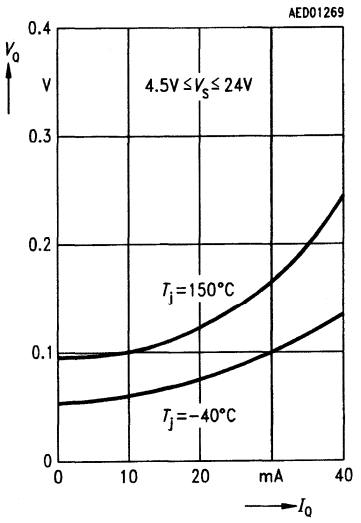
Quiescent Current versus Junction Temperature



Quiescent Current Difference versus Supply Voltage



Saturation Voltage versus Output Current



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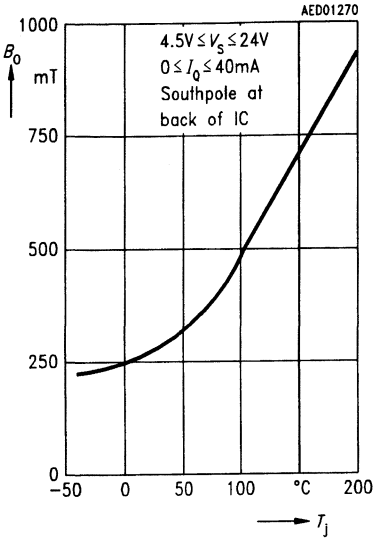
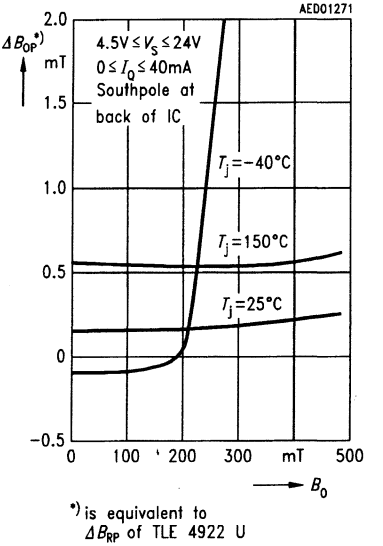
Maximum Preinduction versus Junction Temperature

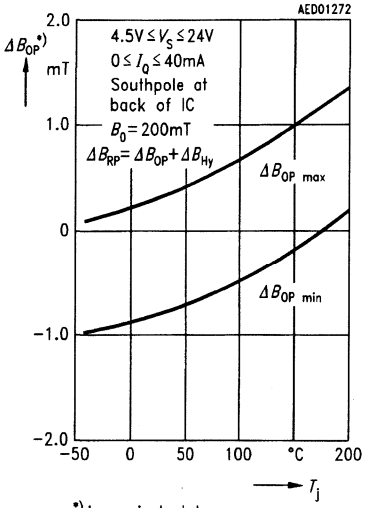


Switching Induction versus Preinduction



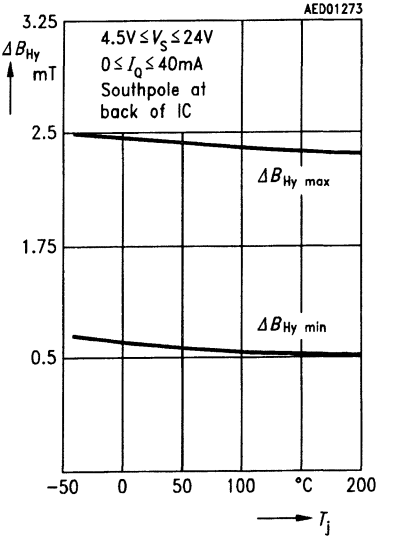
*) is equivalent to ΔB_{RP} of TLE 4922 U

Switching Induction versus Temperature ΔB_{OP} Switches V_Q to Low

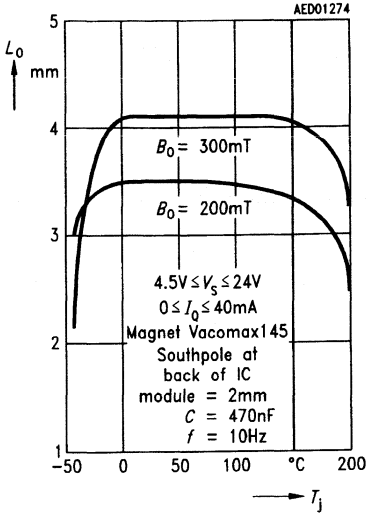


*) is equivalent to ΔB_{RP} of TLE 4922 U

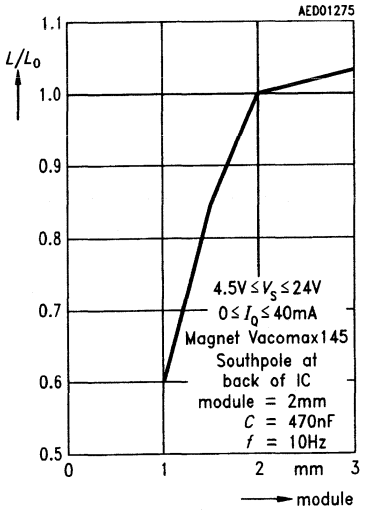
Hysteresis Induction Versus Junction Temperature



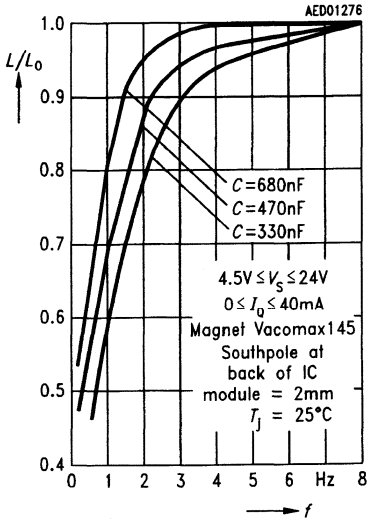
Distance IC-tooth Wheel versus Junction Temperature



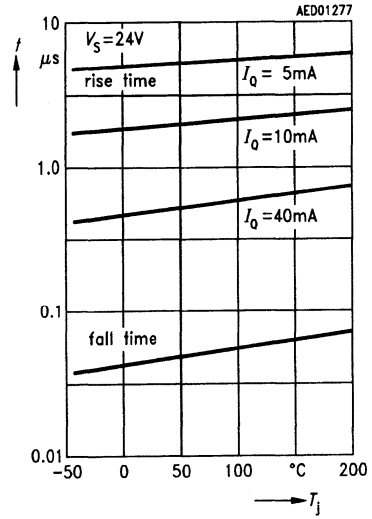
Relative Distance versus Module



Relative Distance versus Switching Frequency



Fall- and Rise-Time versus Junction Temperature



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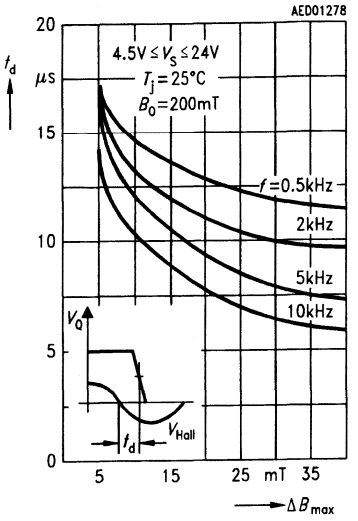
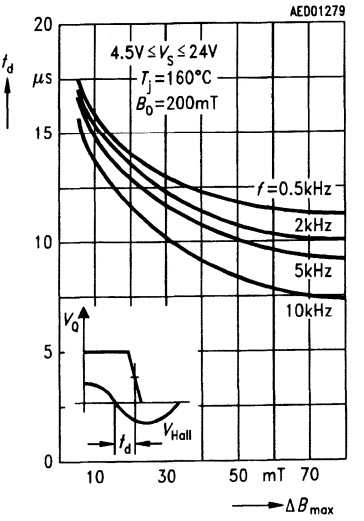
Delay Time between Zero-Axis Crossing of ΔB and Falling Edge of V_Q at T_j = 25 °C



Delay Time between Zero-Axis Crossing of ΔB and Falling Edge of V_Q at T_j = 160 °C



SIEMENS

Differential Hall Effect Sensor IC

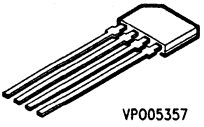
TLE 4971

Preliminary Data

Bipolar IC

Features

- Static operation (zero speed)
- Digital output signal
- Two-wire and three-wire configuration possible
- Large temperature range
- Protection against overvoltage
- Protection against reversed polarity
- Output protection against electrical disturbances



P-SSO-4

Type	Ordering Code	Package
TLE 4971 U	Q67006-A9023	P-SSO-4

The TLE 4971 U is a differential Hall effect sensor designed for rotational speed and timing applications using ferromagnetic toothed wheels and slotted shafts such as camshafts, crankshafts, transmissions, and ABS/TCS systems.

Since the TLE 4971 U can detect zero rotation speed, it is applicable to position sensing as well.

The TLE 4971 U provides a digital signal output with frequency proportional to the speed of rotation. Unlike other rotational sensors differential Hall ICs are not influenced by radial vibration within the effective airgap of the sensor and require no external signal processing.

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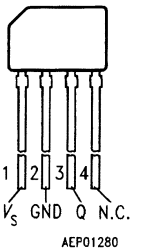

Figure 1
Pin Configuration

Pin Definitions and Functions

Pin	Symbol	Function
1	V_S	Supply voltage
2	GND	Ground
3	Q	Output
4	N.C.	Not connected

Functional Description

The differential Hall sensor IC detects the motion of, and static position of, ferromagnetic and permanent magnet structures by measuring the differential flux density of the magnetic field. To detect ferromagnetic objects the magnetic field must be provided by a back biasing permanent magnet (a magnet attached to the back, unmarked, side of the IC package).

Circuit Description (see Figure 2 and 3)

The TLE 4971 U is comprised of a supply voltage reference, a pair of Hall probes spaced at 2.5 mm, differential amplifier, Schmitt trigger, an open collector output.

Protection is provided at the input/supply (pin 1) for overvoltage and reverse polarity and against overstress such as load dump, etc., in accordance with ISO-TR 7637 and DIN 40839. The output (pin 3) is protected against voltage peaks and electrical disturbances.

Operation

For ease of explanation the probes will be referred to as sensor 1 and sensor 2, and assumes that the Hall IC is back-biased using the south (positive) pole. Operation is reversed, with respect to the active sensor, if back-biasing uses the north (negative) pole.

Applications using a, front (marked side of the IC package) passing, magnet wheel is identical with respect to the Hall sensor operation. Please refer to **figure 8** System Operation.

As a magnetic source, or target pass in front of sensor 2 the magnetic field or field density creates a positive differential at the input of the differential amplifier, resulting in a proportional output to the Schmitt trigger, and a triggered output to the open collector driver.

When the source or target pass in front of sensor 1 (both probes are now influenced by the source/ target) the amplifier inputs are in zero differential state and the output is triggered "off" as the differential amplifier output level falls below the trigger release point.

As the source or target move past sensor 2 (sensor 1 active) the amplifier inputs are in a negative differential state and the Schmitt trigger remains in the "off" state. This insures that there can be no false triggering of the output during the "off" transition.

When the source or target moves past probe 1 (both probes not influenced by source/target) the amplifier is again in the zero differential state and the output remains in a very stable "off" condition, and the cycle repeats.

Rotation Sensing Cycle

1. Sensor 2 active (over target) - Output triggered "on"
2. Sensor 1 and 2 active (both probes over target) - Output triggered "off".
   Note:
   This step might not occure of the gear tooth, or target, width is less than 2.5mm.
3. Sensor 2 inactive (over space), sensor 1 active (over target) - Negative differential mode - Output remains "off".
4. Sensor 1 and 2 inactive (both probes over space) - Output remains "off".

For applications which require larger airgaps (3 mm +) and do not require zero (static) speed sensing, the TLE 4922 U (dynamic-active low output) or TLE 4921 U (dynamic-active high output) should be used.

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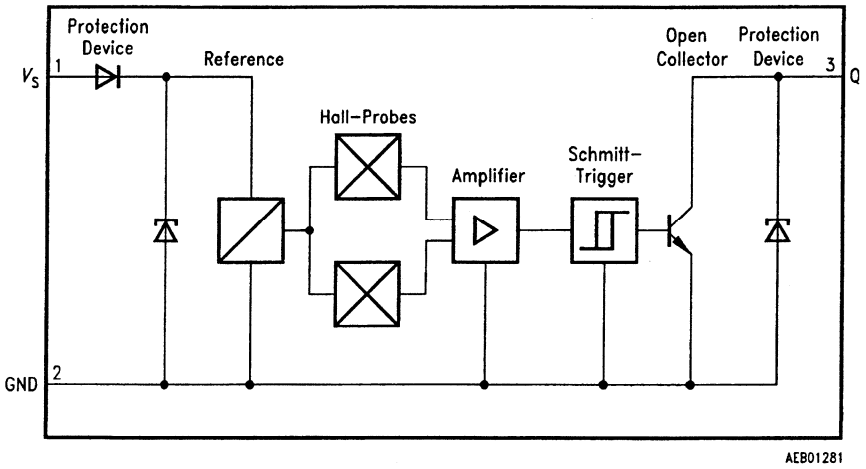

Figure 2
Block Diagram 1

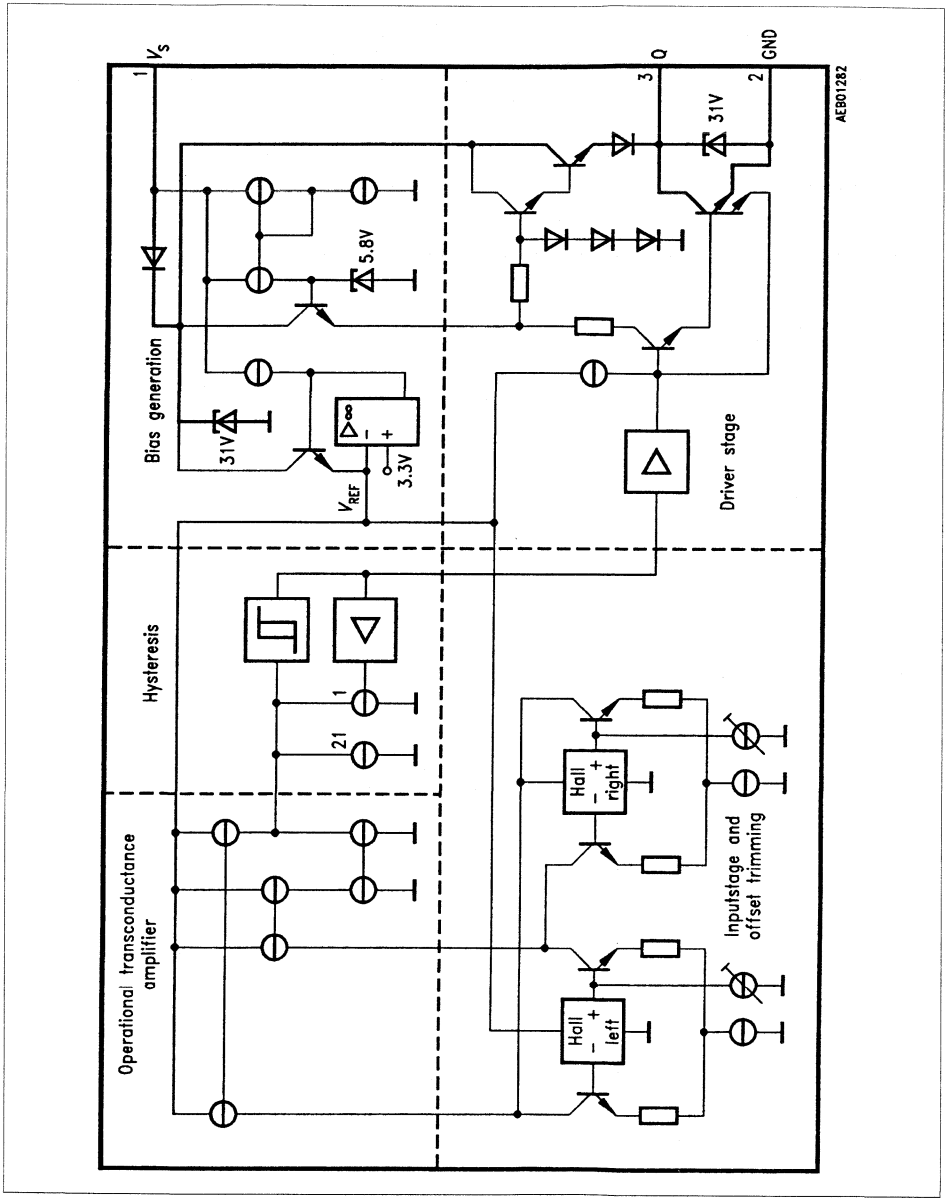

Figure 3
Block Diagram 2

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Absolute Maximum Ratings

T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	– 40	30	V	–
Output voltage	V_Q	– 0.7	30	V	–
Output current	I_Q	–	50	mA	–
Output reverse current	$-I_Q$	–	50	mA	–
Junction temperature	T_j	–	150	°C	–
Junction temperature	T_j	–	180	°C	1000 h
Junction temperature	T_j	–	210	°C	40 h
Storage temperature	T_{stg}	– 40	150	°C	–
Thermal resistance	$R_{th\,JA}$	–	240	K/W	–
Current through input-protection device	I_{SZ}	– 200	200	mA	t < 2 ms; v = 0.1
Current through output-protection device	I_{QZ}	– 200	200	mA	t < 2 ms; v = 0.1

Electro Magnetic Compatibility

ref. DIN 40839 part 1; test circuit 1

Testpulse 1	V_{LD}	– 100	–	V	t_d = 2 ms
Testpulse 2	V_{LD}	–	100	V	t_d = 0.05 ms
Testpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testpulse 4	V_{LD}	– 7	–	V	$t_d \leq$ 20 s
Testpulse 5	V_{LD}	–	120	V	t_d = 400 ms

Operating Range

Supply voltage	V_S	4.5	24	V	–
Junction temperature	T_j	– 40	150	°C	–
Junction temperature	T_j	– 40	180	°C	1000 h
Junction temperature	T_j	– 40	210	°C	40 h
Pre-induction	B_O	– 500	500	mT	–

Absolute Maximum Ratings (cont'd)
T_A = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Electro Magnetic Compatibility
ref. DIN 40839 part 1; test circuit 1

Testpulse 2	V_{LD}	–	100	V	t_d = 0.05 ms
Testpulse 3a	V_{LD}	– 150	–	V	t_d = 0.1 µs
Testpulse 3b	V_{LD}	–	100	V	t_d = 0.1 µs
Testpulse 4	V_{LD}	– 7	–	V	$t_d \leq$ 20 s
Testpulse 5	V_{LD}	–	120	V	t_d = 400 ms

AC/DC Characteristics
4.5 V ≤ V_S ≤ 24 V; – 40 °C ≤ T_j ≤ 150 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Supply current						V_Q = high, I_Q = 0 mA	
	I_S	3.0	8	12	mA	V_S = 4.5 V	1
	I_S	3.5	8.5	13.5	mA	$V_S \geq$ 7 V	1
						V_Q = low, I_Q = 40 mA	
	I_S	3.5	8.5	12.5	mA	V_S = 4.5 V	1
	I_S	4.0	9	14.5	mA	$V_S \geq$ 7 V	1
Output saturation voltage	V_{QSat}	–	0.25	0.6	V	I_Q = 40 mA	1
Output leakage current	I_{QL}	–	–	10	µA	V_Q = 24 V	1
Switching frequency	f	0	–	20	kHz	ΔB = 10 mT	2
Switching flux density	ΔB_{RP}	–	7.5	–	mT	–	2
Hysteresis	ΔB_{Hy}	–	2.5	–	mT	–	2
Overvoltage protection							
– at supply voltage	V_{SZ}	27	–	35	V	I_S = 16 mA	1
– at output	V_{QZ}	27	–	35	V	I_S = 16 mA	1

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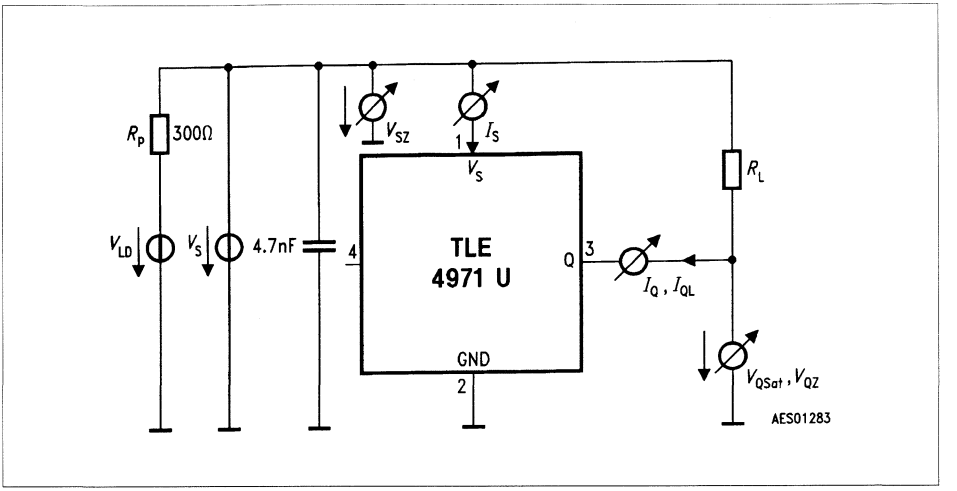


Figure 4
Test Circuit 1

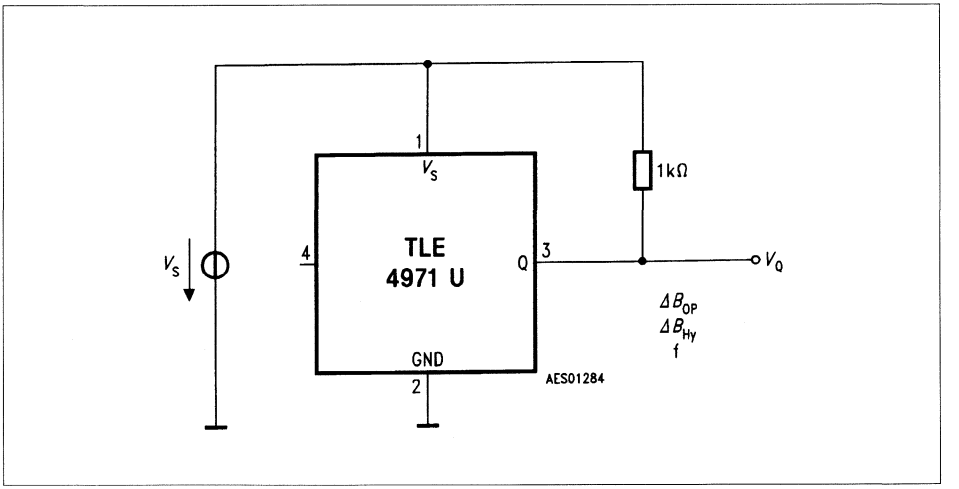


Figure 5
Test Circuit 2

- B_O = 100 mT;
- tooth wheel with module m = 2 mm
- Distance IC-object L = 1 mm
- Southpole at back of IC

Application Notes

Two possible applications are shown in **figure 6 and 7** (Tooth and Magnet Wheel).

The differences between two-wire and three-wire application is shown in **figure 9**.

Tothed Wheel Sensing

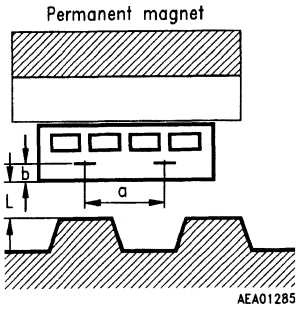
In the case of ferromagnetic toothed wheel application the IC has to be biased by a permanent magnet (e.g. $SECo_5$ (Vacuumschmelze VX145) with the dimensions 8 mm x 5 mm x 3 mm) which should cover both hallprobes.

The maximum air gap depends on

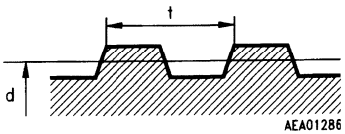
- the magnetic field strength (magnet used),
- the toothed wheel that is used (dimensions, material, etc),
- the ambient temperature

Sensor Spacing

a	centred distance of hall probes	a = 2.5 mm
b	hall-probes to IC surface	b= 0.25 mm
L	IC surface to tooth wheel	



Toothed Wheel Dimensions



Conversion DIN - ASA
m = 25.4 mm/p
t = 25.4 mm x CP

DIN

d	diameter (mm)
z	number of teeth
m	module m = d/z (mm)
t	pitch t = π x m (mm)

ASA

p	diametral pitch p = z/d (inch)
PD	pitch diameter PD = z/p (inch)
CP	circular pitch CP = 1 inch x π /p

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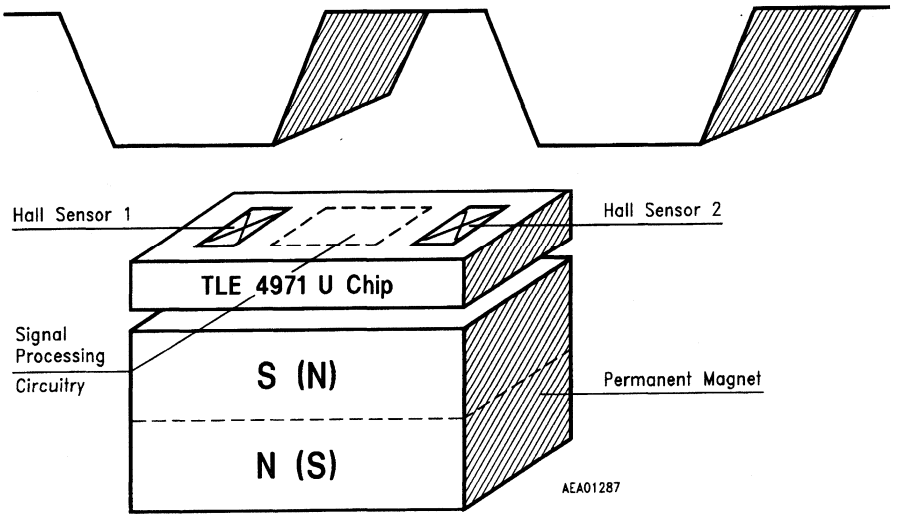


Figure 6
TLE 4971 U, with Ferromagnetic Toothed Wheel

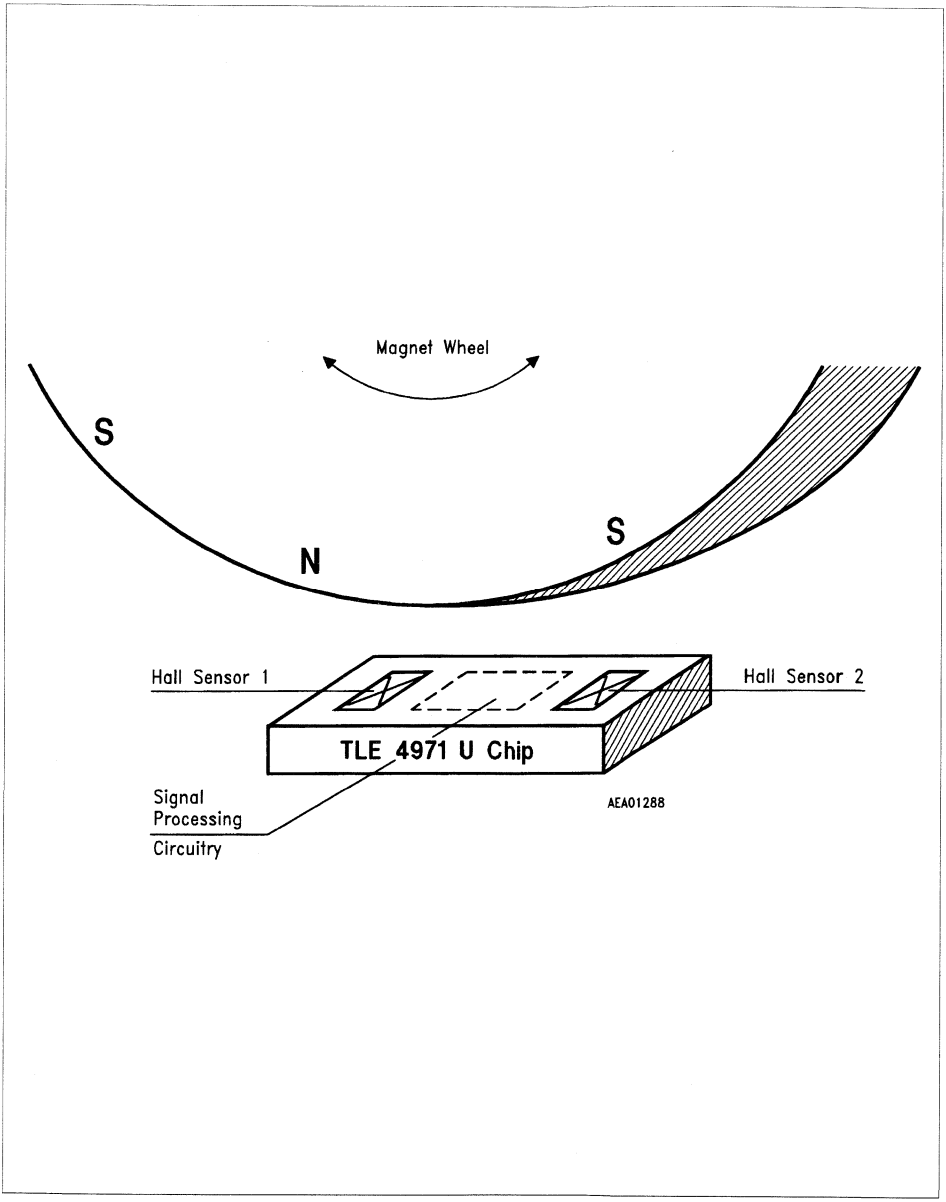
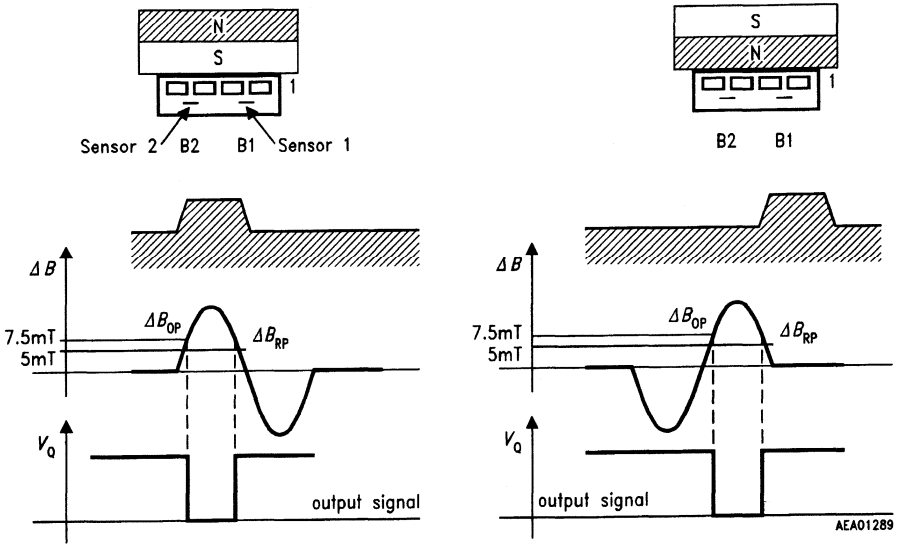


Figure 7
TLE 4971 U, with Magnet Wheel

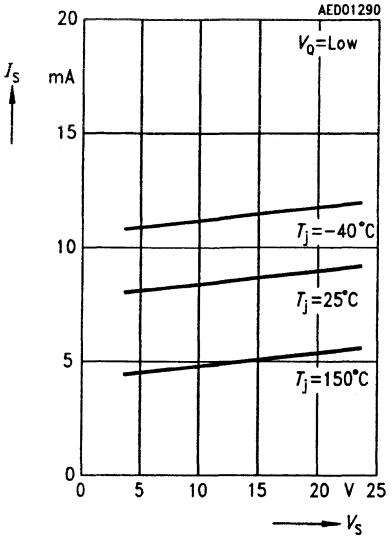


For Southpole or Northpole at the back of the IC

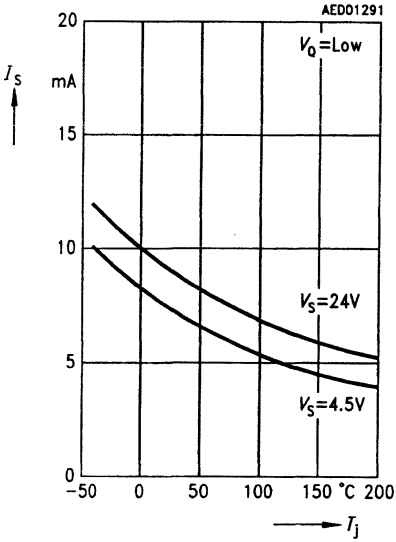
release point: B2-B1 < ΔB_{RP} switches the output OFF (V_Q = HIGH)
operate point: B2-B1 > ΔB_{OP} switches the output ON (V_Q = LOW)
$\Delta B_{OP} = \Delta B_{RP} + \Delta B_{Hy}$

Figure 8
System Operation

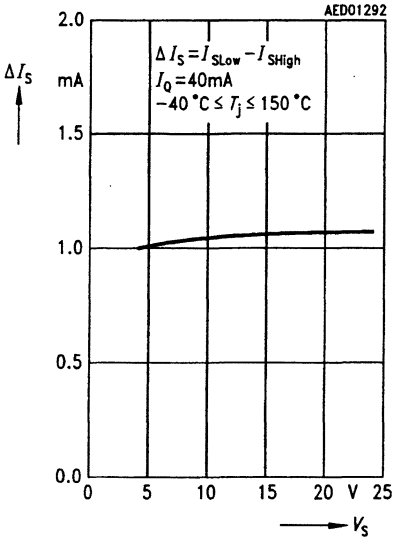
Quiescent Current versus Supply Voltage



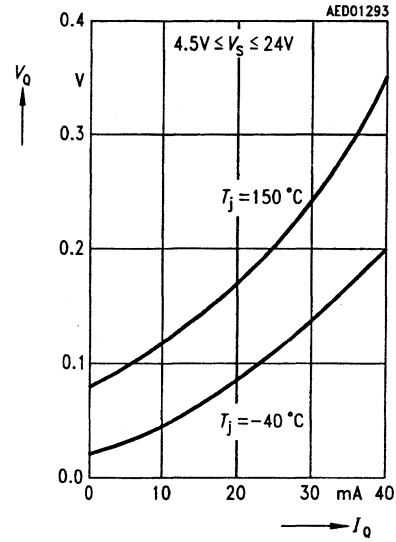
Quiescent Current versus Junction Temperature



Quiescent Current Difference versus Supply Voltage



Saturation Voltage versus Output current



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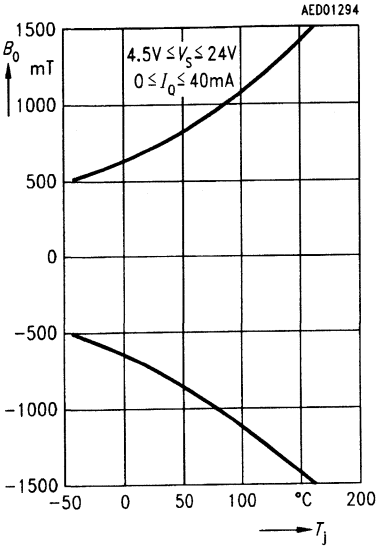
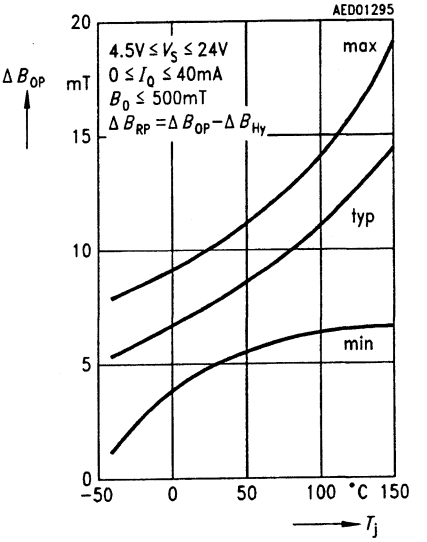
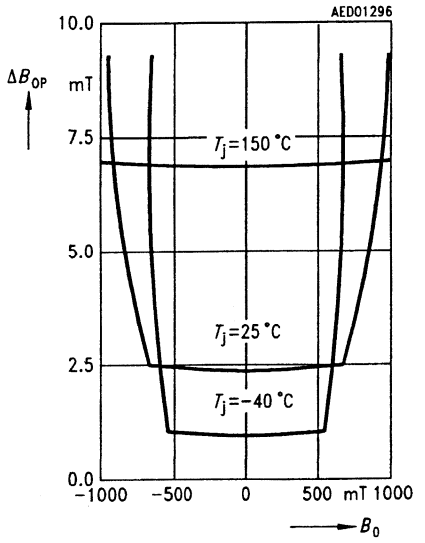
Maximum Preinduction versus Junction Temperature



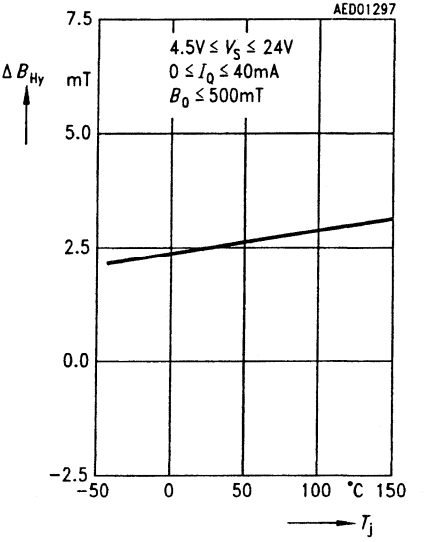
Switching Induction versus Temperature



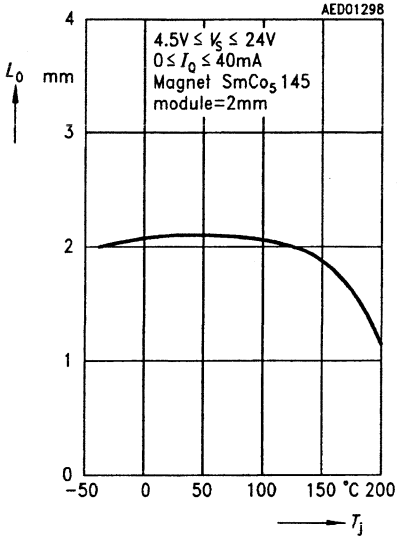
Switching Induction versus Preinduction



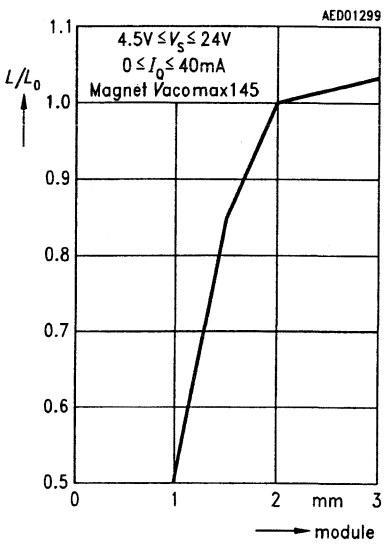
Hysteresis Induction versus Junction Temperature



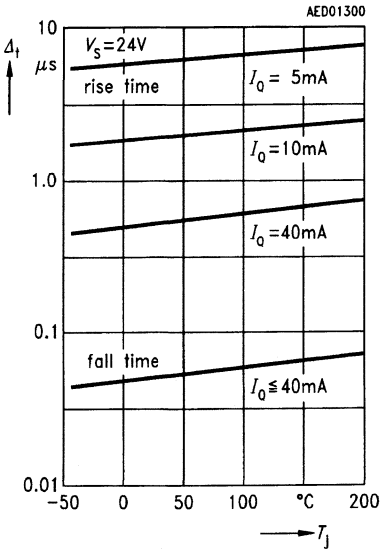
Distance IC-Toothed Wheel versus Junction Temperature



Relative Distance versus Module



Fall and Rise Time versus Junction Temperature



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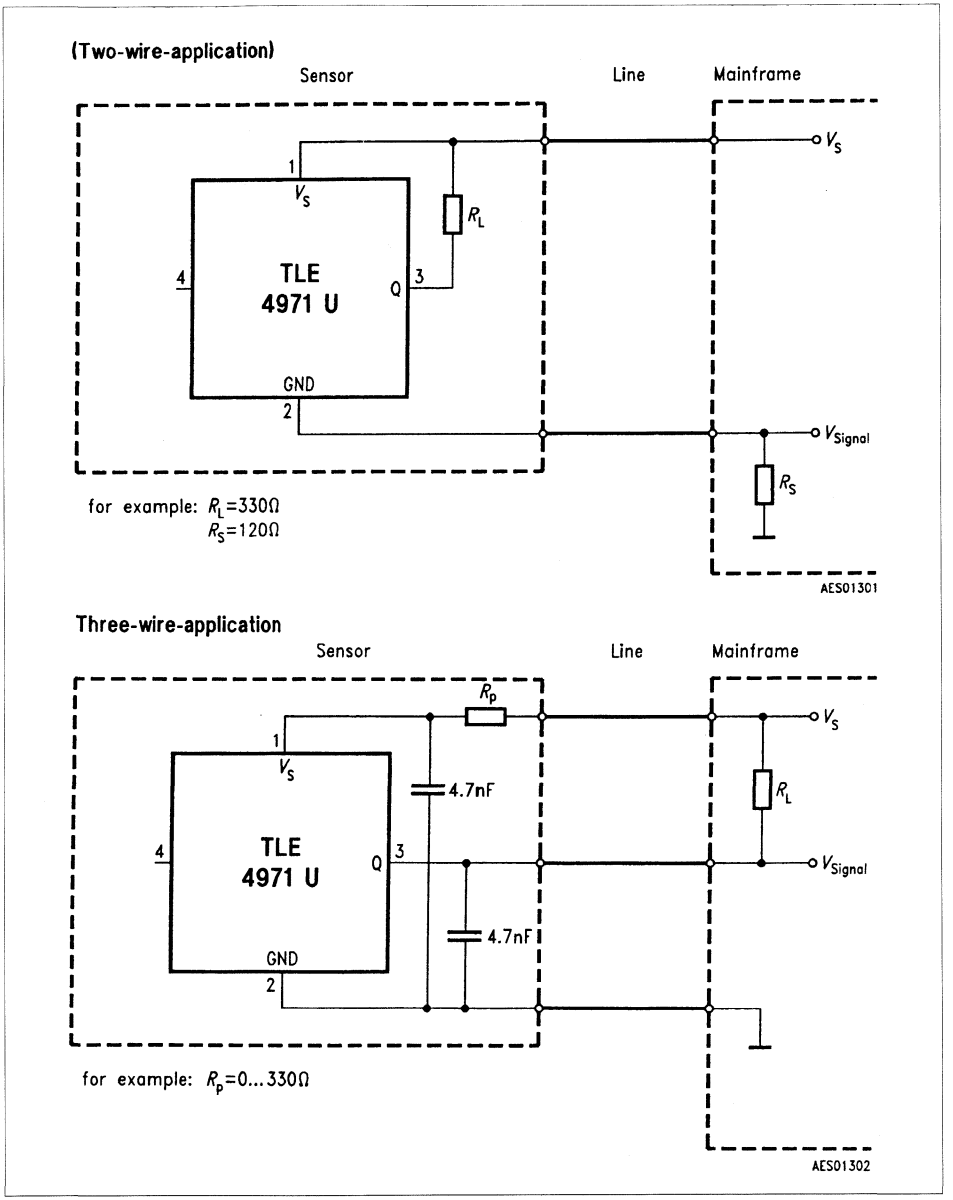


Figure 9
Application Circuits

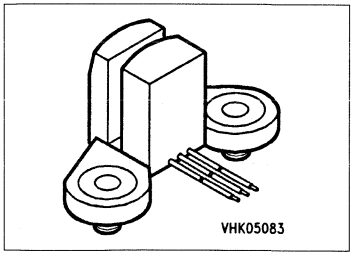
Hall-Effect Vane Switch

HKZ 121

Bipolar IC

Features

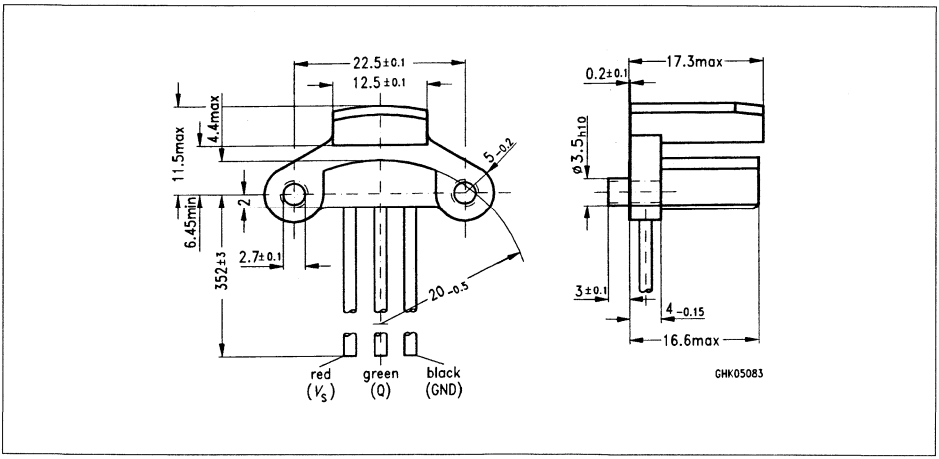
- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity
- Integrated capacitors for EMI protection



Type	Ordering Code	Package
S HKZ 121	Q67000-A9097-A401	Special package

The Hall-effect vane switch HKZ 121 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a soft-iron vane which is passed through the air gap between magnet and Hall sensor.

The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmental conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).



Special Package

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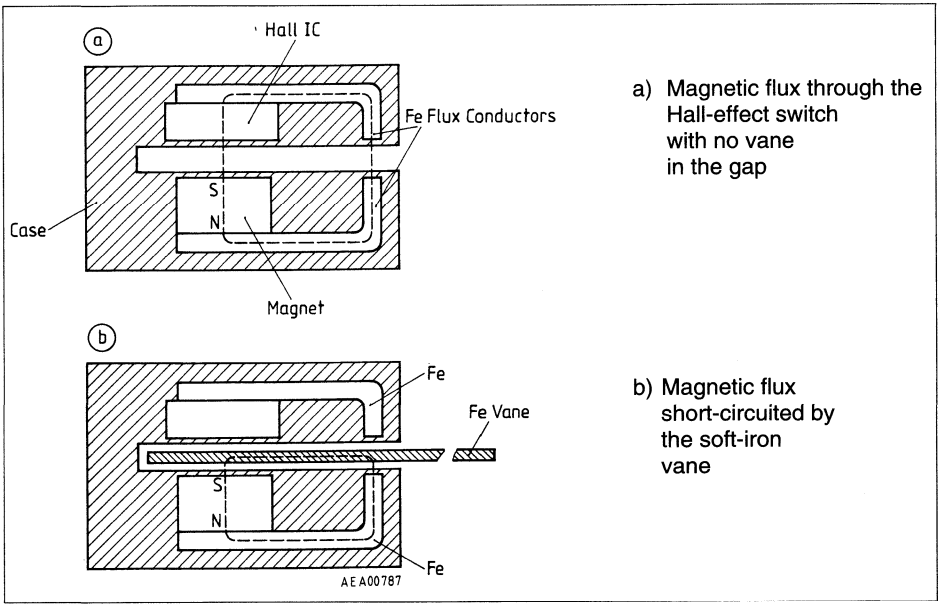
Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the hall-effect sensor, as shown below. The open collector output is conductive (low) when the vane is outside the air gap, and blocks (high) when the vane is introduced into the air gap. The output remains high as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

Principle of Operation

Mechanical Characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic package, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply, output and ground.

Application Notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 1.2	24	V	–
			30	V	T_A = 25 °C
Output voltage in OFF-state	V_Q	– 0.8	30	V	–
Inverse supply current (limited externally)	$-I_S$	–	200	mA	T_A = 80 °C $t \leq 1$ h
Output current	I_Q	–	40	mA	without vane
Inverse output current	$-I_Q$	–	30	mA	
Ambient temperature	T_A	– 40	135	°C	–
Storage temperature	T_{stg}	– 40	150	°C	–
Thermal resistance system - air	$R_{th\,SA}$	–	170	K/W	–

Operating Range

Supply voltage	V_S	4.5	24	V	–
Ambient temperature	T_A	– 40	130	°C	–
Vane[1]: thickness	a	0.5		mm	–
width	b	8		mm	–
gap length	c	8		mm	–
immersion depth	h	4.6	9	mm	–
gap height	d	7.3 – h		mm	–

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[1] **see figure 3**

Characteristics
V_S = 5 V to 18 V, T_A = – 30 to 130 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Output saturation voltage	$V_{Q\,sat}$	–	–	–	without vane
			–	–	I_Q = 40 mA
			0.4	V	T_A = – 30 to 110 °C
			0.6	V	T_A = 110 to 130 °C
Output reverse current	$I_{Q\,R}$	–	10	µA	with vane
Supply current	I_S	–	12	mA	without vane
Fall time	t_{HL}	–	1	µs	I_Q = 40 mA
Overvoltage protection					
– Supply voltage (V_S)	V_{SZ}	32	42	V	I_S = 16 mA
– Output (V_Q)	V_{SO}	32	42	V	I_S = 16 mA

Switching Point Characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics are important on temperature and operating voltage.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown the following figure.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

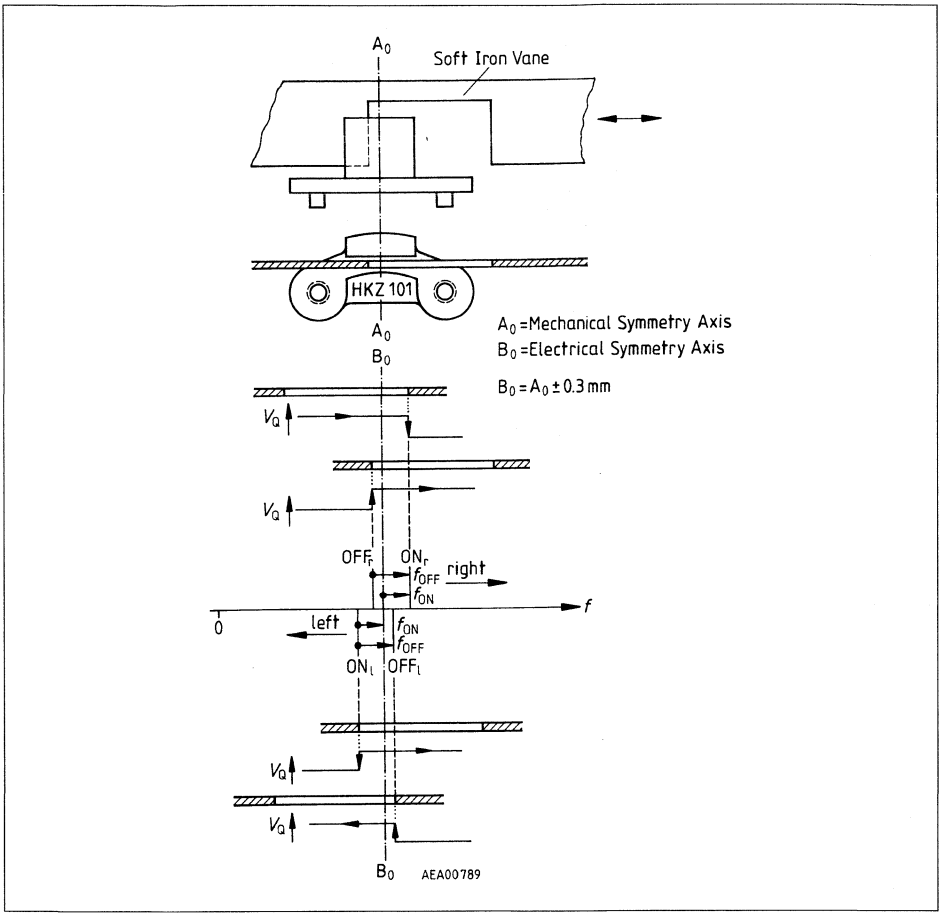
The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions (V_S = 12 V, T_A = 25 °C) within the characteristic device deviation.

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$



Switching Point Definitions

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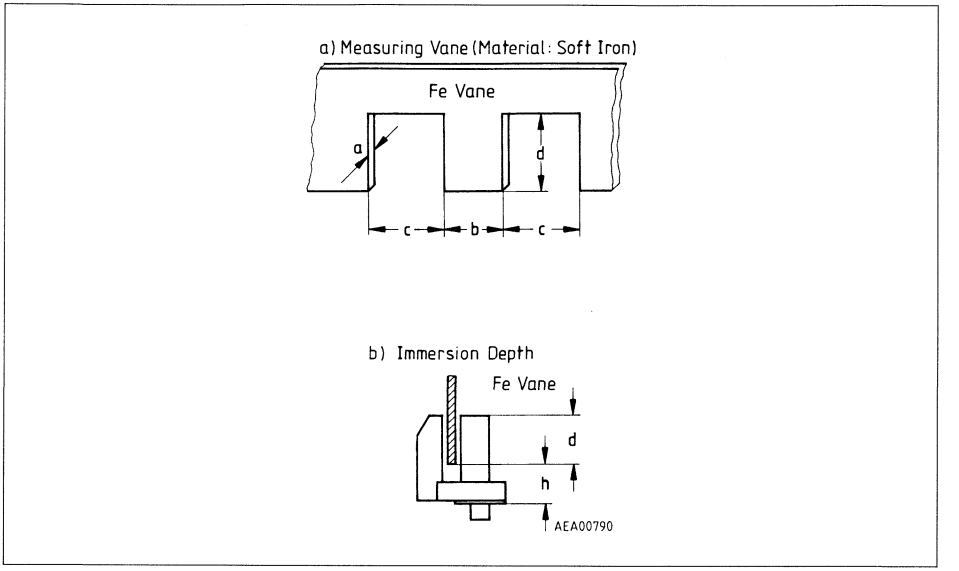


Mechanical Measurement Conditions

Switching Point Characteristics

Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
HKZ 121						
Operate point	$f_{ON\,0}$	0.85	1.45	2.05	mm	V_S = 12 V, T_A = 25 °C
Deviations	Δf_{ON}	– 0.4	0.15	0.7	mm	T_A = – 30 to 25 °C
		– 0.2	0.15	0.4	mm	T_A = 25 to 80 °C
		– 0.4	0.2	0.7	mm	T_A = 80 to 130 °C
Release point	$f_{OFF\,0}$	1.54	2.54	3.54	mm	V_S = 12 V, T_A = 25 °C
Deviations	Δf_{OFF}	– 0.8	0.3	1.4	mm	T_A = – 30 to 25 °C
		– 0.4	0.3	0.8	mm	T_A = 25 to 80 °C
		– 0.8	0.4	1.4	mm	T_A = 80 to 130 °C

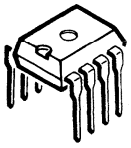
Proximity Switch

TCA 305
TCA 355

Bipolar IC

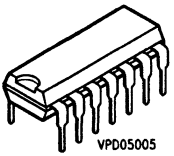
Features

- Lower open-loop current consumption; I_S < 1 mA
- Lower output saturation voltage
- The temperature dependence of the switching distance is lower and compensation of the resonant circuit *TC* (temperature coefficient) is easier
- The sensitivity is higher, so that larger switching distances are possible and coils of a lower quality can be used
- The switching hysteresis remains constant as regards temperature, supply voltage and switching distance
- The TCA 305 even functions without external integrating capacitor. With an external capacitor (or with RC combination) good noise immunity can be achieved
- The outputs are temporarily short-circuit proof (approx. 10 s to 1 min depending on package)
- The outputs are disabled when V_S < approx. 4.5 V and are enabled when the oscillator stabilizes (from $V_{S\,min}$ = 5 V)
- Higher switching frequencies can be obtained
- Miniature package

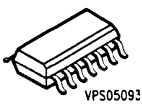


P-DIP-8

P-DSO-8-1



P-DIP-14-1



P-DSO-14-1

	Type	Ordering Code	Package
S	TCA 305 A	Q67000-A2291	P-DIP-14-1
S	TCA 305 G	Q67000-A2305	P-DSO-14-1 (SMD)
S	TCA 355 B	Q67000-A2443	P-DIP-8
S	TCA 355 G	Q67000-A2444	P-DSO-8-1 (SMD)

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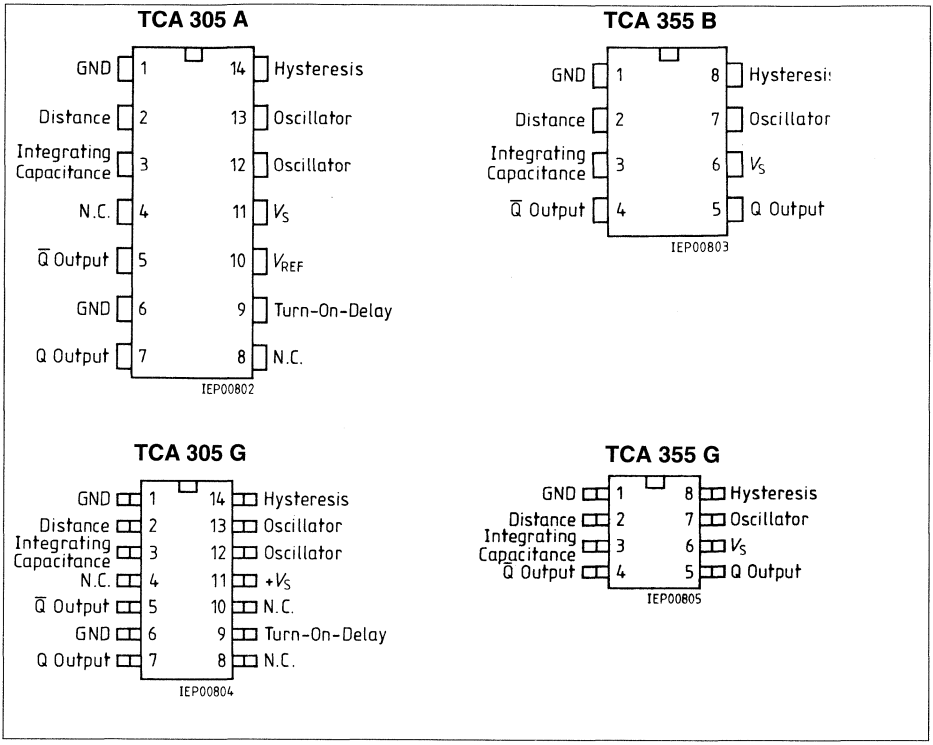


Pin Configurations (top view)

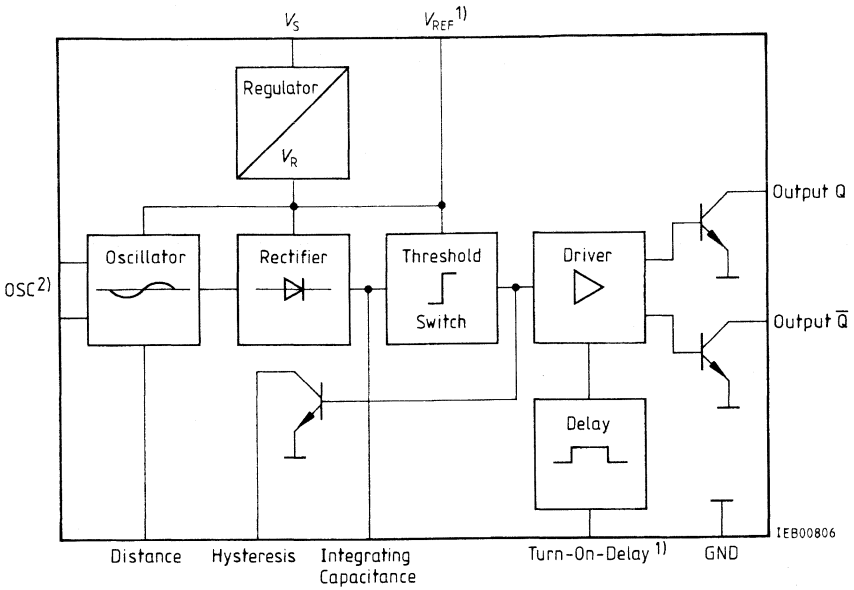
The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

Operation Schematic: see TCA 205

The types TCA 305 and TCA 355 have been developed from the type TCA 205 and are outstanding for the following characteristics:

Logic Functions

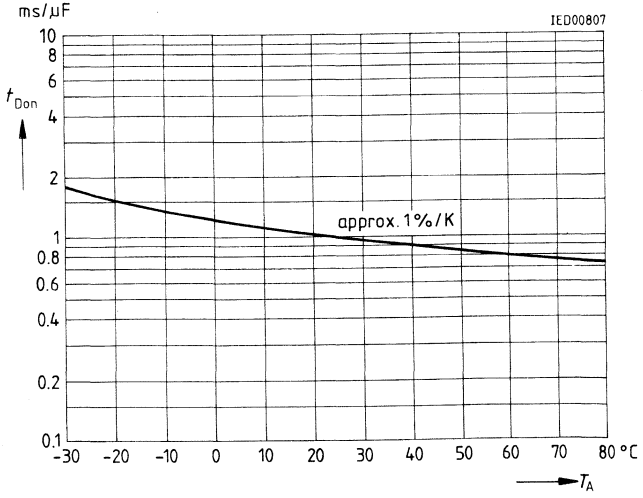
Oscillator	Outputs	
	Q	$\bar{Q}$
not damped	H	L
damped	L	H



1) TCA 305 only
2) Connected internally in case of TCA 355

Block Diagram

Standard Turn-ON Delay Referred to T_A = 25 °C



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Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	35	V
Output voltage	V_Q	35	V
Output current	I_Q	50	mA
Distance, hysteresis resistance	R_{Di}, R_{Hy}	0	Ω
Capacitances	C_I, C_D	5	µF
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance			
system - air TCA 305 A	$R_{th\,SA}$	85 (135)[2]	K/W
TCA 305 G	$R_{th\,SA}$	140 (200)[2]	K/W

Operating Range

Supply voltage	V_S	5 to 30[3]	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	– 25 to 85	°C

Characteristics

V_S = 12 V, T_A = – 25 to 85 °C

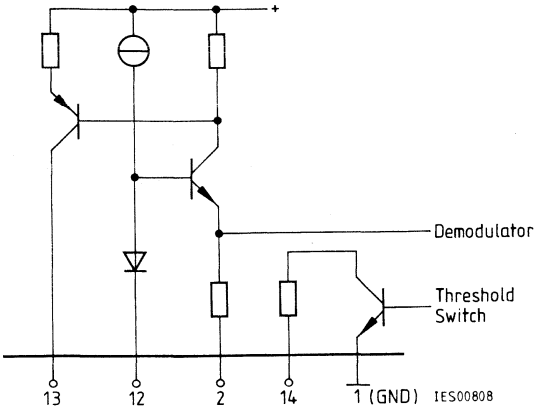
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Open-loop current consumption	I_S		0.6	0.9 (1.0)[2]	mA	outputs open
Reference voltage[1]	V_{REF}		3.2		V	I_{REF}< 10 µA
L-output voltage	V_{QL}		0.04	0.15	V	I_{QL} = 5 mA
per output	V_{QL}		0.10	0.35	V	I_{QL} = 25 mA
	V_{QL}		0.22	0.75	V	I_{QL} = 50 mA
H-output current per output	I_{QH}			10	µA	V_{QH} = 30 V
Threshold at 3	V_{S3}		2.1		V	
Hysteresis at 3	V_{Hy}	0.4	0.5	0.6	V	
Turn-ON delay[1]	$t_{D\,ON}$	– 25 %	600	– 25 %	ms/µF	T_A = 25 °C
Switching frequency w/o C_I	f_S			5	kHz	

[1] TCA 305 only

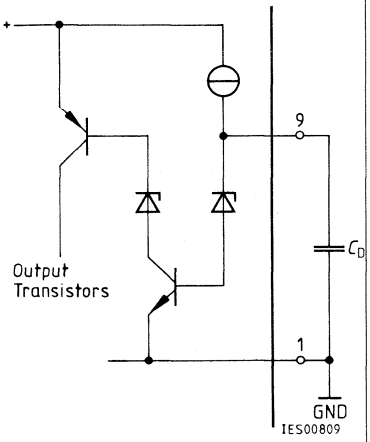
[2] Values in parenthesis apply to TCA 355 only

[3] Operation at voltages less than 5 V (between approx. 2.5 and 5 V) is possible, if V_{REF} is connected to V_S. In this case V_{REF} is no longer internally stabilized. Additionally, the pin "turn-on delay" is to be applied as follows: If no turn-on delay is needed, this pin has to be connected to V_S. If, however, a turn-on delay is required, the charge current for D_D has to be adjusted with an external resistor between this pin and V_S (recommended value 390 kΩ).

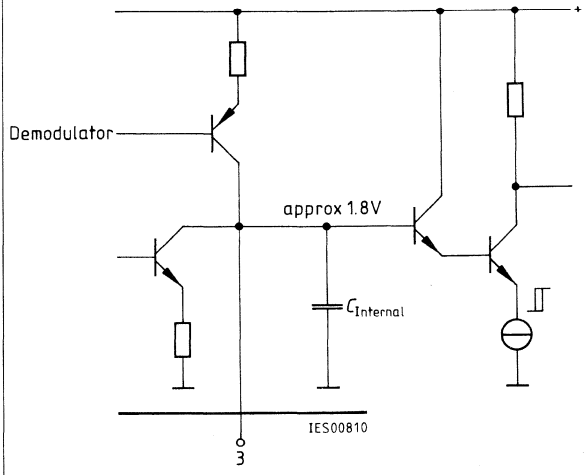
Oscillator



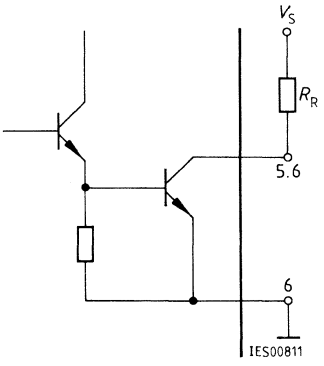
Turn-ON Delay for TCA 305 A; G



Integrating Capacitor



Outputs



Schematic Circuit Diagrams

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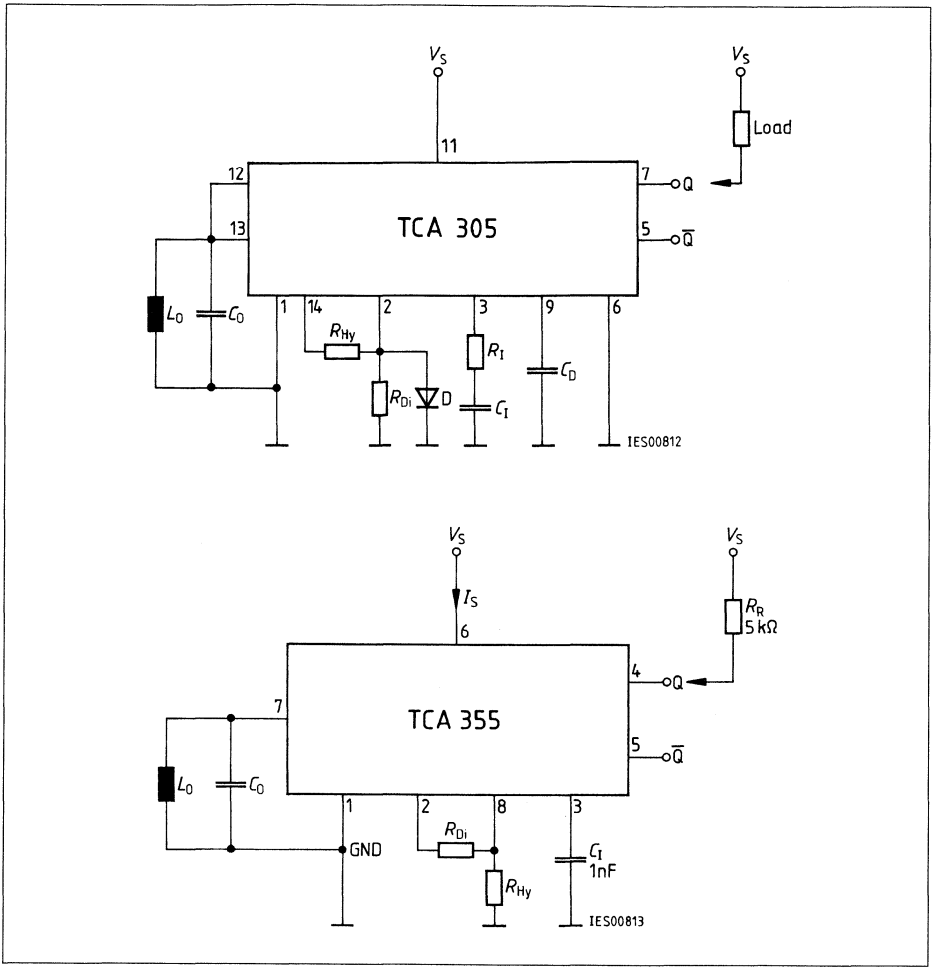

Application Circuits

L_0, C_0	Resonant circuit
R_{Hy}	Hysteresis adjustment
R_{Di}	Distance adjustment
D	Temperature compensation of the resonant circuit; possibly with series resistance for the purpose of adjustment. The diode is not absolutely necessary. Whether it is used or not depends on the temperature coefficient of the resonant circuit.
R_I; C_I	Integration element. At pin 3 (integrating capacitance) we recommend a capacitor of typ. 1 nF. To increase noise immunity this capacitor can be substituted by an RC circuit with, e.g., R_I = 1 MΩ and C_I = 10 nF.
C_D	Delay capacitor

Dimensioning Examples in Accordance with CENELEC Standard (flush)

	M 12	M 18	M 30
Ferrite pot core	M 33 (7.35 × 3.6) mm	N 22 (14.4 × 7.5) mm	N 22 (25 × 8.9) mm
Number of turns	100	80	100
Cross section of wire	0.1 CuL	20 × 0.05	10 × 0.1
L_0	206 µH	268 µH	585 µH
C_0 (STYROFLEX®)	1000 pF	1.2 nF	3.3 nF
f_{OSC}	appr. 350 kHz	appr. 280 kHz	appr. 115 kHz
Sn	4 mm	8 mm	15 mm
R_A (Metal)	8.2 kΩ + 330 Ω	33 kΩ	22 kΩ + 2.7 kΩ
C_D	100 nF	100 nF	100 nF

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SIEMENS

IC for Inductive Proximity Switches with Short-Circuit Protection

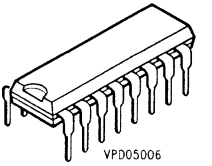
TCA 505 B

Preliminary Data

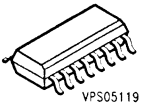
Bipolar IC

Features

- Wide supply voltage of 3.1 to 4.5 V and 4 to 40 V
- Low current consumption of less than 0.8 mA
- Integrated output stage for up to 60 mA output current
- Short-circuit and overload protection of output stages and external components
- Temperature response of the IC compensates that of the coil
- High noise immunity
- High switching frequencies up to 5 kHz
- Useful extra functions
- Suitable for two-wire AC proximity switches
- Temperature range – 40 to 110 °C



P-DIP-16



P-DSO-16-1

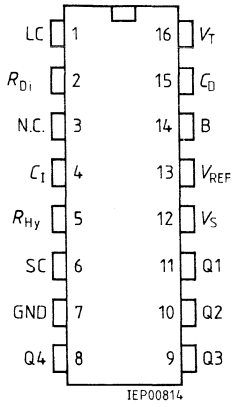
	Type	Ordering Code	Package
S▼	TCA 505 B	Q67000-A8344	P-DIP-16
S▼	TCA 505 BG	Q67000-A8341	P-DSO-16-1 (SMD)

▼ New type

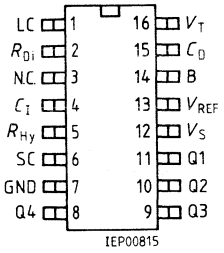
Besides its basic functions (oscillator, demodulator and threshold switch), the bipolar monolithic IC TCA 505 B includes a number of useful extra functions that enable high-grade, inductive proximity switches to be designed for an attractive price/performance ratio and with space savings.

Compared to earlier ICs for inductive proximity switches temperature drift, noise immunity and the switching frequency of the IC have been improved.

TCA 505 B



TCA 505 BG



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	LC	Oscillator
2	R_{Di}	Distance
3	N.C.	Not connected
4	C_I	Integrating capacitance
5	R_{Hy}	Hysteresis
6	SC	Short-circuit detector
7	GND	Ground
8	Q4	Output
9	Q3	Output
10	Q2	Output
11	Q1	Output
12	V_S	Supply voltage
13	V_{REF}	Reference voltage
14	B	Base Output Transistors
15	C_D	Turn-ON delay / Short-circuit delay
16	V_T	Two-wire regulator

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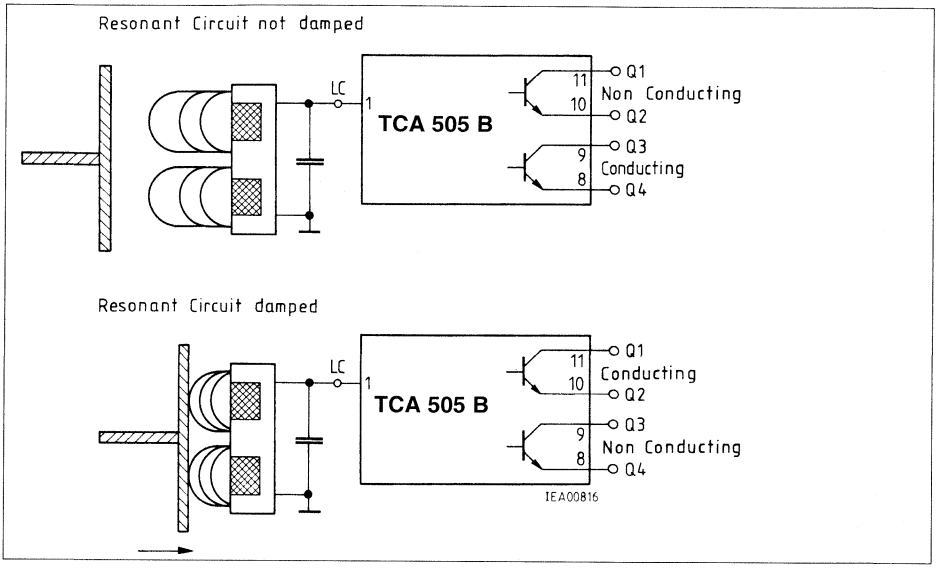
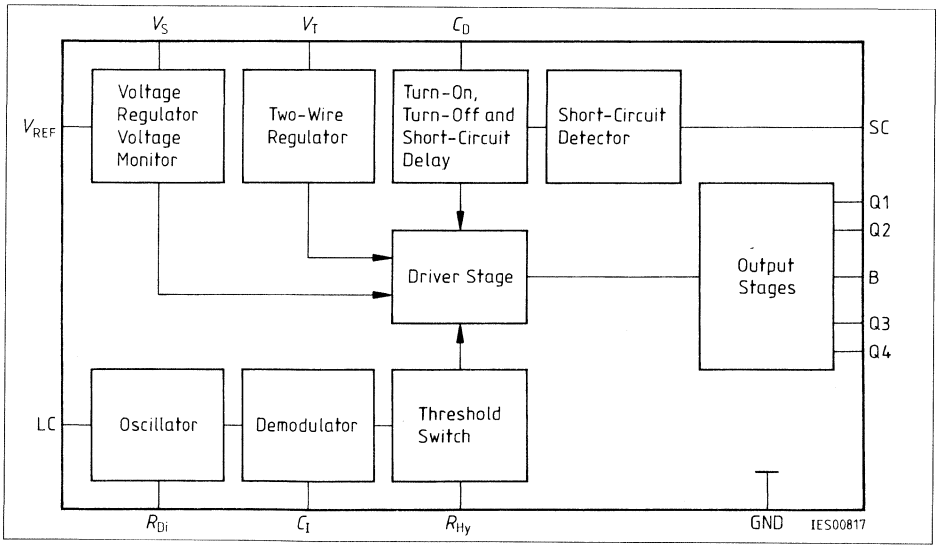
Functional Description and Application



Operation Schematic



Block Diagram

Functional Description

This circuit is used to design inductive proximity switches. The resonant circuit of the LC oscillator is implemented with an open half-pot ferrite and a capacitor in parallel (pin LC). If a metallic target is moved closer to the open side of the half-pot ferrite, energy is drawn from the resonant circuit and the amplitude of the oscillation is reduced accordingly. This change in amplitude is transmitted to a threshold switch by means of a demodulator and triggers the outputs (**see operation schematic**).

By means of an external distance resistor on the oscillator (pin R_{Di}) it is possible to set the switching distance within wide limits, the optimal distances being 0.1 to 0.6 of the diameter of the half-pot ferrite, although both of these parameters can be exceeded. The circuit also enables the setting of a path hysteresis by switching of the external distance resistor via pin R_{Hy} (**see application circuit 1**).

There are two antiphase output stages (Q1 / Q2 and Q3 / Q4) for max. 50 mA. The output transistors are driven in a floating state thus providing the user with optimal flexibility for evaluation of the output signals. It is therefore possible to use the output transistors either as emitter follower, open-collector, as a current source or in push-pull operation. When pin B is connected to V_{REF}, Q2 and Q4 can be used between 0 V and V_{REF}. The maximum base voltage of the output transistors can be set on pin B. If B is connected to V_{REF}, any constant current up to 50 mA can be set on the outputs by means of resistors on Q2 or Q4 (**see application circuits 2 and 3**).

Q1 through Q4 and also additional external output transistors can be protected against destruction by short-circuit or overload. This is the purpose of pin SC which turns off the output transistors periodically in the presence of overload.

By means of a capacitor on C_D it is possible to set the response delay and the turn-OFF time of short-circuit protection. The same capacitor also defines the turn-ON delay of the output stages when the supply voltage is applied, whereby the output stages are inhibited during buildup of the oscillator. Finally C_D produces a turn-OFF delay of the output stages to prevent the turn-ON delay from running its full length at brief voltage dips on V_S.

A switching regulator is incorporated for the voltage supply of the circuit when it is used as a two-wire AC proximity switch, and this is activated when pin V_T is connected to V_S. The circuit has a stabilized voltage of approx. 2.9 V that is brought out on pin V_{REF}.

Supply-voltage range: The operating range in normal operation is between 4 and 40 V. If pin V_{REF} is connected to V_S, the circuit is operating between 3.1 and 4.5 V. In this case, however, V_{REF} is no longer internally stabilized, i.e. the analog IC functions depend on the operating voltage.

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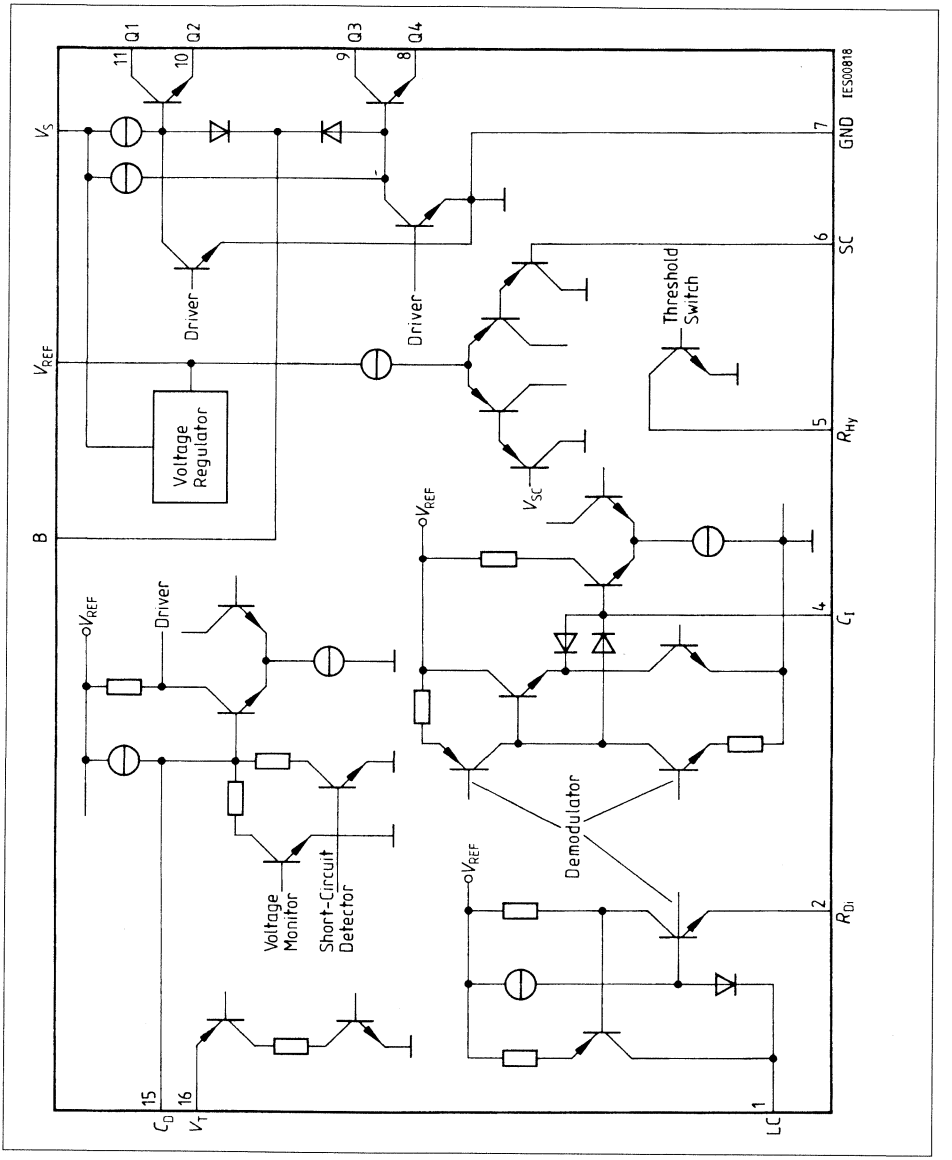

Circuit Diagram (simplified)

Pin Functions

Pin 1; LC

The resonant circuit of the proximity switch is connected between LC and ground.

Pin 2; R_{Di}

A resistor between this pin and ground sets the current in the oscillator circuit. The greater the value of the resistor, the smaller is the current feed from the oscillator into the resonant circuit and the greater therefore is the switching distance. The greater the Q of the resonant circuit, the greater is the value of the distance resistor necessary for setting a certain switching distance.

Pin 4; C_I

C_I can remain open; if high noise immunity is to be achieved however, this pin should be provided with a series RC element (R_I, C_I). If pin C_D is not used, a correctly dimensioned RC element on this pin will also prevent any erroneous pulses on the output when the supply voltage is turned on (**see application circuit 1**).

Pin 5; R_{Hy}

Depending on the status of the circuit, R_{Hy} will be high-impedance or low-impedance to ground (open collector). If the distance resistance (see R_{Di}) is split into two resistors R_{Di} and R_{Hy}, a distance hysteresis can be set by means of R_{Hy}. If series hysteresis is applied, R_{Hy} is connected in series with R_{Di} or shorted. If parallel hysteresis is applied, R_{Hy} is connected in parallel with R_{Di} or made high-impedance (**see application circuit 1**).

Pin 6; SC

SC serves for short-circuit sensing in the output circuit that is to be protected. The current can be sensed referred to ground or V_S. The current sensing is made by a dedicated resistor in the output circuit. For a voltage drop $\geq$ 0.3 V across V_S and SC or across ground and SC, all outputs are turned off after the turn-OFF delay (brief glitches on the outputs or the charging of line capacitances therefore do not trigger the short-circuit protection). After a pause about 200 times the turn-off delay, the outputs turn-ON again. If the short-circuit is still present, the turn-OFF cycle will start up anew.

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Both the internal output stages and externally connected output stages can be protected against sustained short-circuits or overload.

A limiting of the output current is an externally connected output stage during the turn-off delay must be ensured. Normally the current limiting by the β of the output transistor is sufficient, meaning that no further circuit devices are called for (**see application circuits**). The outputs Q1 to Q4 are already internally protected against overcurrent so that, in the case of a short-circuit, the current will not exceed 250 mA.

In order to prevent thermal overloads, the current-conducting output is to be connected to pin SC (**see application circuit 4**).

Pins 8, 9, 10, 11; Outputs Q1, Q2, Q3, Q4

Q1 is the open collector, Q2 the open emitter of one output transistor, Q3 the open collector and Q4 the open emitter of the second output transistor in antiphase with the first output transistor (**see operation schematic**). Q1 and Q3 or Q2 and Q4 can be connected in parallel as required. The function of the outputs is ensured when the emitter potential of the output transistors (Q2, Q4) is between 0 V and the voltage on pin B. If B is not connected, the operating range of Q2 and Q4 extends to approx. $V_S - 2$ V. For current setting on the outputs, **see pin B**.

Pin 12; V_S

Outputs Q1 through Q4 are inhibited as long as the voltage on V_S is below approx. 3.6 V. They are enabled between approx. 3.6 and 4 V, the basic function of the circuit is then ensured. During the turn-ON and turn-OFF of V_S there are consequently no undesirable static states. The operating data and characteristics apply upwards from 4 V. See pin C_D for the avoidance of erroneous pulses during oscillator buildup.

Pin 13; V_{REF}

The internal stabilized voltage of the IC of approx. 2.9 V appears on this pin. A capacitor can be connected between V_{REF} and ground to improve the noise immunity of the overall circuit function. If V_{REF} is connected to V_S, it is possible to operate the circuit in a supply-voltage range of 3.1 through 4.5 V. In this case V_{REF} is no longer stabilized. The analog functions of the circuit e.g. switching distance, however, are then dependent on the supply voltage.

Pin 14; B

This pin serves for limiting the base voltage of the internal output-stage transistors. If this pin is connected to V_{REF} for example, it is possible to set a constant output current ($I_Q = V_{REF}$ / external resistor) that is independent of the supply voltage by means of an external resistor across Q2 (or Q4) and ground (watch out for power dissipation!).

Pin 15; C_D

A capacitor on this pin delays the activation of the outputs after the supply voltage is applied (turn-ON delay). In this way erroneous pulses are prevented on the output during buildup of the oscillator.

If V_S falls to less than 3.6 to 4 V, the outputs are not inhibited until after a turn-OFF delay time, this also being determined by C_D. In this way the delayed turn-ON operation described above is suppressed if there are just short glitches (voltage dips) on V_S. This is of particular advantage for large core diameters, because in such cases a relativity long turn-ON delay has to be selected and the delayed twin-on operation would otherwise be activated each time there was a brief voltage dip.

The capacitor C_D also sets the turn-off delay and the pause duration in short-circuit operation. The sample / pause ratio is approx. 1:200 (**see pin SC**).

If these functions can be dispensed with, C_D can remain open.

Pin 16; V_T

If this pin is connected to + V_S, the supply voltage of the IC (when used as a two-wire proximity switch) can be generated by switching the outputs. The quiescent current can then be kept low. This mode is primarily suitable for AC switches with power supply by phase-control.

The switching of the outputs is made in a V_S range of 6 to 8 V. At 8 V the outputs are turned on, until V_S falls to 6 V. At 6 V the outputs are inhibited, until V_S again reaches 8 V. In this mode V_S should not exceed 14 V or fall below 4 V.

Absolute Maximum Ratings

T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 0.3	42	V	
Output voltages B open B connected	V_{Q1}; V_{Q3} V_{Q2}; V_{Q4} V_{Q2}; V_{Q4}	– 1 – 1 – 1	41 V_S + 1 V_B	V V V	V_{Q2}; $V_{Q4} \leq V_S$ V_{Q2}; V_{Q1}; V_{Q4} < V_{Q3}
Output currents	I_{Q1}; I_{Q3} – I_{Q2}; – I_{Q4}	0 0	60 60	mA mA	does not apply to shortcircuit
Voltage on V_T	V_T	– 0.3	14	V	
Current on V_{REF}	– I_{REF}	0	100	µA	
Voltage on SC	V_{SC}	0	V_S	V	
Current from R_{Di}	– I_{RDi}	0	2	mA	
Current to R_{Hys}	I_{RHy}	0	2	mA	
Voltage on B	V_{SB}	– 0.3	V_S	V	
Storage temperature	T_{stg}	– 55	110	°C	
Thermal resistance (system - air)	$R_{th\,SA}$ $R_{th\,SA}$		81 110	K/W K/W	P-DIP-16 P-DSO-16-1
Junction temperature	T_j T_j		110 150	°C °C	 max. 70.000 h
Capacitor	C_V		50	nF	applies to short-circuit at the TCA 505 B only

Operating Range

Supply voltage	V_S	4 3.1	40 4.5	V V	 $V_{REF} = V_S$
Ambient temperature	T_A	– 40	110	°C	
Distance and Hysteresis resistance R_{Di} and R_{Hy} in series R_{Di} and R_{Hy} parallel	 R_{Di} R_{Hy} R_{Di}/R_{Hy}	 300 0 300		 Ω Ω Ω	
Output voltage on Q2, Q4 B open B connected	 V_{Q2}; V_{Q4} V_{Q2}; V_{Q4}	 – 0.3 – 0.3	 V_S – 2 V_B	 V V	

Only the circuitry provided for passive components may be connected to pins LC, R_{Di}, C_I, C_D

Characteristics
4 V ≤ V_S ≤ 40 V; T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Power Supply (V_S)						
Current consumption Normal mode (S1 = S2 = OFF) Two-wire operation S1 = ON, S2 = OFF 4 V ≤ V_S ≤ 12 V	 I_S I_S		 550 625	 740 840	 µA µA	 1 1
Turn-ON threshold (outputs active) S1 = OFF	V_{TON1}		3.64	4	V	1
Turn-OFF threshold (outputs disabled) S1 = OFF	V_{TOFF1}	3.0	3.6		V	1
Hysteresis $V_{TON1} - V_{TOFF1}$ S1 = OFF	ΔV_{Hy1}		40		mV	1
Oscillator (LC, R_{Di})						
Oscillator frequency	f_{OSC}			3	MHz	1
Oscillator amplitude	A_{OSC}		0.8		V_{pp}	1
Demodulator, Threshold Switch (C_I, R_{Hy})						
Threshold on C_I	V_{CI}		2		V	1
Hysteresis on C_I	V_{HyCI}		0.8		V	1
Current in C_I	I_{CI}		7		µA	1
Current from C_I	$-I_{CI}$		6		µA	1
Switching frequency C_I < 50 pF	f_S		5		kHz	1 (L = 70 µH)
Reference Voltage (V_{REF}); Base Output Transistors						
Reference voltage I_{REF} = 0 to 100 µA	V_{REF}	2.65	2.9	3.10	V	
Offset voltage $V_B = V_{Q2,4}$ $V_B = V_{REF}$; $I_{Q2,4}$ = 5 mA	V_{OB}		110	155	mV	1

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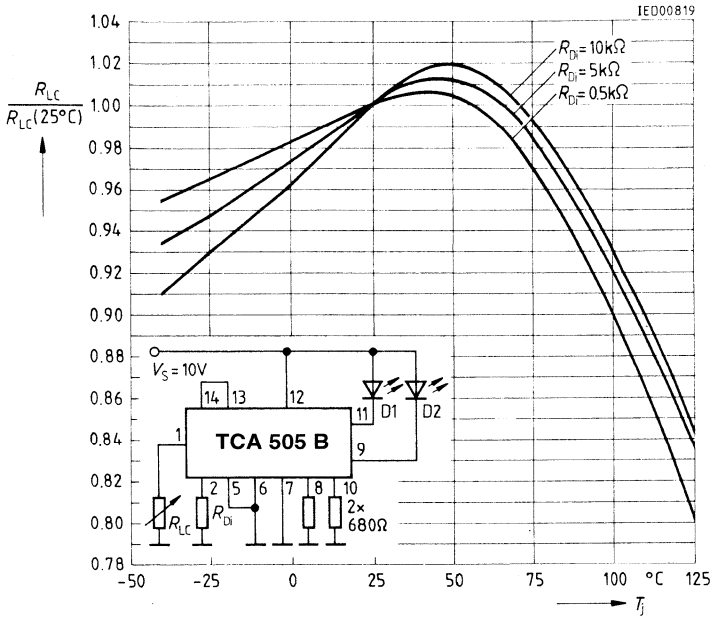
Characteristics (cont'd)
4 V ≤ V_S ≤ 40 V; T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values			Unit	Test Circuit
		min.	typ.	max.		
Two-Wire Regulator (V_T)						
Turn-ON threshold (outputs active) S1 = ON	V_{TON2}	6.7	8	9.3	V	1
Turn-ON threshold (outputs disabled) S1 = ON	V_{TOFF2}	5.0	6	7.0	V	1
Hysteresis $V_{TON2} - V_{TOFF2}$, S1 = ON	ΔHy_2	1.6	2	2.4	V	1
Turn-ON, Turn-OFF and Short-Circuit Delay (C_D)						
Turn-ON delay S1 = OFF	t_{DON}	0.49	0.65	0.82	ms/nF	2
Turn-OFF delay S1 = OFF; $V_S \geq 3.6$ V	t_{VA}	17.0	25	34.0	µs/nF	2
Shortcircuit turn-off delay S1 = OFF	t_{SC}	1.70	2.5	3.40	µs/nF	2
Shortcircuit pause S1 = OFF	t_P	0.36	0.5	0.65	ms/nF	2
Outputs (Q1, Q2, Q3, Q4)						
Residual voltage Q1-Q2, Q3-Q4 SQ2 0-1 = ON, SQ4 0-1 = ON S1 = OFF	V_{QRes}					
I_Q = 5 mA	V_{QR}		0.10	0.14	V	1
I_Q = 60 mA	V_{QR}		0.5	0.99	V	1
I_Q = 60 mA	V_{QR}	$V_S - 2.2$	$V_S - 1.8$		V	1
Reverse current on Q1, 3	I_{QR}			10	µA	
Residual current on Q2, 4*) Q2, 4 conducting but Q1, 3 open	I_{Qres}			50	µA	1
In case of short-circuit output current	I_{QSC}		300	500	mA	1
Shortcircuit Detector (SC)						
Trigger level ref. to V_S, S1 = OFF	V_{SCS}	0.255	0.3	0.345	V	1
Trigger current S1 = OFF	I_{SCS}			30	µA	1
Trigger level ref. to ground S1 = OFF	V_{SCO}	0.255	0.3	0.345	V	1
Trigger current S1 = OFF	$-I_{SCO}$			6	µA	1

Diagrams

Temperature Response of Switching Point



Resistor R_{LC} is set in each case so that the TCA 505 B just switches from D2 to D1. In this way the TCA 505 B, together with a suitably dimensioned resonant circuit, can form a proximity switch that exhibits a very good temperature coefficient (± 2.5 %) over the entire temperature range and without any kind of extra external wiring.

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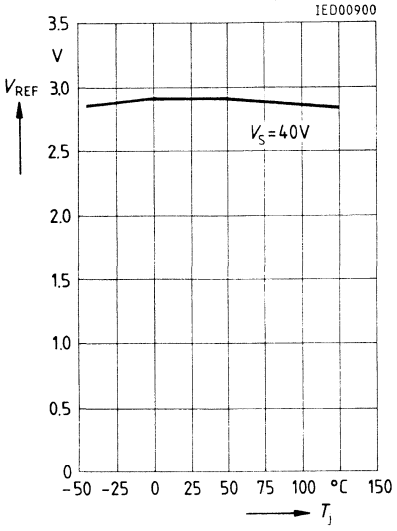
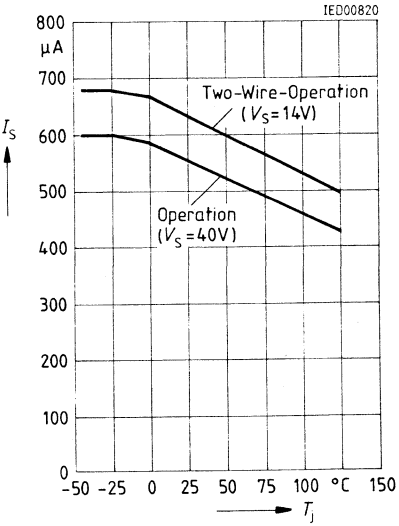
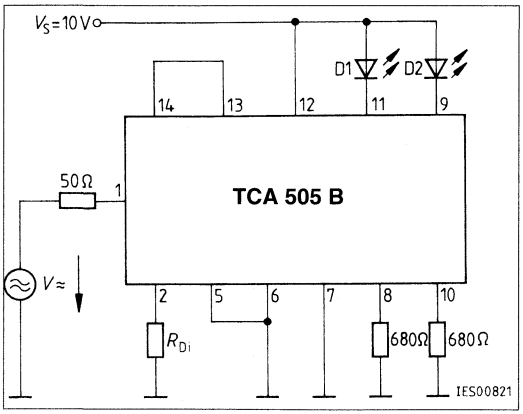
Diagrams

Reference Voltage versus Junction Temperature T_j

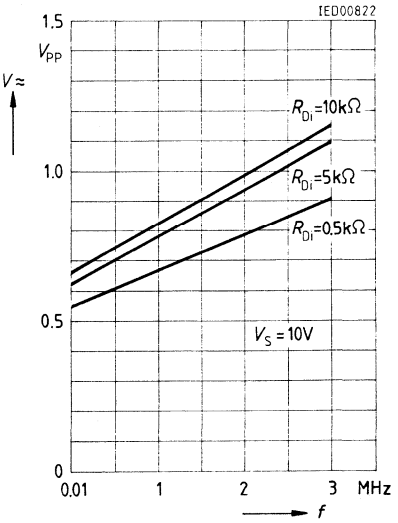


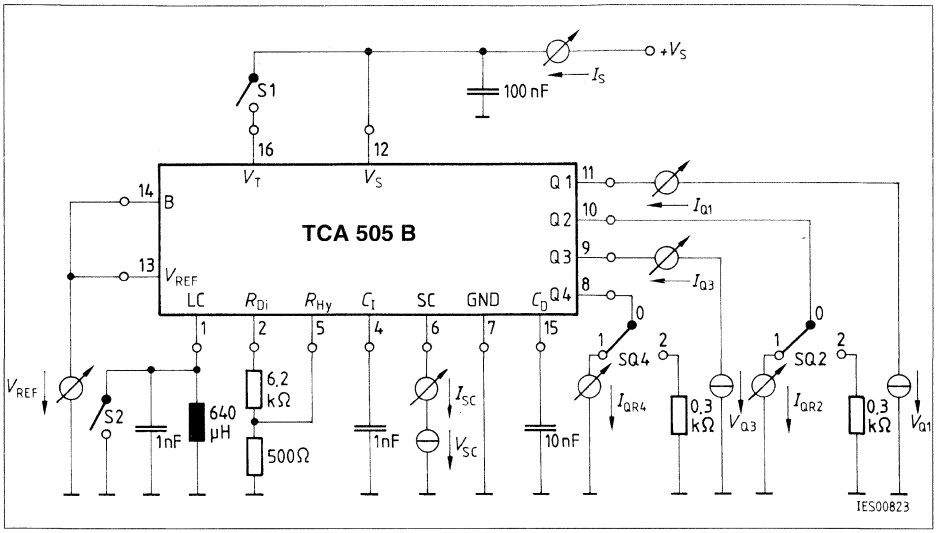
Current Consumption versus Junction Temperature T_j



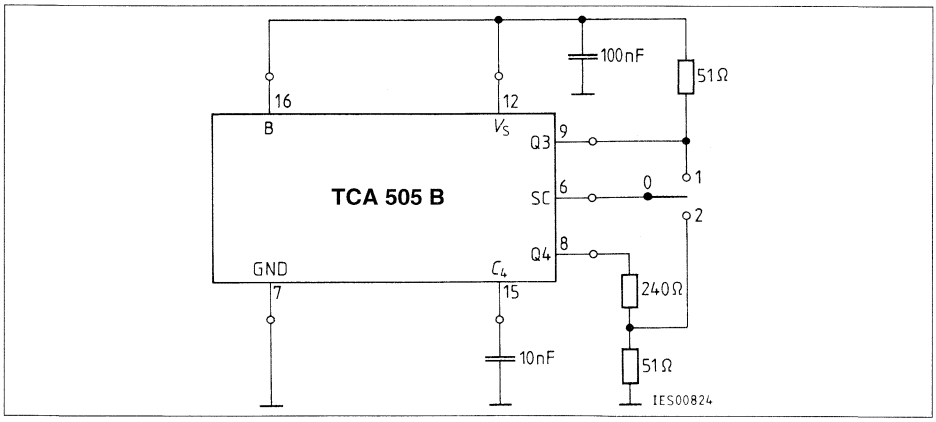


Switching Amplitude versus Frequency f





Test Circuit 1



Test Circuit 2

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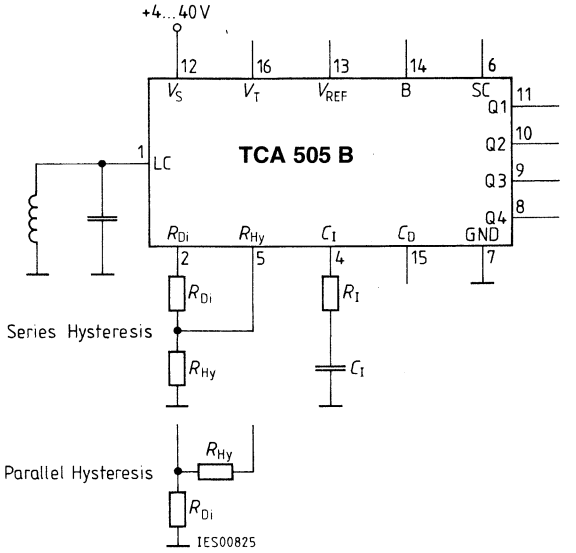
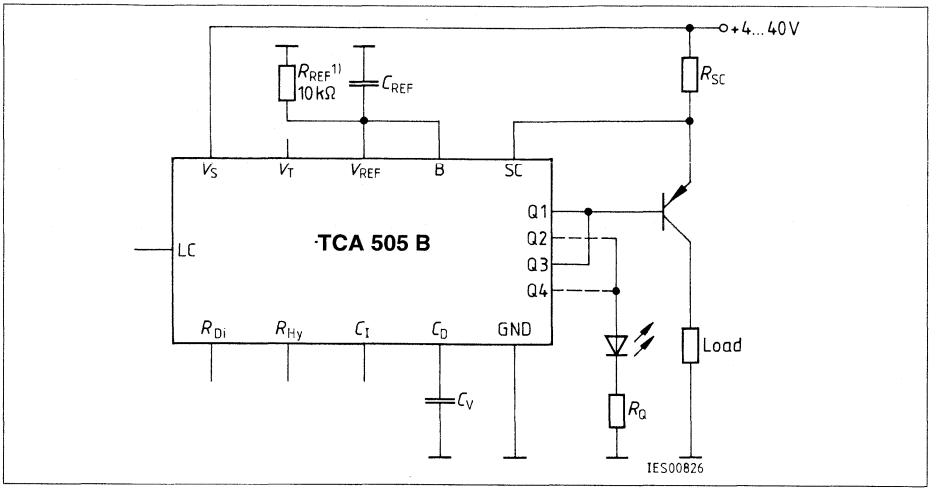


For explanation see under "Pin Functions".

Application Circuit 1
Input Circuitry (Use of pins LC, R_{Di}, R_{Hy}, C_I)



Application Circuit 2

Output Circuitry (Use of pins V_{REF}, B, SC, Q1 through Q4, C_D)

P-switch, short-circuit-proof, LED indicator, configurable as normally closed or normally open

Short-circuit-current sampling: $R_{SC} = \dfrac{0.3\ V}{\text{max. load current}}$

Constant base current: [1] $R_Q = \dfrac{2.9\ V - V_{LED}}{\text{max. base current}}$

For dimensioning of C_D **see characteristics.** C_D is usually between 1 and 10 nF. Filtering of V_{REF} is for noise immunity. C_{REF} can be 10 nF for example.

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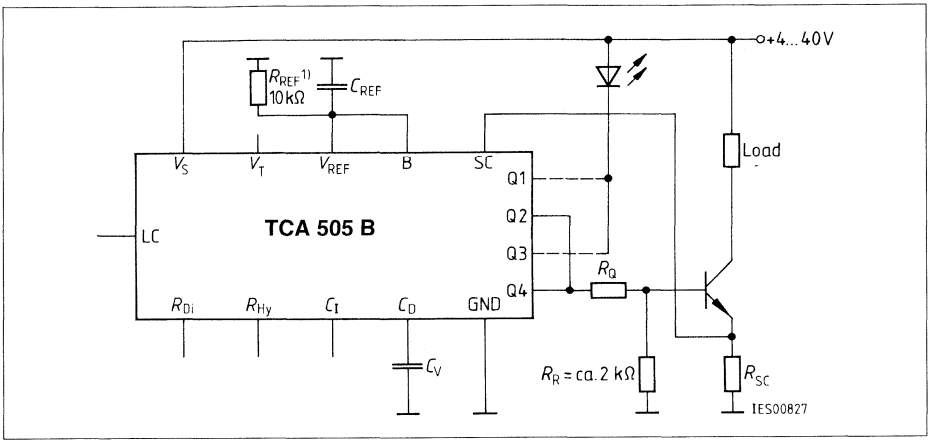
[1] When I_Q > 10 mA, a resistor R_{REF} on pin V_{REF} will improve the constant current operation.



Application Circuit 3

Output Circuitry (Use of pins V_{REF}, B, SC, Q1 through Q4, C_D)

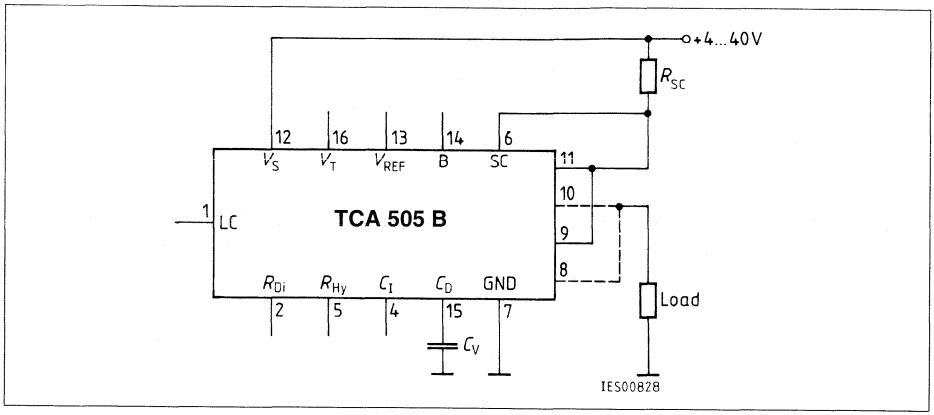
N-switch, short-circuit-proof, LED indicator, configurable as normally closed or normally open

Short-circuit-current sampling: $$R_{SC} = \frac{0.3\ V}{\text{max. load current}}$$

Constant base current: [1] $$R_Q = \frac{2\ V}{\text{max. base current} + I_{RR}}$$

For dimensioning of C_D **see characteristics**. C_D is usually between 1 and 10 nF. Filtering of V_{REF} is for noise immunity. C_{REF} can be 10 nF for example. R_{REF} serves for discharging residual current of outputs Q2, 4.

1) When I_Q > 10 mA, a resistor R_{REF} on pin V_{REF} will improve the constant current operation.



Application Circuit 4

Output Circuitry (Use of pins SC, Q1 to Q4, C_D)

P-switch, short-circuit-proof, configurable as normally closed or normally open

Short-circuit-current sampling: $R_{SC} = \frac{0.3\ V}{\text{max. load current}}$

During the sampling time, the short-circuit current within the IC is limited to a maximum of 250 mA. For dimensioning of C_V, **see characteristics**. C_D is usually between 1 and 10 nF.

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SIEMENS

IC for Inductive Proximity Switches with 0.5 A Output Stage

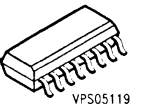
TCA 705

Advance Information

SPT IC

Features

- Output current up to 500 mA
- Switch-ON and switch-OFF
- High-side-switch and low-side-switch
- Short-circuit and overload protection
- Supply voltage range from 7.5 V to 65 V
- Few external components
- LED output for "switch-ON/OFF" and short-circuit failure indication
- High switching frequency
- High noise immunity, low temperature coefficient
- Temperature protection

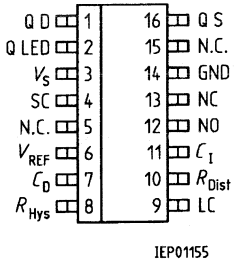


P-DSO-16-1

Type	Ordering Code	Package
▼ TCA 705 G	Q67000-A8310	P-DSO-16-1 (SMD)

▼ New type

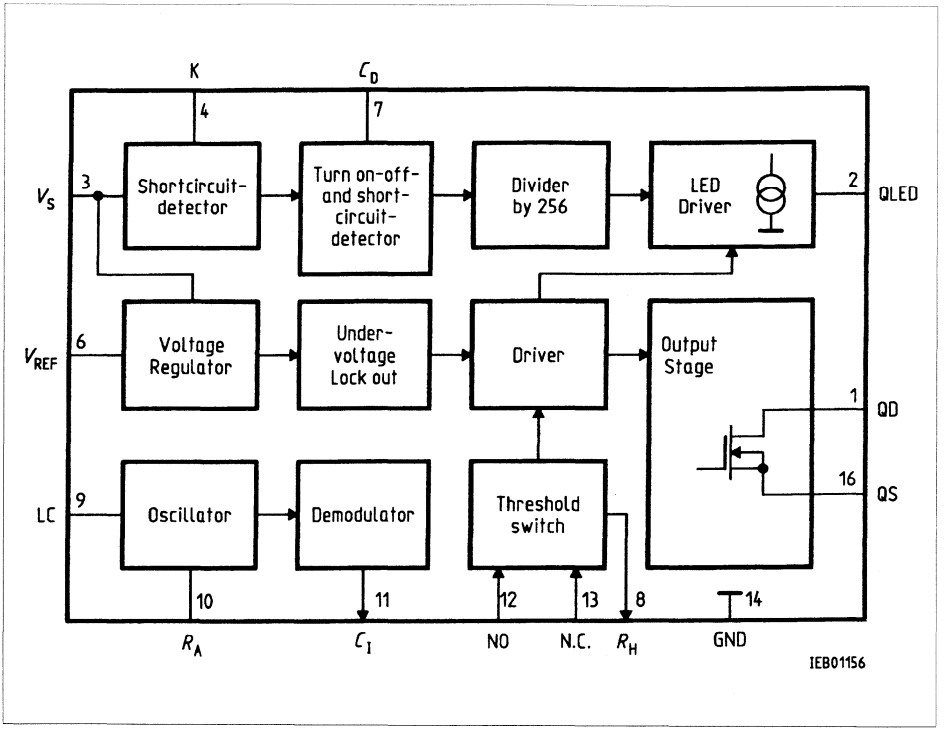
The TCA 705 is a monolithic IC in the new Smart Power Technology (SPT) for designing excellent inductive proximity switches at low cost and with little space. Features like 0.5 A output current, short-circuit, overload and temperature protection classify the TCA 705 as a versatile general-purpose circuit. The separate LED output indicates the switching state of the sensor (switch-ON / switch-OFF) and an eventual short-circuit failure.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	QD	Output; open drain
2	Q LED	Output LED
3	V_S	Supply voltage
4	SC	Short-circuit detector
5	N.C.	Not connected
6	V_{REF}	Reference voltage
7	C_D	Turn-ON delay / Turn-OFF delay / Short-circuit delay
8	R_{Hys}	Hysteresis
9	LC	Oscillator
10	R_{Dist}	Distance
11	C_I	Integrating capacitance
12	NO	Input driver (normally open)
13	NC	Input driver (normally closed)
14	GND	Ground
15	N.C.	Not connected
16	QS	Output; open source



Block Diagram

Pin Functions

Pins 1/16: QD, QS

A load has to be connected between QS and ground, i.e. high-side switch respectively between QD and V_S, i.e. low-side switch. The current through the load is 500 mA max. To protect the IC against destruction by short-circuit or overload, a capacitor has to be connected between pin C_D and ground.

Pin 2: Q LED

Output QLED drives a LED with up to 10 mA, connected between QLED and V_S. The LED indicates the switching state (switch-ON / switch-OFF) and blinks during an eventual short-circuit failure.

Pin 3: V_S

Outputs QD , QS and QLED are inhibited as long as the voltage on V_S is below approx. 7.5 V. They are enabled between approx 8.0 and 8.5 V, the basic function of the circuit is then ensured. During the turn-ON and turn-OFF of V_S there are consequently no undesirable static states. The operating data and characteristics apply upwards from 8.5 V. See pin C_D for the avoidance of erroneous pulses during oscillator built-up.

Pin 4: SC

SC serves for short-circuit sensing in the output circuit that is to be protected. The current can be sensed referred to ground or V_S (**see application circuits 2 and 3**). The current sensing is made by a dedicated resistor (R_{SC}) in the output circuit. For a voltage drop ≥ 0.3 V across V_S and SC or across ground and SC, all outputs are turned off after the turn-OFF delay (brief glitches on the outputs or the charging of line capacitances therefore do not trigger the short-circuit protection). After a pause of about 200 times of the turn-OFF delay, the outputs turn on again. If the short-circuit is still present, the turn-OFF cycle will start up a new.

Pin 6: V_{REF}

The internal stabilized voltage of the IC of approx. 3.5 V appears on this pin. A capacitor can be connected between V_{REF} and ground to improve the noise immunity of the overall circuit function. The output current at this pin is up to 10 mA.

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Pin 7: C_D

A capacitor on this pin delays the activation of the output after the supply voltage is applied (turn-ON delay). In this way erroneous pulses are prevented on the output during built-up of the oscillator.

If V_S falls to less than 7.8 to 8 V, the output is not inhibited until after a turn-OFF delay time, this also being determined by C_D. In this way the delayed turn-ON operation described above is suppressed if there are just short glitches (voltage dips) on V_S. This is of particular advantage for large core diameters, because in such cases a relatively long turn-ON delay has to be selected, since this would otherwise start to run every time there was a brief voltage dip.

The capacitor C_D also sets the turn-OFF delay and the pause duration in short-circuit operation.

Pin 8: R_{Hys}

Depending on the status of the circuit, R_{Hys} will be high-impedance or low-impedance to ground (open collector). If the distance resistance (see R_{Dist}) is split into two resistors R_{Dist} and R_{Hys}, a distance hysteresis can be set by means of R_{Hys}. If series hysteresis is applied, R_{Hys} is connected in series with R_{Dist} or shorted. If parallel hysteresis is applied, R_{Hys} is connected in parallel with R_{Dist} or made high-impedance **(see application circuit 1)**.

Pin 9: LC

The resonant circuit of the proximity switch is connected between LC and ground.

Pin 10: R_{Dist}

A resistor between this pin and ground sets the current in the oscillator circuit. The greater the value of the resistor, the smaller is the current feed from the oscillator into the resonant circuit and the greater therefore is the switching distance. The greater the quality of the resonant circuit, the greater is the value of the distance resistor necessary for setting a certain switching distance.

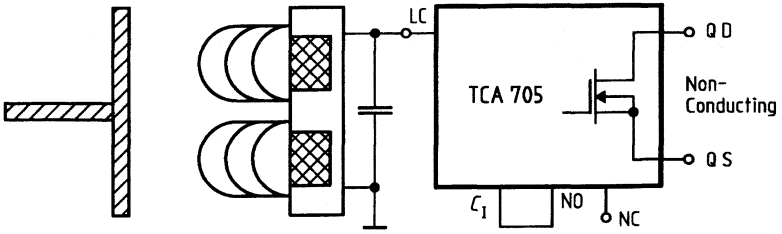
Pin 11: C_I

C_I can remain open; if high noise immunity is to be achieved however, this pin should be provided with a serial RC element (R_I, C_I). If pin 7 (C_D) is not used, a correctly dimensioned RC element on pin C_I will also prevent any erroneous pulses on the output when the supply voltage is turned on **(see application circuit 1)**.

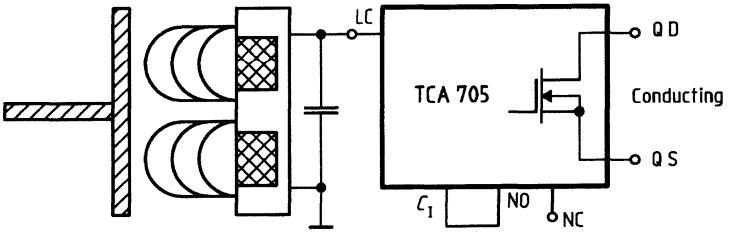
Pins 11/12/13: C_I, NO, NC

A direct connection between C_I and NO will result in a "normally open" output stage, i. e. switch-ON. A direct connection between C_I and NC will result in a "normally closed" output stage, i. e. switch-OFF.

Resonant circuit, normally open, not damped:



Resonant circuit, normally open, damped:



	Not Damped	Damped
Normally Open C_I/NO	Non-Conducting	Conducting
Normally Closed C_I/NC	Conducting	Non-Conducting

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Operational Diagram

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Functional Description

This circuit is used to design inductive proximity switches. The resonant circuit of the LC oscillator is implemented with an open half-pot ferrite and a capacitor in parallel (pin LC). If a metallic target is moved closer to the open side of the half-pot ferrite, energy is drawn from the resonant circuit and the amplitude of the oscillation is decreasing accordingly. This change in amplitude is transmitted to a threshold switch by means of a demodulator and triggers the output **(see operation schematic)**.

By means of an external distance resistor R_A on the oscillator (pin R_{Dist}) it is possible to set the switching distance within wide limits. The optimal distances are 0.1 to 0.6 of the diameter of the half-pot ferrite in use, but extensions to both of these parameters can also be produced. The circuit also enables the setting of a path hysteresis by switching an external distance resistor (R_H) via pin R_{Hys} **(see application circuit 1)**.

The device includes one integrated output stage for max. 500 mA output current. It can be used as "normally open" or "normally closed" by means of programming the NO-respectively NC-input driver and as a high-side- or low-side-switch **(see application circuits 2 and 3)**. The output stage is automatically protected against destruction by short-circuit or overload.

By means of a capacitor on pin C_D it is possible to set the response delay and the turn-OFF time of short-circuit protection. The same capacitor also defines the turn-ON delay of the output stage when the supply voltage is applied, whereby the output stage is inhibited during built-up of the oscillator. Finally C_D is used to produce a turn-OFF delay of the output stage so that the turn-ON delay is prevented from running its full length if there are brief voltage dips on V_S.

Absolute Maximum Ratings

T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage	V_S	– 0.3	70	V	–
Output voltage	V_Q	– 0.3	V_S + 1	V	–
Output current	$-I_Q$	–	–	–	internally limited
Current from V_{REF}	$-I_{REF}$	0	1	mA	–
Voltage on SC	V_{SC}	0	V_S	V	–
Current from R_{Dist}	$-I_{RDist}$	0	2	mA	–
Current to R_{Hys}	I_{RHys}	0	2	mA	–
Storage temperature	T_{stg}	– 65	125	°C	–
Thermal resistance (system-air)	$R_{th\ SA}$	–	110	K/W	–
Junction temperature	T_j T_j	– –	125 150	°C °C	– max. 70.000 h
Capacitor on C_D	C_V	–	50	nF	–

Operating Range

Supply voltage	V_S	7.5	65	V	–
Ambient temperature Distance and hysteresis resistance	T_A	– 40	110	°C	–
R_A and R_H in series	R_A R_H	300 0	– –	Ω Ω	– –
R_A and R_H parallel	R_A / R_H	300	–	Ω	–
Output current	$-I_Q$	–	500	mA	–

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Characteristics

7.5 V ≤ V_S ≤ 65 V; T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Power Supply (V_S)					
Current consumption	I_S	–	550	750	µA
Turn-ON threshold (output active)	V_{TON1}	–	8.0	8.5	V
Turn-OFF threshold (output disabled)	V_{TOFF1}	7.5	8.0	–	V
Hysteresis $V_{TON1} - V_{TOFF1}$	ΔV_{Hys1}	–	40	–	mV
Reference Voltage	V_{REF}	3.0	3.3	3.5	mV
Oscillator (LC, R_{Dist})					
Oscillator frequency	f_{OSC}	–	–	3	MHz
Oscillator amplitude	A_{OSC}	–	0.8	–	V_{PP}
Demodulator, Threshold Switch (C_I, R_{Hys})					
Threshold on C_I	V_{CI}	–	2	–	V
Hysteresis on C_I	V_{HysCI}	–	0.8	–	V
Current in C_I	I_{CI}	–	7	–	µA
Current from C_I	$-I_{CI}$	–	6	–	µA
Switching frequency (C_I < 50 pF)	f_S	–	5	–	kHz
Integrating capacitance	C_I	–	1	–	nF
Reference Voltage (V_{REF})					
Reference voltage I_{REF} = 0 to 1 mA	V_{REF}	3.0	3.3	3.5	V
Turn-ON, Turn-OFF and Short-Circuit Delay (C_D)					
Turn-ON delay	t_{DON}	0.48	0.65	0.82	ms/nF
Turn-OFF delay	t_{VA}	17.0	25	34.0	µs/nF
Short-circuit turn-OFF delay	t_{SC}	1.70	2.5	3.40	µs/nF
Short-circuit pause	t_P	0.35	0.5	0.65	ms/nF

Characteristics (cont'd)

7.5 V ≤ V_S ≤ 65 V; T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Outputs (QD, QS, Q LED)					
Current on Q LED	I_{QLED}	–	–	10	mA
	R_{DSON}	0.3	–	0.5	Ω
Residual current on QD, QS	I_{QRES}	–	–	100	µA
Short-Circuit Detector (SC)					
Trigger level ref. to V_S	V_{SCS}	0.255	0.3	0.345	V
Trigger current	I_{SCS}	–	–	30	µA
Trigger level ref. to ground	V_{SCO}	0.255	0.3	0.345	V
Trigger current	$-I_{SCO}$	–	–	6	µA

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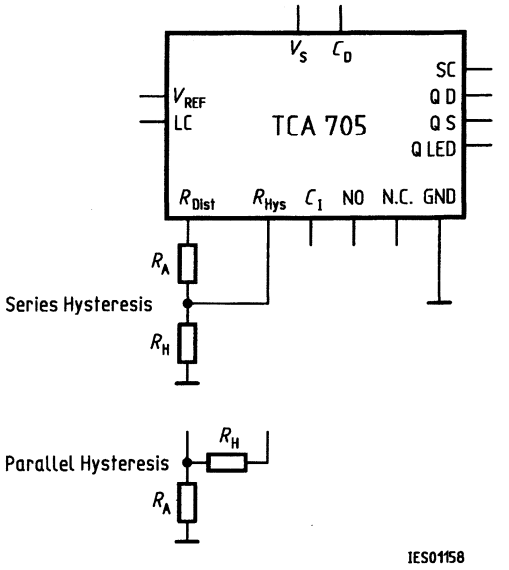
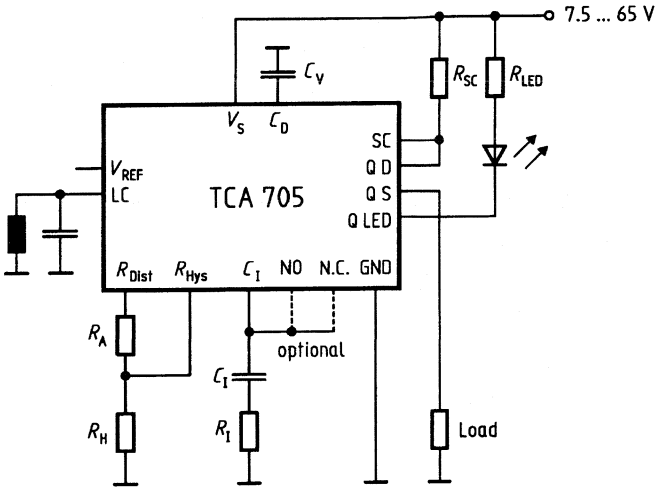


Application Circuit 1
Series Hysteresis / Parallel Hysteresis

For explanation see under "Pin Functions".



High-side-switch, short-circuit-proof, LED indicator, normally closed (normally open).

Short-circuit sensing: $R_{SC} = \frac{0.3\ V}{max.\ I_Q}$

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Application Circuit 2

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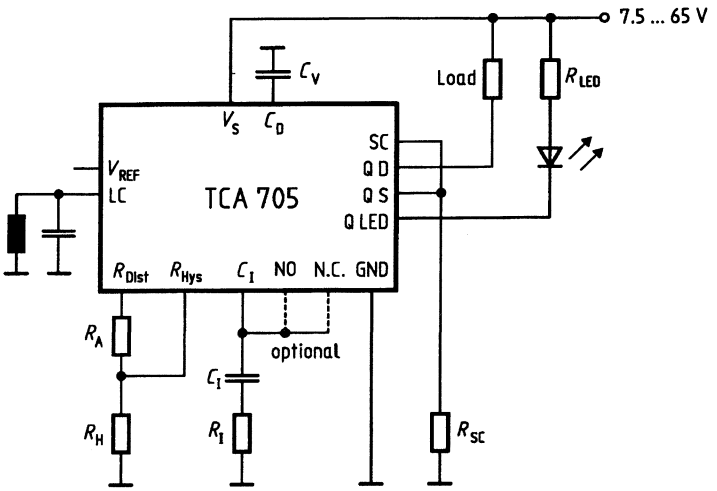

Low-side-switch, short-circuit-proof, LED indicator, normally open (normally closed).

Short-circuit sensing: $R_{SC} = \frac{0.3\ V}{max.I_Q}$

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Application Circuit 3

Selector Guide

Type	Package	Features	Temperature Range	Page
SAE 81C52 P	P-DIP-16	Static CMOS RAM 256 × 8 bits SAB 8051-compatible	– 40 ... 110 °C	875
SAE 81C52 G	P-DSO-20-1			
SAE 81C54 P	P-DIP-16	Static CMOS RAM 512 × 8 bits SAB 8051-compatible	– 40 ... 110 °C	882
SAE 81C80 A	P-LCC-44	Dual Port RAM 504 × 8 bits Multiprocessor system	– 40 ... 110 °C	889
SDE 2506 A2	P-DIP-8	EEPROM 128 × 8 Bit 3-line bus	– 40 ... 110 °C	909
SDE 2526 A2	P-DIP-8	EPPROM 256 × 8 Bit I^2C bus	– 40 ... 110 °C	919
SDE 2526 A2G	P-DSO-8-1	EPPROM 256 × 8 Bit I^2C bus	– 40 ... 110 °C	919

= SMD

256 x 8-Bit Static CMOS RAM NMOS-Compatible

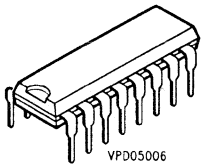
SAE 81C52

Preliminary Data

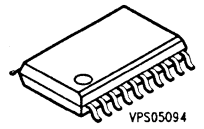
CMOS IC

Features

- 256 × 8-bit organization
- Standby mode
- Compatible with the NMOS and CMOS versions of the microprocessor/microcontroller families SAB 8086, SAB 8051
- Very low power dissipation
- Data retention up to $V_{DD} \geq 1$ V
- Three different chip select inputs for two chip select modes
- No increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range – 40 to 110 °C



P-DIP-16



P-DSO-20-1

Type	Ordering Code	Package
S SAE 81C52 P	Q67100-H9017	P-DIP-16
S SAE 81C52 G	Q67100-H9015	P-DSO-20-1 (SMD)

The SAE 81C52 is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus interfaces directly to 8-bit microprocessors/microcontrollers without any timing or level problems, e.g. the families SAB 8086, SAB 8051.

All inputs and outputs are fully compatible with NMOS circuits, except CS 1. Data retention is ensured up to $V_{DD} \geq 1.0$ V. The SAE 81C52 has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD 0 ... AD 7) and the control lines ($\overline{WR}$, $\overline{RD}$, ALE, CS2, $\overline{CS3}$), or only the control lines $\overline{RD}$, $\overline{WR}$.

The power consumption is max. 5.5 µW in standby mode and max. 16.5 mW in operation. In standby mode, the power consumption will not increase if the controls inputs are on undefined potential.

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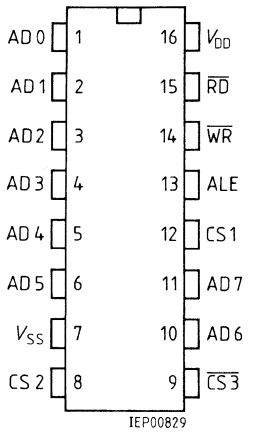
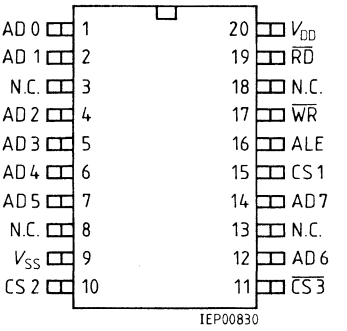
SAE 81C52 P



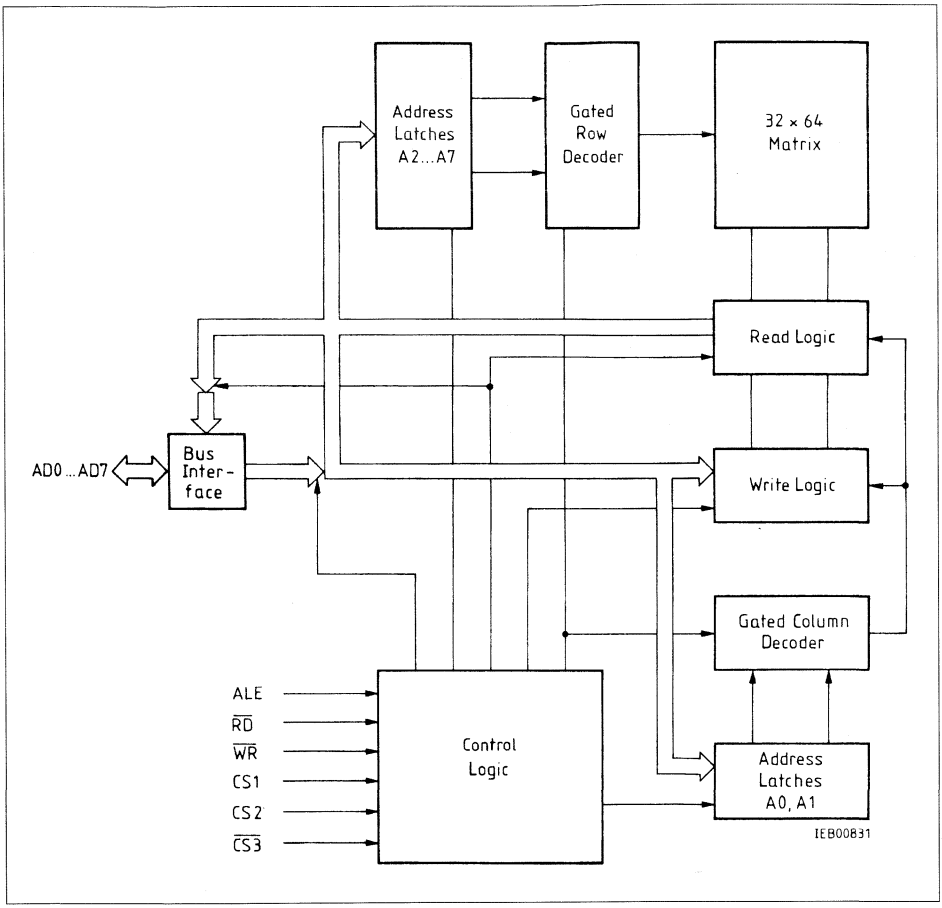
SAE 81C52G



Pin Configurations
(top view)

Pin Definitions and Functions

SAE 81C52 G	SAE 81C52 P	Symbol	Function
Pin	**Pin**		
1, 2, 4, 5, 6 7, 12, 14	1 ... 6 10, 11	AD 0 ... 7	Address/data lines
15	12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17	14	$\overline{WR}$	Write enable
19	15	$\overline{RD}$	Read enable
20	16	V_{DD}	Power supply
9	7	V_{SS}	GND (0 V)
10	8	CS 2	Chip select 2; inhibits control inputs $\overline{RD}$, $\overline{WR}$
11	9	$\overline{CS\,3}$	Counterpart to CS 2



Block Diagram

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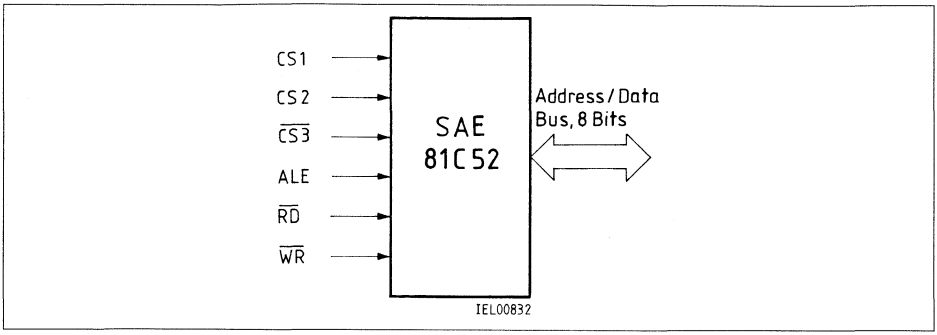

Logic Symbol

Truth Table

CS 1	CS 2	CS 3	ALE	RD	WR	AD 0 ... AD 7	Function
L	*	*	*	*	*	Floating (tristate)	Standby
H	X	X	H	H	H	Addresses to memory	Store addresses
H	H	L	L	L	H	Data from memory	Read
H	H	L	L	H	L	Data to memory	Write
H	L	X	L	X	X	Floating (tristate)	None
H	X	H	L	X	X	Floating (tristate)	None

*: Level = V_{SS} ... V_{DD}
X: Level = low or high

Absolute Maximum Ratings
T_A = – 40 to 110 °C

Parameter	Symbol	Limit Values	Unit
Supply voltage referred to GND (V_{SS}) All input and output voltages	V_{DD} V_{IM}	0 to 6 V_{SS} – 0.3 V_{DD} + 0.3	V V V
Total power dissipation Power dissipation for each output	P_{tot} P_Q	250 50	mW mW
Junction temperature Storage temperature	T_j T_{stg}	125 – 55 to 125	°C °C
Thermal resistance system - air P-DIP-16 P-DSO-20-1	 $R_{th\ SA}$ $R_{th\ SA}$	 70 95	 K/W K/W

Operating Range

Supply voltage	V_{DD}	4.5 to 5.5	V
Ambient temperature	T_A	– 40 to 110	°C

DC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 4.25 V to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Standby supply current	I_{DD}	–	1	µA	V_{DD} = 5.5 V; T_A = 25 °C; V_{CS1} = 0 V
Supply current	I_{DD}	–	3	mA	Δt_{cyc} = 1 µs; V_{DD} = 5.5 V; C_L = 100 pF
Standby voltage for data retention	V_{DD}	1.0	–	V	–
L-input current (for each input)	I_{IL}	–	1	µA	V_I = 0 to V_{DD}
Output leakage current	I_{QLK}	–	1	µA	V_Q = 0 to V_{DD} tristate
L-input voltage	V_{IL}	V_{SS}	0.8	V	–
H-input voltage	V_{IH}	2.2	V_{DD}	V	–
L-output voltage	V_{QL}	–	0.4	V	I_{QL} = 1 mA
H-output voltage	V_{QH}	2.6	–	V	I_{QH} = 1 mA
L-input voltage CS1	V_{IL}	V_{SS}	1	V	–
H-input voltage CS1	V_{IH}	V_{DD} – 1	V_{DD}	V	–

AC Characteristics

T_A = – 40 to 110 °C[1]; V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LHLL}	100	–	ns
ALE low before $\overline{RD}$ low	t_{LLRL}	50	–	ns
$\overline{RD}$ high before ALE high	t_{RHLH}	18	–	ns
ALE low before $\overline{WR}$ low	t_{LLWL}	50	–	ns
$\overline{WR}$ high before ALE high	t_{WHLH}	18	–	ns
Address setup before ALE	t_{AVLL}	18	–	ns
Address hold after ALE	t_{LLAX}	30	–	ns
$\overline{WR}$ or $\overline{RD}$ pulse width	t_{WLWH}	250	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	18	–	ns
Data hold after $\overline{RD}$	t_{RHDX}	–	90	ns
Chip select (2, 3) before $\overline{RD}$, $\overline{WR}$	t_{CS}	50	–	ns
Chip select (2, 3) after $\overline{RD}$, $\overline{WR}$	t_{SC}	18	–	ns
Chip select 1 before ALE	t_{CSLH}	20	–	ns
Chip select 1 after $\overline{RD}$, $\overline{WR}$	t_{CSWH}	50	–	ns
Output delay time	t_{RLDV}	–	200	ns
Input capacitance to V_{SS} (for each input)	C_I	–	10	pF

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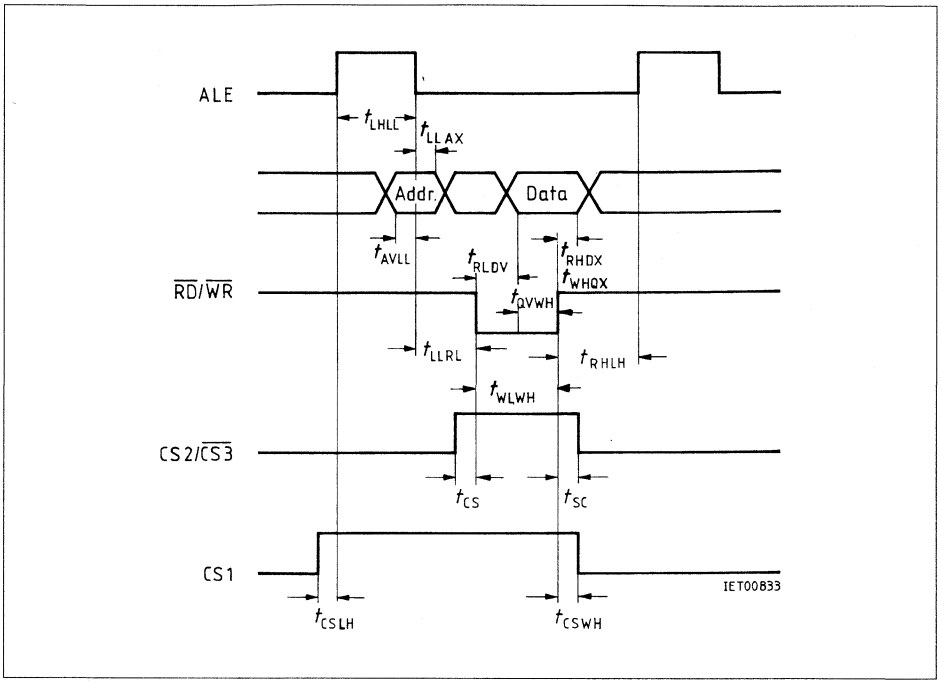
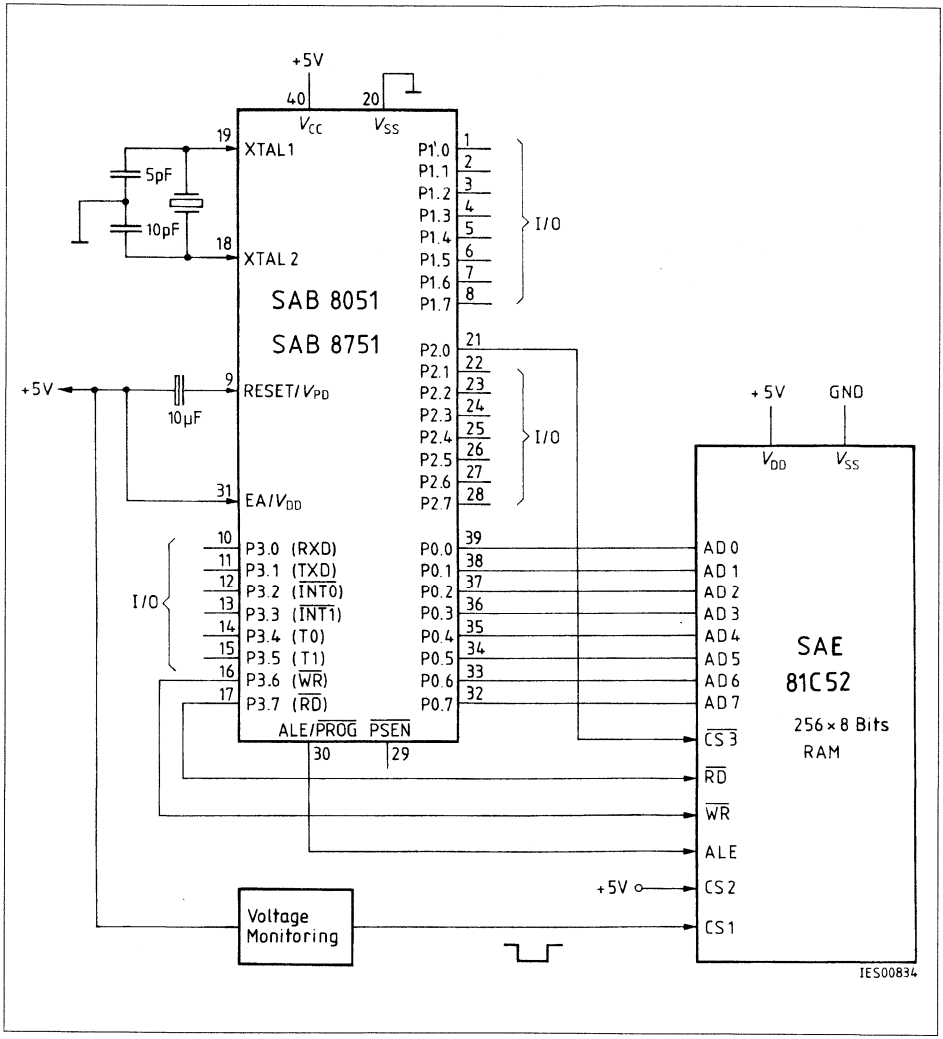


Timing Diagram



Application Circuit

SAE 81C52 with the µC SAB 8051

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SIEMENS

CMOS RAM

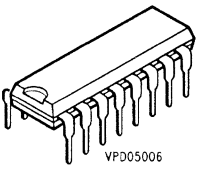
SAE 81C54

Preliminary Data

ACMOS IC

Features

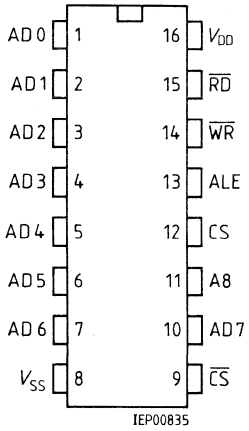
- 512 × 8 bit-organization
- Multiplexed address and data bus
- Tristate address and data lines
- On-chip address register
- Very low current consumption: 1 µA at 5.5 V during standby
- Dual chip selection
- Wide supply voltage range from 2.5 V to 5.5 V
- Fully compatible 5 V ±10 %
- Data retention up to 1.0 V
- Temperature range from – 40 to 110 °C



P-DIP-16

	Type	Ordering Code	Package
S	SAE 81C54 P	Q67100-H8486	P-DIP-16

The SAE 81C54 P is a static 4096-bit RAM (512 words by 8 bits) in Advanced CMOS technology. The address and data bus in the multiplex operation allows directly interfaces to 8-bit microprocessors/microcontroller families, e.g. SAB 8086, SAB 8088, SAB 8051. Due to its low power dissipation of less than 1 µA in standby mode this component requires only minimum supply current.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1-7, 10	AD 0-7	Address/data lines
8	V_{SS}	Ground
9	$\overline{CS}$	Chip select
11	A8	Address line
12	CS	Chip select
13	ALE	Address signal latch enable
14	$\overline{WR}$	Write enable
15	$\overline{RD}$	Read enable
16	V_{DD}	Supply voltage

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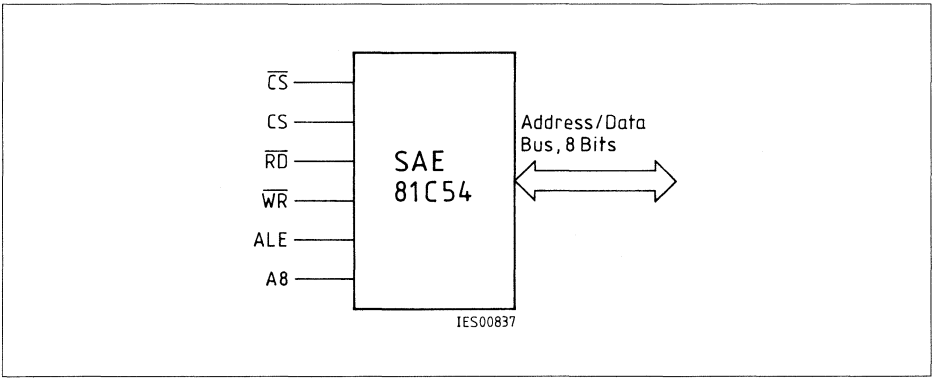
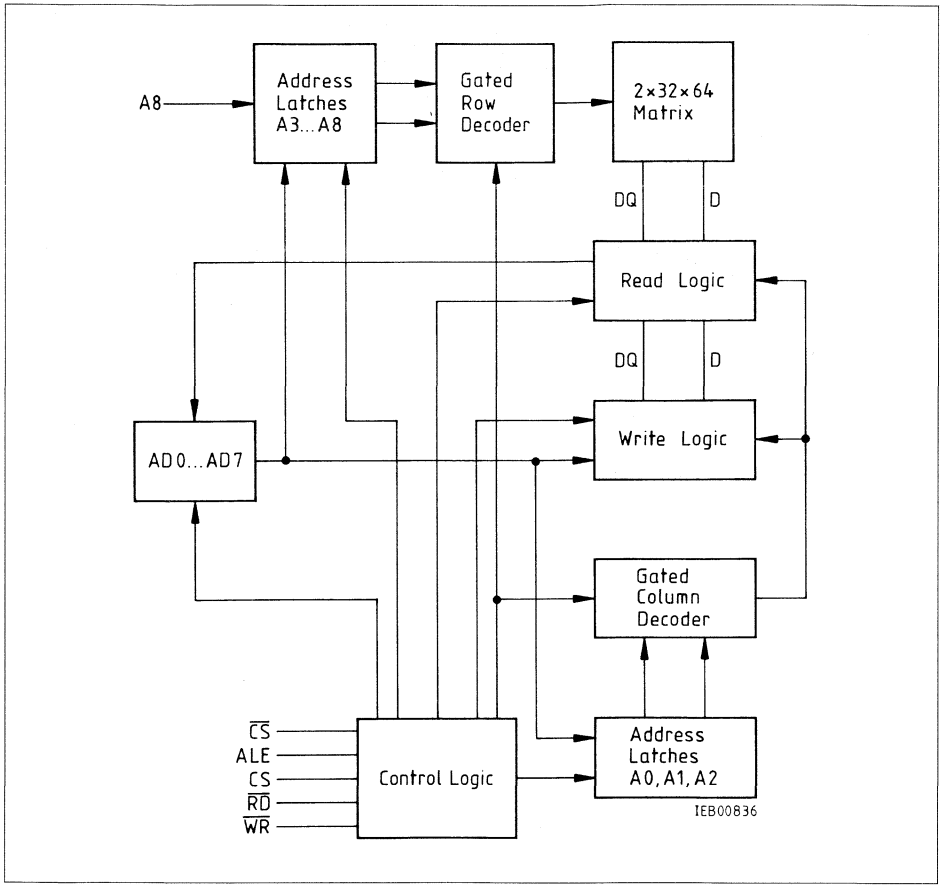
Truth Table for Control and Data Bus Pin Status

$\overline{CS}$	CS	$\overline{RD}$	$\overline{WR}$	AD 0-7 During Data Phase	Function
H	X	X	X	Floating	None
X	L	X	X	Floating	None
L	H	L	H	Data from memory	Read
L	H	H	L	Data to memory	Write



Logic Symbol



Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature	T_A	– 40 to 110	°C
Storage temperature range	T_{stg}	– 55 to 125	°C
Thermal resistance system - air	$R_{th\ SA}$	70	K/W

DC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Standby supply current	I_{DD}	–	–	1	µA	T_A = 25 °C
Operating supply current	I_{DD}	–	500	–	µA	100 kHz ALE
Operating supply voltage	V_{DD}	2.5	–	5.5	V	
Standby supply voltage	V_{DD}	1.0	–	5.5	V	Data retention
Input current	I_{IL}	–	–	1	µA	V_I = 0 – 5.5 V
Output leakage current	I_{QL}	–	–	1	µA	V_Q = 0 – 5.5 V floating
L-input voltage (V_{DD} < 4.5 V)	V_I	– 0.8	–	0.6	V	–
L-input voltage (V_{DD} > 4.5 V)	V_{IL}	– 0.8	–	0.8	V	–
H-input voltage	V_{IH}	0.6 × V_{DD}	–	V_{DD} + 0.8	V	–
H-input voltage	V_{IH}	–	–	V_{DD} + 0.8	V	V_{DD} = 5 V
L-output voltage (V_{DD} < 4.5 V)	V_{QL}	–	–	0.4	V	I_{QL} = 1 mA
L-output voltage (V_{DD} > 4.5 V)	V_{QL}	–	–	0.4	V	I_{QL} = 2 mA
H-output voltage (V_{DD} < 4.5 V)	V_{QH}	0.75 × V_{DD}	–	–	V	I_{QH} = 1 mA
H-output voltage (V_{DD} > 4.5 V)	V_{QH}	0.75 × V_{DD}	–	–	V	I_{QH} = 2 mA

AC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LL}	40	–	ns
Address setup before ALE	t_{AL}	25	–	ns
Address hold after ALE	t_{LA}	25	–	ns
$\overline{WR}$ pulse width	t_{CC}	60	–	ns
$\overline{RD}$ pulse width	t_{CW}	130	–	ns
Data setup before $\overline{WR}$	t_{DW}	70	–	ns
Data hold after $\overline{WR}$	t_{WD}	20	–	ns
Data hold after $\overline{RD}$	t_{DR}	–	30	ns
Access time $\overline{RD}$ to data output	t_{RD}	–	130	ns
Address floating to $\overline{RD}$	t_{AFC}	0	–	ns
CS before ALE	t_{CS}	30	–	ns
CS after $\overline{WR}$ or RD	t_{SC}	10	–	ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	35	–	ns
RD or $\overline{WR}$ to ALE = high	t_{CL}	25	–	ns

AC Characteristics

T_A = – 40 to 110 °C; V_{DD} = 2.5 to 5.5 V; V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{LL}	60	–	ns
Address setup before ALE	t_{AL}	40	–	ns
Address hold after ALE	t_{LA}	60	–	ns
$\overline{WR}$ pulse width	t_{CC}	200	–	ns
$\overline{RD}$ pulse width	t_{CW}	350	–	ns
Data setup before $\overline{WR}$	t_{DW}	200	–	ns
Data hold after $\overline{WR}$	t_{WD}	60	–	ns
Data hold after $\overline{RD}$	t_{DR}	–	95	ns
Access time $\overline{RD}$ to data output	t_{RD}	–	350	ns
Address floating to $\overline{RD}$	t_{AFC}	0	–	ns
CS before ALE	t_{CS}	80	–	ns
CS after $\overline{WR}$ or $\overline{RD}$	t_{SC}	30	–	ns
ALE to $\overline{RD}$ or $\overline{WR}$	t_{LC}	60	–	ns
RD or $\overline{WR}$ to $\overline{ALE}$ = high	t_{CL}	30	–	ns

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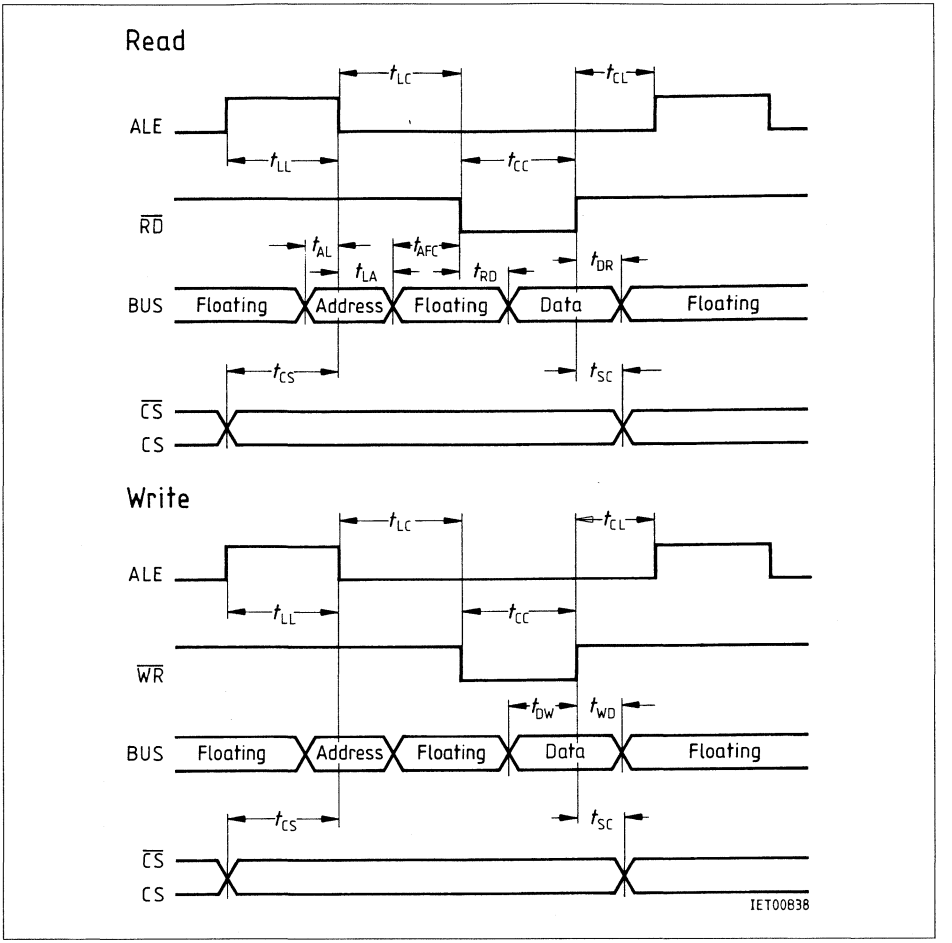

Read
ALE
RD
BUS
Floating
Address
Floating
Data
Floating
CS
CS
Write
ALE
WR
BUS
Floating
Address
Floating
Data
Floating
CS
CS
IET00838

Diagrams

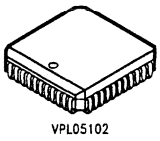
CMOS Dual-Port RAM

SAE 81C80 A

CMOS IC

Features

- Processor interface with address and data bus plus signals $\overline{ALE}$, $\overline{WR}$, RD
- 8051-, 8096-compatible timing
- Memory capacity 504 bytes
- All functions fully static (excl. oscillator watchdog)
- Standby operation
- On-chip oscillator with separate clock output
- Eight scheduling registers
- Three loadable timers for processor monitoring or applicable as longterm timers
- Monitoring of internal oscillator (hardware watchdog)
- Three outputs for interrupt triggering (can be set on the bus)
- Fully asynchronous operation of two processors possible
- Data retention down to 1 V
- PL-CC-44 (SMD) package
- Extended temperature range from – 40 through 110 °C
- CMOS technology



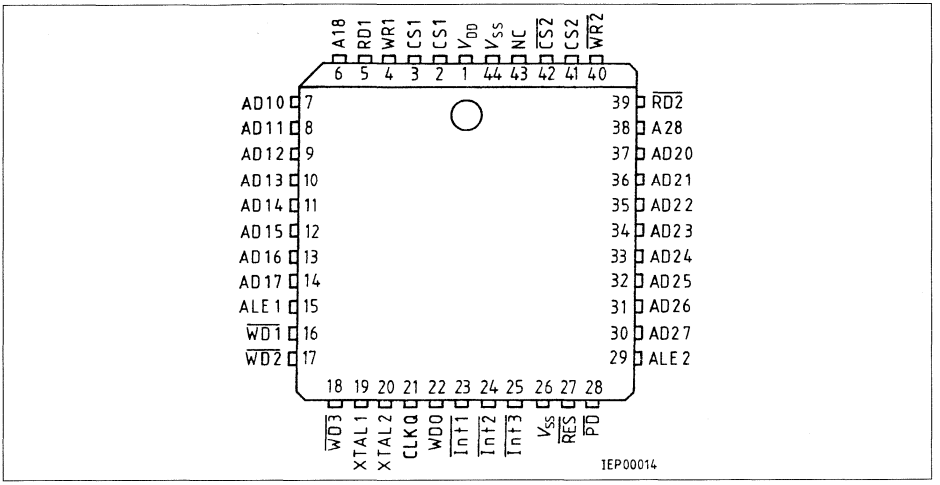
P-LCC-44

Type	Ordering Code	Package
S SAE 81C80 A	Q67100-H8706	P-LCC-44 (SMD)

The SAE 81C80 A dual-port RAM (DPR) is a CMOS memory IC with a capacity of 504 bytes (**figure 1**).

A very notable feature of this DPR is that it can be used by two microcontrollers (MCs) simultaneously and fully asynchronously. Each microcontroller uses the DPR like a normal static RAM. Thus, when comparing the circuit development of this DPR with that of standard memory, no extra effort is required. Access collisions are excluded, which is the pre-requisite for fast communication between the two MCs.

The SAE 81C80 A DPR is ideally suited for multi-processor/multi-controller applications like master/slave configurations or controls where one controller acquires measured data and a second one controls the actuators (e.g. in motors, etc.). (See **figures 2 and 3**).



Pin Configuration
(top view)

Pin Definitions and Function

Pin	Symbol	Function
7 8 9 10 11 12 13 14	AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17	Data and address bus port 1
06	A18	Address 8 port 1
37 36 35 34 33 32 31 30	AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27	Data and address bus port 2
38	A28	Address 8 port 2
15 29	ALE1 ALE2	Address latch enable port 1 Address latch enable port 2 These signals are for separating data and addresses on the bus. The address is stored on the falling edge of the signal.

Pin Definitions and Function (cont'd)

Pin	Symbol	Function
5 39	$\overline{RD1}$ $\overline{RD2}$	Read signal port 1 (active low) Read signal port 2 (active low)
4 40	$\overline{WR1}$ $\overline{WR2}$	Write signal port 1 (active low) Write signal port 2 (active low)
3 2	CS1 $\overline{CS1}$	Chip select port 1 Chip select port 1 (active low)
41 42	CS2 $\overline{CS2}$	Chip select port 2 Chip select port 2 (active low) The chip-select inputs select a port when the two associated inputs are on active level.
27	$\overline{RES}$	Reset input Resets the IC to a defined initial state when $\overline{RES}$ is low. At the same time the outputs $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$ are switched low for the duration of the reset pulse. The oscillator continues to operate.
28	$\overline{PD}$	Power-down Disables all other inputs and the oscillator when $\overline{PD}$ is low.
44 1	V_{SS} V_{DD}	Negative supply voltage Positive supply voltage
43	NC	Not connected
19	XTAL1	Pin for crystal (must remain open for external clock supply).
20	XTAL2	Pin for crystal or applying external clock
21	CLKQ	Clock output
22	$\overline{WDO}$	Oscillator watchdog (open-drain output) High indicates that the oscillator is working.
16 17 18	$\overline{WD1}$ $\overline{WD2}$ $\overline{WD3}$	Open-drain outputs of three timers
26	V_{SS}	No function (must be connected)
23 24 25	$\overline{Int1}$ $\overline{Int2}$ $\overline{Int3}$	Open-drain outputs Outputs that can be controlled via the port for triggering an interrupt on a processor for example.

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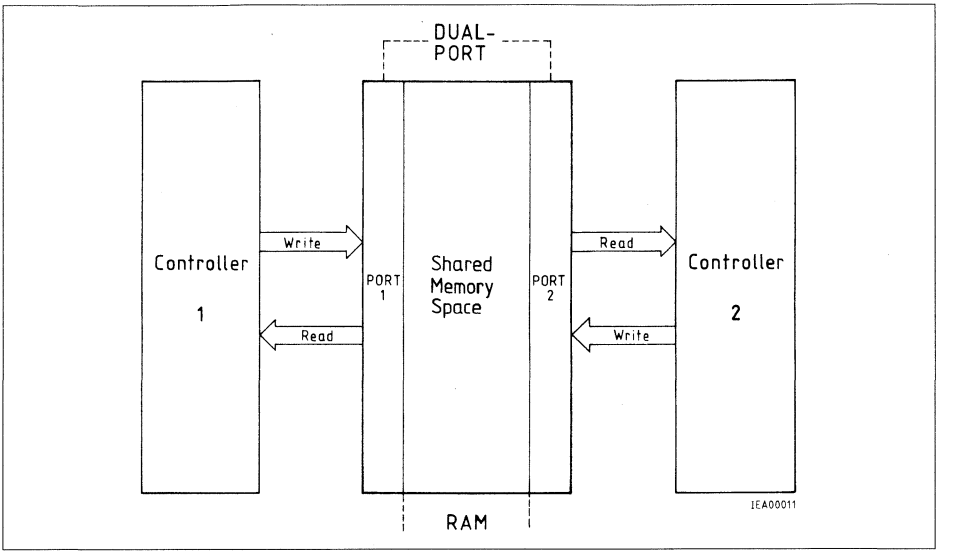

Figure 1
Principle of the Dual-Port RAM (DPR)

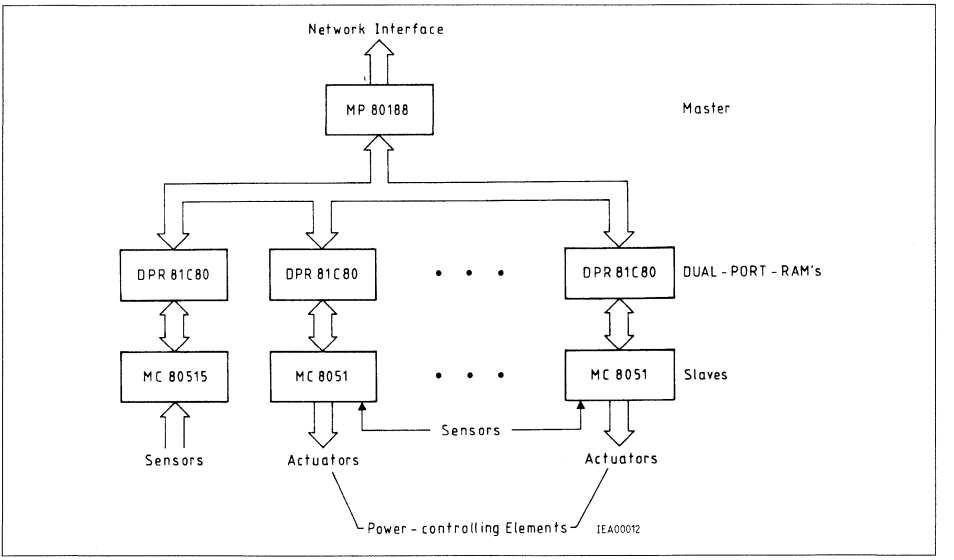

Figure 2
Interfacing Master and Slave Processors by DPRs

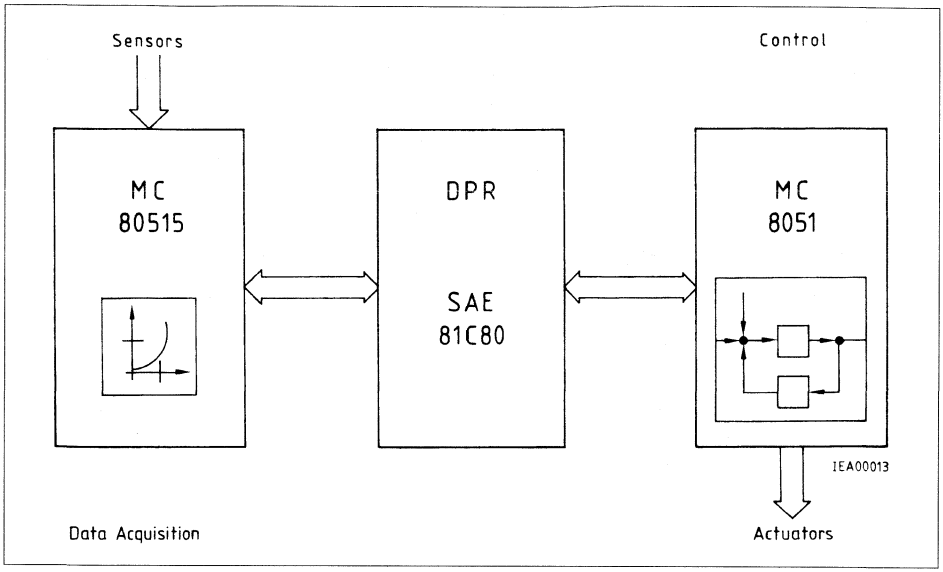

Figure 3
Dual-Port RAM used between Measured-Data Acquisition and the Actuators

Functional Description

Dual-Port RAM

The SAE 81C80A is a 504-byte static RAM simultaneously accessible by two microcontrollers. The memory locations are selected via a mutliplexed address/data bus and two chip-select inputs. The direction of data transfer is determined by the $\overline{RD}$ and $\overline{WR}$ inputs.

There will be no undefined states when a memory location is concurrently accessed by two processors, even if they write simultaneously to the same memory location. Depending on the internal state of the access control and the actual physical sequence, the value of one of the two ports will be stored. Also, if one memory location is read and written to at the same time, the data will not be mixed, i.e. either the original data or the new data are read out.

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Chip-Select Inputs

The chip-select inputs affect signals $\overline{WR}$ and $\overline{RD}$, but not the ALE input. Therefore, the ALE signal on the DPR (even if the DPR is not selected) must correspond to the specified values. To eliminate selection, it is sufficient if one of the two chip-select inputs becomes inactive when the falling edge of $\overline{WR}$ or $\overline{RD}$ appears.

Reset

The reset is necessary for setting the control units of the DPR to a defined initial state. It initializes the timer-mode registers with the values 0000XXX0B (timers 1 and 2) and 00000XX0B (timer 3). The $\overline{INT}$ outputs are set to 0.
The reset input is a TTL input without Schmitt-trigger response. For this reason, neither an ALE nor a $\overline{WR}$ signal must be applied to the DPR if the voltage on the reset input is below V_{IH}. The length of the Reset pulse must be greater than six clock (oscillator) cycles and the clock must be active.
When the reset input is low, outputs $\overline{WD1}$, $\overline{WD2}$ and $\overline{WD3}$ are set to low. After a reset these outputs are high. The scheduling registers are set to state 1 by reset.
A reset is also necessary if the DPR is reactivated from power-down, while the contents of the RAM and oscillator remain unaffected.

Power-Down Mode

When the power-down mode ($\overline{PD}$) is activated, all inputs (except $\overline{PD}$ and XTAL1, XTAL2) plus the oscillator are disabled. This means that any levels are possible on the remaining inputs.
An active level on $\overline{PD}$ also produces an internal reset. Nevertheless, to ensure proper operation after deactivation of the power-down mode, an external reset should be made to bridge the time required by the oscillator for buildup. The outputs of the ports go high-impedance, while outputs CLKO, $\overline{WDO}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{INT1}$, $\overline{INT2}$ and $\overline{INT3}$ are set to low. The $\overline{PD}$ input shows a Schmitt-trigger response. This allows V_{DD} to be evaluated directly, for example (**see application circuit**).

Interrupt Outputs

The DPR has three interrupt outputs that can be set and reset directly by writing to an address (**see table 1**). The outputs are located in the same address range as the scheduling registers. However, only bits 2 and 3 are relevant for the interrupt outputs. At least one of bits 0 and 1 should be other than 1 to prevent the scheduling registers from being affected. The functions of the outputs are shown in the following table:

RES	Bit 3	Bit 2	Output
1	0	0	no change
1	0	1	1
1	1	0	0
1	1	1	undefined
0	–	–	0

Oscillator Watchdog

This part of the circuit is a fail-save mechanism for the oscillator. If the frequency of the clock is missing, the output switches to $\overline{WDO}$ low. The circuit works like an analog integrator. Below approx. 100 kHz, low pulses are produced on the output. The pulse width depends on the clock frequency. This part of the circuit should not be used at operating frequencies of less than 500 kHz.

Supply Voltage

To prevent any interference, the supply voltage of the DPR should be blocked as close as possible to the pins with a capacitor of approx. 100 nF (**see application circuit**).

Timers

The three timers are 24-bit counters with a clock frequency of $f_{OSC}/6$. Each of the counters can be set by writing to three specific RAM addresses. The value is then simultaneously stored in the RAM and a buffer register of the timer. When the low byte is written, all three bytes are parallely stored in the reload register. The value in the reload register is kept in all operating modes until the associated low byte is written again.

The counters are down-counters. They can be started by setting bit 7 in the associated timer-mode register (TMR). Each counter can be configured by a TMR. The bits of the TMRs have the following function:

Bit 0: This bit provides overwrite protection for the reload register.

Use: After writing to the reload registers and starting of the timer – by writing to the associated protection bit – the adjacent RAM area can be used without affecting the reload register (reset state = 0).

Bit 4: It serves for switching the polarity of the output signal (reset state = 0).

Bit 4 = 0; idle state 1, active 0
Bit 4 = 1; idle state 0, active 1

Bit 5: This bit switches the operating mode (reset state = 0).

Bit 5 = 0 single-shot, i.e. when the counter is started, the output signal becomes active. After reaching zero, the output signal is reset. The timer has to be restarted to trigger another count cycle. The values from the reload register are then loaded into the counter.

Bit 5 = 1 auto reload, i.e. when the counter is started, the value of the reload register is loaded into it. When zero is reached, the counter issues a pulse ($\approx 4\,\mu s$ at 12 MHz), automatically reloads the original value and the entire operation starts again. In this way a frequency can be set with a resolution of 24 bits. Because of the pulse width of eight timer clock pulses, however, the shortest period is limited to nine timer clock pulses ($t_{OSX} \times 6$). If a new start pulse appears in the count cycle (even without "STOP"), no pulse is issued and the counter is reloaded.

Bit 6: In the reload mode the timer can be halted by setting this bit and resetting bit 5. (In a new start the contents of the counter are lost and that of the reload registers remain unaffected).

Bit 7: Setting this bit starts the counter.

Only for the registers of timers 1 and 2

Bit 1-3: These are used together with bit 0 for switching the watchdog mode ON and OFF.

Only for the register of timer 3

Bit 1-2: Reserved (should always be 0 for correct operation).

Bit 3: Switches **all three timers** to test mode, i.e. only the upper twelve bits are used to generate the output signal (reset state = 0).

Watchdog Mode

For timers 1 and 2a special mode was implemented which can be used to monitor the two processors. In this mode there is a control register (CR) for each timer (**see table 1** for addresses). The watchdog mode is set by loading the TMR with the value 101X1111B, the polarity of the output signal being freely selectable with bit 4. This mode works similarly to the auto-reload mode, but neither the reload register nor the TMR can be altered.

In the watchdog mode, the timer can only be restarted (and the output pulse suppressed) if the values 055H and 0AAH are successively written into the control register. The time between these two write operations is random, but the sequence must be completed before the timer has run down, i.e. the output pulse is generated. No value may be written into either the TMR or CR between the two write operations, otherwise the sequence has to be started again.

To reset the timer to the normal mode, first the value 055H has to be written into the CR, then the value 010X0000B into the TMR, and finally the value 0AAH into the CR. Here, too, if any other value is written into either of the two registers during the sequence, the entire operation has to be started again. The time between the accesses is random.

The timer operation in watchdog mode is illustrated in the appendix in an 8051 example program.

Note: The relevant bits for changing the timer state to watchdog mode are bit 0 - bit 3; the shown pattern is the only one, which makes sense for this mode.

Figure 4
Bit Assignment of Timer-Mode Registers for Timer 1 and 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (=1)	Timer stop (=1) for auto-reload	Mode (auto-reload= 1, single-shot = 0)	Polarity of output pulse (High = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Protection (=1) against overwriting of reload register

Figure 5
Bit Assignment of Timer-Mode Register for Timer 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (=1)	Timer stop (=1) for auto-reload	Mode (auto-reload =1, single-shot = 0)	Polarity of output pulse (High = 0)	Test (=1) switches timer to test mode	Reserved (normal mode = 0)	Reserved (normal mode = 0)	Protection (=1) against overwriting of reload register

Access Collisions

With a RAM which can be written to or read simultaneously by two controllers, different kinds of access collision are possible:

1. Simultaneous read access to the same memory location from both ports;
2. One port reads the same memory location which the other port writes to concurrently
3. Concurrent write access to the same memory location from both ports;
4. Read access to a logically linked data block by one port, while the other port modifies the same data block.

The SAE 81C80A dual-port RAM avoids the first three types of access collision by hardware. The fourth problem can be solved by user software.

The standard solution for the access collisions described above would be as follows: **before** accessing the memory area, an additional memory location must be established by setting an access flag (semaphore). This would necessitate three memory operations:

- First access: read the flag and check whether the data area is free.
- Second access: write the flag with the data for reservation.
- Third access: read the flag and make sure that your own reservation has not been overwritten by the other port.

Only after this sequence would a microcontroller be priviledged for access and could write or read to the data area without the risk of contention.

With the SAE 81C80A dual-port RAM this access routine is simplified using scheduling registers.

Scheduling Registers

Note: The assignment of a memory area to a scheduling register is defined by the user software of both controllers

With the scheduling registers synchronization can be done with only one access because the reservation is performed during reading. The other port cannot overwrite it.

This means that a scheduling register is **written by reading,** unless it was occupied.

The description above shows that these registers are no ordinary RAM locations. They are formed by a finite state machine (FSM), which can assume the following four states **(see figure 6):**

- State 1: port 1 was the previous owner and the register is free.
- State 2: port 1 occupies the register.
- State 3: port 2 was the previous owner and the register is free.
- State 4: port 2 occupies the register.

The state of a register can be read out from the particular address, but causes also a change in the state of the FSM (arrows in **figure 6**). Reading produces 2-bit information:

- Bit 0 is the owner bit. It is set when the reading port is or was the owner of a register.
- Bit 1 is the occupied bit. It is set when a register has been reserved by a port.
- Bit 2 through 7 are always 0.

Reserving is done by reading a register and enabling by writing to it XXXXXX11 B (pay attention to the interrupt outputs of bits 2 and 3!). Thus a correct protocol using the scheduling registers takes the following form:

1. Read the scheduling register.
2. Check whether the occupied bit is set and the owner bit is not set (i.e. the other port has reserved). If so, go back to 1, otherwise continue.
3. Process the data area.
4. Enable the scheduling register by writing 03 H to the address of the register
5. End

In cases where accessing of a data area requires prior reading of or writing to this data area by the second processor, a separate evaluation of the occupied bit and owner bit can be done in step 2:

2a. Owner bit self? If so, continue to 2c, otherwise to 2b.
2b. Occupied bit self? If so, continue to 2c, otherwise to 3.
2c. Enable the scheduling register by writing 03 H to the address of the register (continue with 1).

The following applies only to the scheduling registers:

Usually, in the case of a concurrent access by both processors, writing has priority over reading. However, a simultaneous read or write access from the two ports means that port 1 has priority over port 2.

The addresses of the scheduling registers are listed in **table 1**.

The assignment of scheduling registers to specific data areas is made by the user. The software (of both controllers) should be configured so that, prior to accessing a logically related data area, the associated scheduling register is accessed first (according to the above sequence).

So the assignment of the various dual-port RAM address spaces to scheduling registers will depend solely on the structure of the user software.

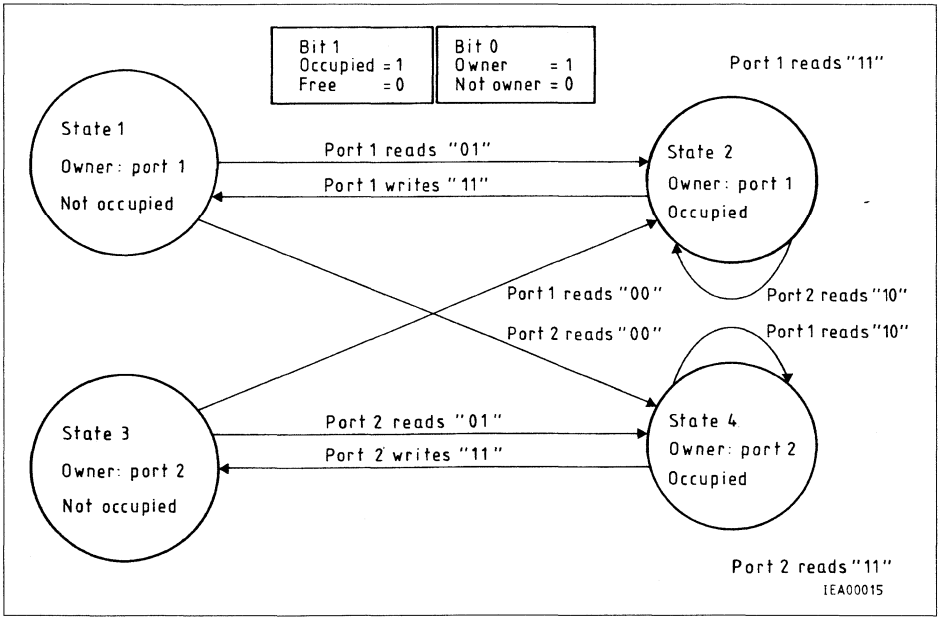

Figure 6
Diagram Showing the Various States of the Scheduling Registers
Only the two least significant bits of the data are shown (in converted commas).

Notes:

1) The owner bit indicates the last owner of a register
2) Only if the port is owner of the register will writing change the state.
3) The reset state is state 1.
4) The FSM is symmetrical. Therefore, the two processors can use the same program.

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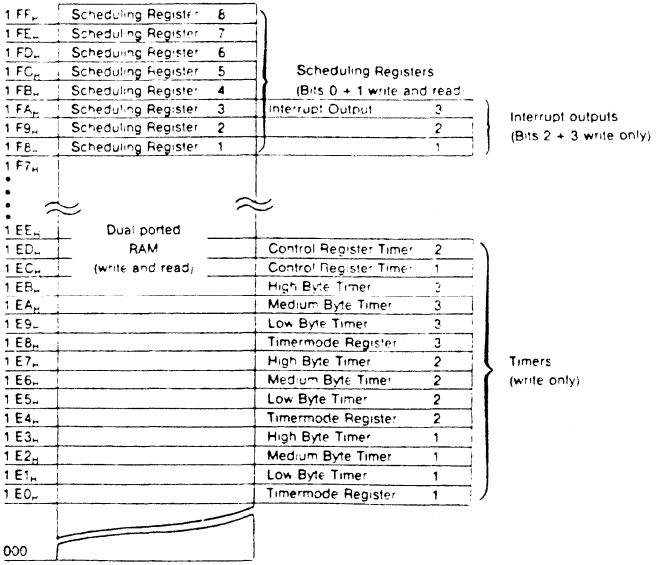
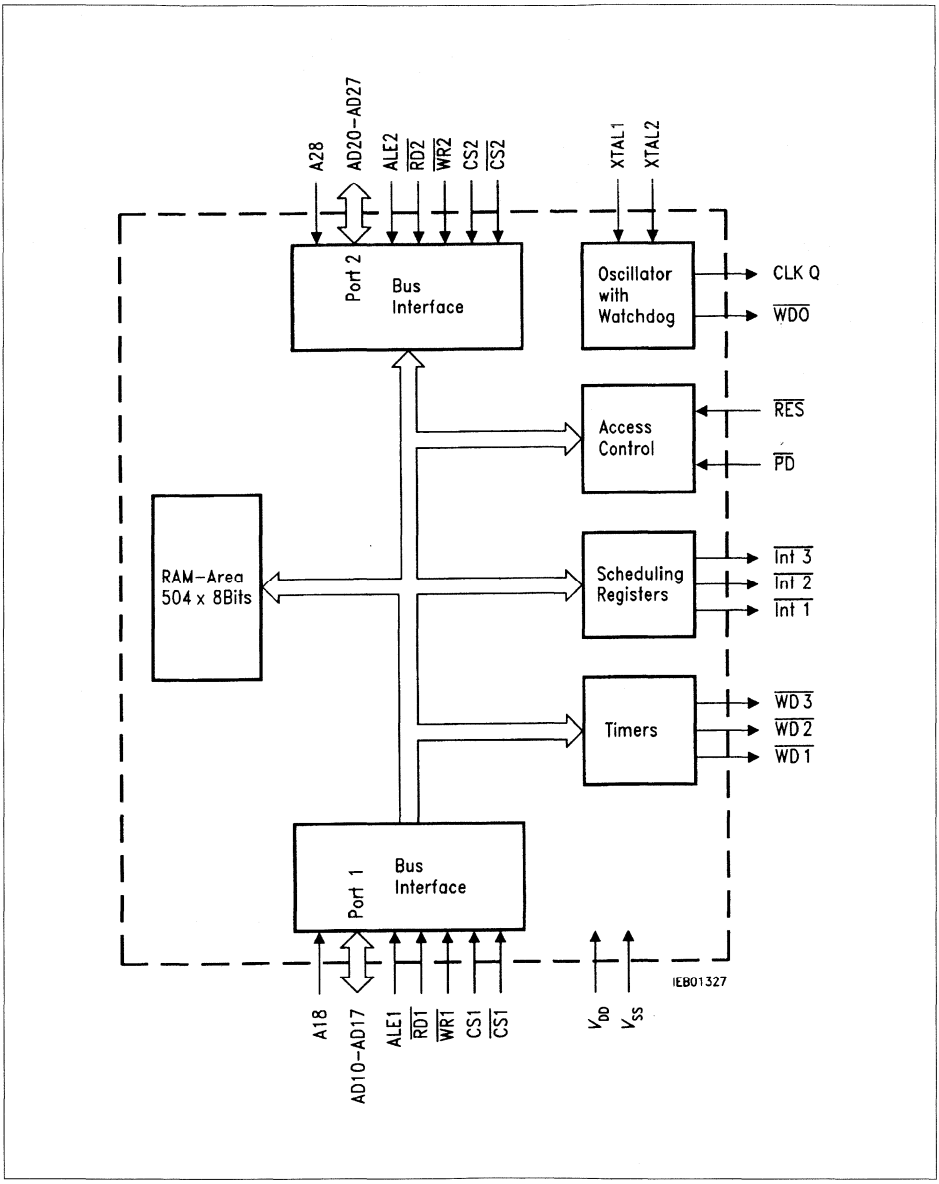
Table 1
Address Assignment of DPR Registers

Register	Address	Register	Address
Scheduling register 1	1F8H	High-byte timer 2	1E7H
Scheduling register 2	1F9H	Medium-byte timer 2	1E6H
Scheduling register 3	1FAA	Low-byte timer 2	1E5H
Scheduling register 4	1FBH		
Scheduling register 5	1FCH	High-byte timer 3	1EBH
Scheduling register 6	1FDH	Medium-byte timer 3	1EAH
Scheduling register 7	1FEH	Low-byte timer 3	1E9H
Scheduling register 8	1FFH		
Timer-mode register 1	1E0H	Control-register timer 1	1ECH
Timer-mode register 2	1E4H	Control-register timer 2	1EDH
Timer-mode register 3	1E8H		
High-byte timer 1	1E3H	Interrupt output 1	1F8H
Medium-byte timer 1	1E2H	Interrupt output 2	1F9H
Low-byte timer 1	1E1H	Interrupt output 3	1FAA

Figure 7
Memory Map





Block Diagram

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Absolute Maximum Ratings

T_A = – 40 to 110 °C; all voltages referred to V_{SS}

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Storage temperature	T_{stg}	– 50	–	125	°C
Total power dissipation	P_{tot}	–	–	500	mW
Power dissipation per output	P_Q	–	–	50	mW
Input voltage	V_I	– 0.5	–	V_{DD} + 0.5	V
Supply voltage	V_{DD}	– 0.5	–	6	V
Operating Range					
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (w/o loading of outputs)	I_{DD}	–	–	20	mA
Operating frequency	f_s	–	–	12	MHz
Ambient temperature *)	T_A	– 40	–	110	°C
Standby current	I_{DD}	–	–	1	µA
Data-retention voltage	V_{DH}	1	–	–	V

DC Characteristics

T_A = 25 °C; all voltages referred to V_{SS}

Parameter	Symbol	Limit Values			Test Condition
		min.	max.	Unit	
All Input Signals Except XTAL2 and $\overline{PD}$					
H-input voltage	V_{IH}	2.2	V_{DD}	V	–
L-input voltage	V_{IL}	0	0.8	V	–
Input capacitance	C_I	–	10	pF	–
Input current	I_I	–	1	µA	–
XTAL2 (as external clock input)					
H-input voltage	V_{IH}	3.5	V_{DD}	V	–
L-input voltage	V_{IL}	0	0.5	V	–
Input capacitance	C_I	–	10	pF	–
$\overline{PD}$ (Schmitt-trigger characteristics)					
H-input voltage	V_{IH}	V_{DD} – 1	V_{DD}	V	–
L-input voltage	V_{IL}	0	1.0	V	–
Input capacitance	C_I	–	10	pF	–
Output Signals AD10-17, AD20-27					
H-output voltage	V_{QH}	2.4	V_{DD}	V	I_Q = 0.5 mA
L-output voltage	V_{QL}	–	0.4	V	I_Q = 1.6 mA

DC Characteristics (cont'd)
T_A = 25 °C; all voltages referred to V_{SS}

Parameter	Symbol	Limit Values			Test Condition
		min.	max.	Unit	
Output Signals $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{WD0}$ (open drain, weak pull-up)					
L-output voltage	V_{QL}	–	0.4	V	I_Q = 1.6 mA
Output Signal Clock-Out					
H-output voltage	V_{QH}	2.4	–	V	I_Q = 0.5 mA
L-output voltage	V_{QL}	–	0.4	V	I_Q = 1.6 mA
Load capacitance	C_L	–	80	pF	–

AC Characteristics
The AC characteristics apply throughout the operating range T_A = 25 °C.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Read cycle time	t_{CYR}	300 + t_{LHLL}	–	ns
Write cycle time	t_{CYW}	440 + t_{LHLL}	–	ns
ALE pulse width	t_{LHLL}	40	–	ns
Address setup to ALE low	t_{AVLL}	30	–	ns
Address hold after ALE low	t_{LLAX}	40	–	ns
$\overline{RD}$ pulse width	t_{RLRH}	120	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	ns
ALE low to $\overline{RD}$ or $\overline{WR}$ active	t_{LLWL}	30	–	ns
Data hold after $\overline{RD}$ high	t_{RHDX}	0	30	ns
ALE low to valid data out	t_{LLDV}	–	290	ns
$\overline{RD}$ low to data valid (only scheduling registers)	t_{RLDV}	–	2 t_{OSC} + 20	ns
Valid data in after $\overline{WR}$ low	t_{DVWL}	–	30	ns
$\overline{WR}$ low to ALE high	t_{WLLH}	150	–	ns
Data setup before $\overline{WR}$ high	t_{QVWH}	30	–	ns
Data hold after $\overline{WR}$ high	t_{WHQX}	30	–	ns
Delay $\overline{RD}$ low to both chip select active	t_{RLCH}	–	20	ns
Delay $\overline{WR}$ low to both chip select active	t_{WLCH}	–	20	ns

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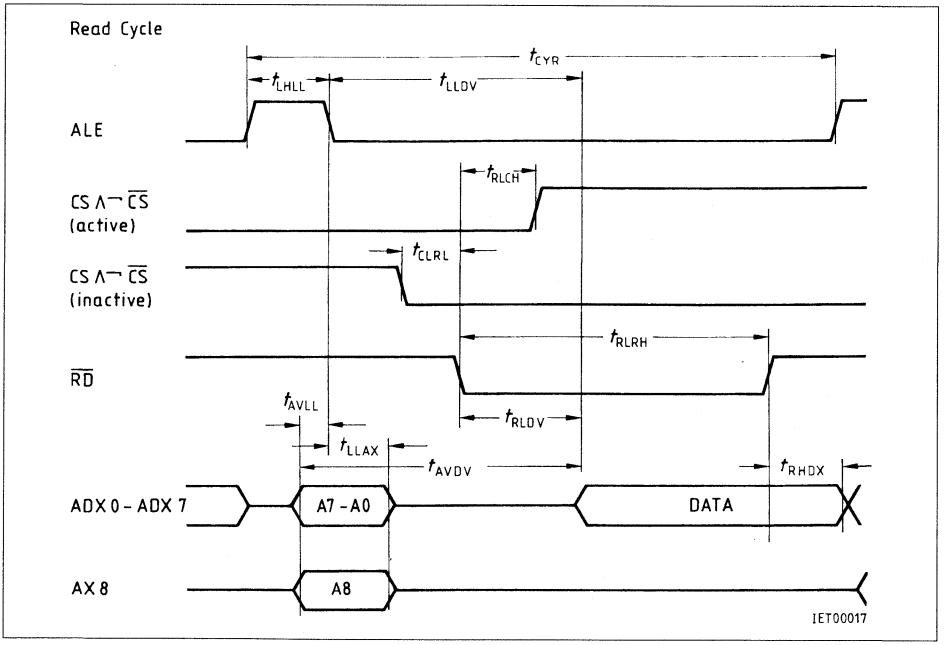
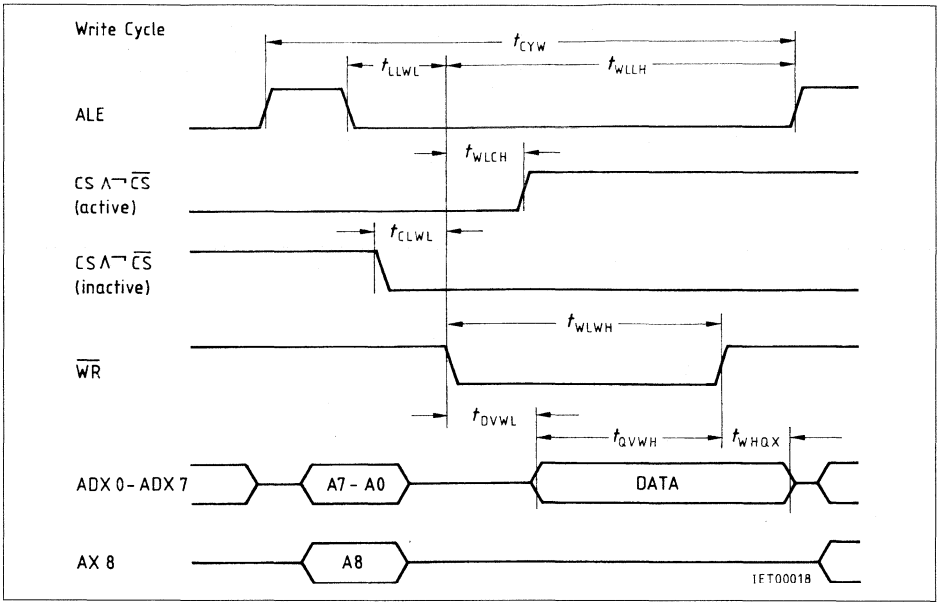
AC Characteristics (cont'd)
The AC characteristics apply throughout the operating range T_A = 25 °C.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Set-up of chip select to $\overline{RD}$*)	t_{CLRL}	0	–	ns
Set-up of chip select to $\overline{WR}$*)	t_{CLWL}	0	–	ns
Active pulse length of timer outputs	t_{ACT}	48 t_{OSC}	48 t_{OSC}	ns
Oscillator period	t_{OSC}	83	–	ns
High time	t_{OSCH}	35	–	ns
Low time	t_{OSCL}	35	–	ns

*) For deselection



Pulse Diagram 1



Pulse Diagram 2

Note to Chip Select Timing:
The shown timing is not necessary, if the device is always activated or deactivated. This means either of CS or $\overline{CS}$ or both may be constant "high" or "low".

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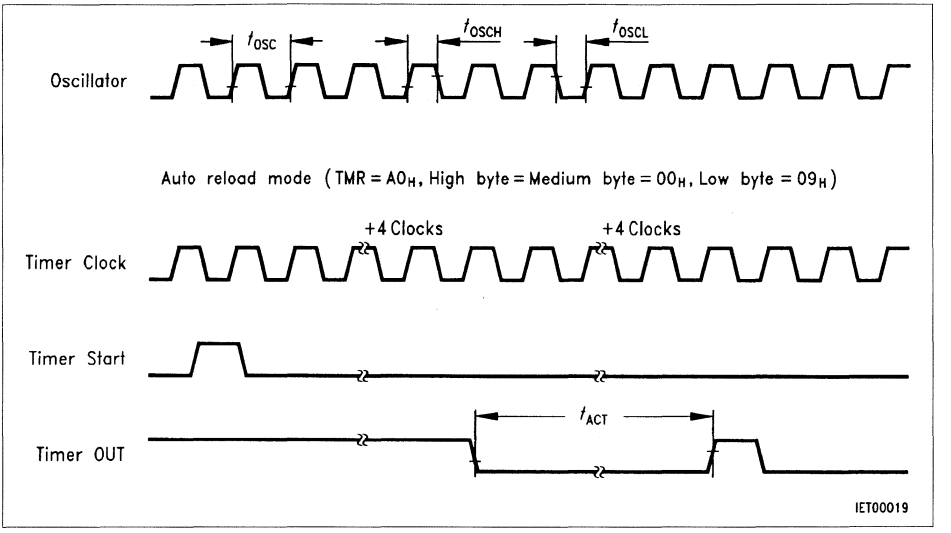
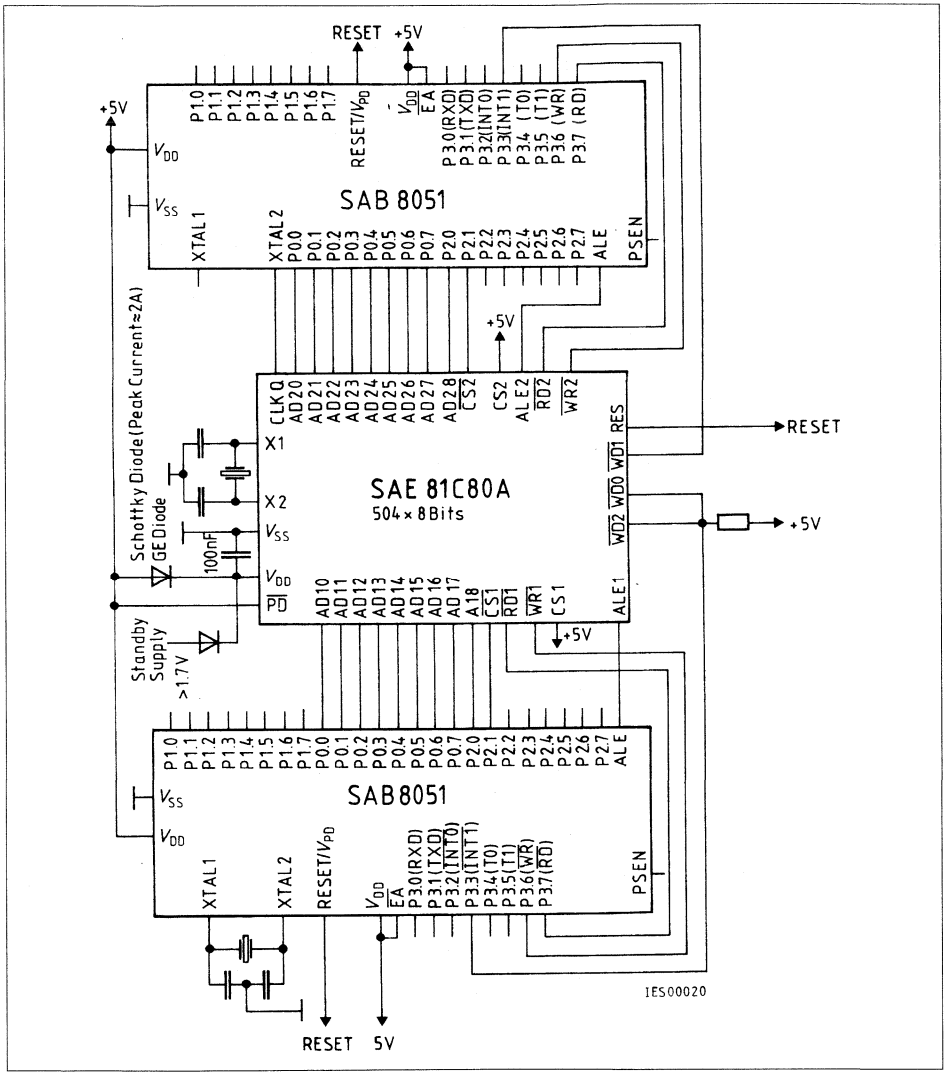


Pulse Diagram 3



Example of an Application Circuit[1)]

1) Design proposal (non-obligatory)

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Appendix

8051 Program for Timer Operation in Watchdog Mode

```
HBYTE   EQU   1E3H    ; Address high byte reload register
TMR     EQU   1E0H    ; Address timer-mode register
CR      EQU   1ECH    ; Address control register
REST1   EQU   055H    ; 1st value to restart timer
REST2   EQU   0AAH    ; 2nd value to restart timer
WDOFF   EQU   040H    ; Value to switch off watchdog mode

; Load reload register

MOV     DPTR, #HBYTE
CLR     A
MOVX    @ DPTR,A
DEC     DPL
MOV     A, #0FFH
MOVX    @ DPTR,A
DEC     DPL
MOVX    @ DPTR,A

; Set watchdog mode and start timer

MOV     A, #0AFH
DEC     DPL
MOVX    @ DPTR,A

; Reset timer

MOV     DPTR, #KR
MOV     A, #REST1
MOVX    @ DPTR,A
MOV     A, #REST2
MOVX    @ DPTR,A

; Switch off watchdog mode and halt timer

MOV     DPTR, #KR
MOV     A, #REST1
MOVX    @ DPTR,A
MOV     A, #WDOFF
MOV     DPTR, #TMR
MOVX    @ DPTR,A
MOV     A, #REST2
MOV     DPTR, #KR
MOVX    @ DPTR,A

;

END
```

Nonvolatile Memory 1-Kbit E²PROM

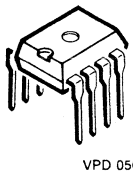
SDE 2506 A2

Preliminary Data

MOS IC

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 × 8-bit organization
- 5 V supply voltage
- 3 lines processor interface for data transfer and chip control
- Data input (8 bits), address input (7 bits), control information input (1 bit) and data output are serial
- More than 10^5 reprogramming cycles per address
- Data retention longer than 10 years (operating temperature range)
- Unlimited number of read-out operations without refresh
- 5 ms erase/write cycle
- Extended temperature range from – 40 to 110 °C



VPD 05025

P-DIP-8

Type	Ordering Code	Package
SDE 2506 A2	Q67100-H9018	P-DIP-8

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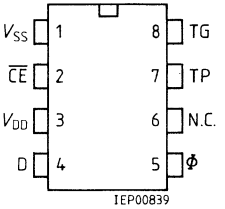
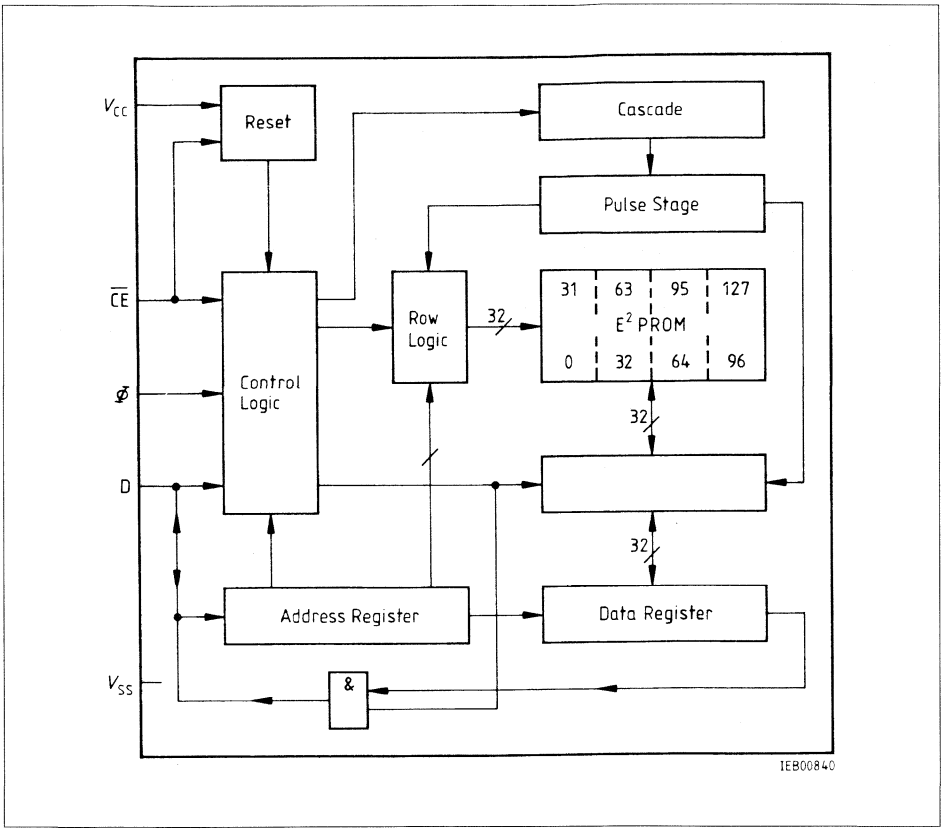


Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE}$ = 1 for data input/output, $\overline{CE}$ = 0 for reprogramming
3	V_{DD}	+ 5 V supply voltage
4	D	Data input/output bidirectional data line For reprogramming D = 1 erase, D = 0 write
5	Φ	Clock
6	N.C.	Not connected
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open



Block Diagram

Circuit Description

Data Transfer and Chip Control

Three lines having several functions each are required for data transfer between control processor and E²PROM memory.

a) Data line D
- bidirectional serial data transfer
- serial address input
- clocked input of a control information
- direct control input

b) Clock line Φ
- data input, address input and control bit input
- data output
- start read-out with takeover of data from memory in shift register or start data-change during reprogramming

c) Chip enable line $\overline{EC}$
- chip reset and data input (active high)
- chip enable (active low)

Prior to activating the chip, the data, address and control information is clocked in via the bidirectional data bus. These data are maintained in the shift register during reprogramming and read-out up to the second clock pulse. The following data formats have to be input:

a) Memory read-out: one 8-bit control word, consisting of
- 7 address bits A0 to A6 (at first A0 being LSB)
- 1 control bit, SB = "0", after A6

b) Memory reprogramming (erasure and/or writing) 16-bit input information, consisting of
- 8 bits D0 to D7 new memory information (at first D0 being LSB)
- 7 bits A0 to A6 address information (at first A0 being LSB after D7)
- 1 bit control information, SB = "1", after A6

Memory Read-Out

After data input and with SB = "0" the read-out operation of the selected word address is started by the transition of $\overline{CE}$ from "1" to "0". The information being on the data line during chip enable is of no influence.

With the first clock pulse after $\overline{CE}$ = "0" the data word is taken over from the selected memory address into the shift register. After termination of the first Φ pulse the data output is in the low impedance state. With every following clock pulse another data bit is pushed to the output. Through the transition of $\overline{CE}$ from "0" to "1" the data line returns to the high impedance state.

Reprogramming

In general, a full reprogramming operation consists of an erasure operation and a subsequent writing operation. During erase all bits of the selected word are set into the uniform "1" state, during writing "0" states are produced according to the information in the shift register.

A reprogramming operation is started when after data input and due to chip activation an information SB = "1" is in the relevant cell. Whether an erase or a writing operation is then taking place depends on the information that is on data line D during chip enable.

For erasure in state "1", a "1" must be present at the data input during transition of $\overline{CE}$ to low. If, however, a writing process is to be started in state "0", a "0" has to be present at the data line during chip enable.

Afterwards, a start pulse at the clock input Φ is required for the programming start. The control information has to remain stable at D until the leading edge of the start pulse is reached. The active data change starts with the trailing edge of this start pulse. The programming process is terminated by suppression of the chip enable, i.e. by CE.

The reprogramming of a word is initiated with start and followed by an erase procedure. $\overline{CE}$ = "1" stops erasure. The control bit SB = "1" (in the shift register), which is also necessary for the write process, remains stable even after the termination of erasure. Thus, for writing the selected word, only the data line D has to be changed from "1" to "0", the chip has to be enabled again by $\overline{CE}$ = "0" and the data change has to be started by the start pulse.

An erase and a write process can also be executed separately. In order to obtain a safe "1" in all 8 bits of the selected memory address by the erase process, a data word is, however, to be entered with 8 times "1" before erasure. During the writing of a word which has not been erased before, the "0" states of the previous and the actual information are added.

Test Mode - Total Erasure

The test mode is activated, if the input TP (pin 7) is set from 0 V to 5 V = V_{DD}. To erase the entire memory, the test mode is to be turned on and the address 0 (A0 to A6) together with the control bit SB = 1 is to be entered. The subsequent programm sequence is identical to the erasure of address 0. As soon as the erase procedure has terminated due to $\overline{CE}$ changing from 0 to 1, the test mode is to be turned off.

RESET

A memory which has not been selected is automatically in reset state by state $\overline{CE}$ = "1". All flipflops of the sequence control are reset. However, the information in the shift register is maintained and will only be changed by shifting the data. The reset state is also set in the case of the turning-on of the memory (power-on) by an on-chip circuit.

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Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D	–	40	mW
Storage temperature	T_{stg}	– 55	125	°C
Junction temperature	T_j	–	125	°C
Thermal resistance system - air	$R_{th\ SA}$	–	100	K/W

Operating Range

Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	– 40	110	°C

Characteristics

T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5	5.25	V	–
Supply current	I_{CC}	–	–	3	mA	(V_{DD} = 5.25 V)
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L	–	–	0.8	V	–
Input voltage (D, Φ, $\overline{CE}$)	V_H	2.4	–	–	V	–
Input current (D, Φ, $\overline{CE}$)	I_H	–	–	10	µA	(V_H = 5.25 V)
Data Output D (open drain)						
L-output current	I_L	–	–	0.5	mA	(V_L = 0.8 V)
H-output current	I_H	–	–	10	µA	(V_H = 5.25 V)

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Clock Pulse Φ						
H-clock period	t_H	2.5	–	60	µs	–
L-clock period	t_L	5	–	–	µs	–
Edge spacing $\overline{CE}$ to D	Δt	2.5	–	–	µs	–
Edge spacing $\overline{CE}$ to Φ	t_{AKT}	5	–	–	µs	–
Data hold time (before/after Φ trailing edge	t_{HD}	2.5	–	–	µs	–
Data delay time (after Φ trailing edge)	t_{DD}	2.5	–	–	µs	–
Rise time	t_r	–	–	1	µs	–
Fall time	t_f	–	–	1	µs	–
Chip erase duration	t_{er}	5	–	20	ms	–
Write duration	t_{wr}	5	–	20	ms	–
Full erasure duration	$t_{tot\ er}$	20	–	25	ms	–

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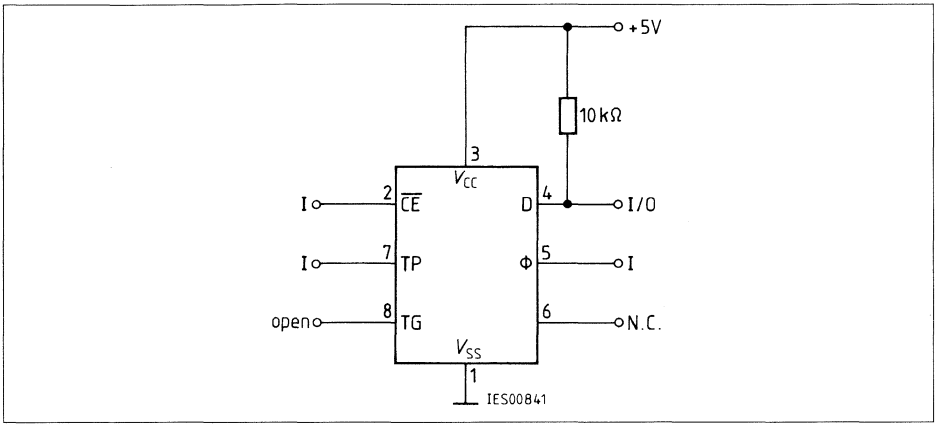
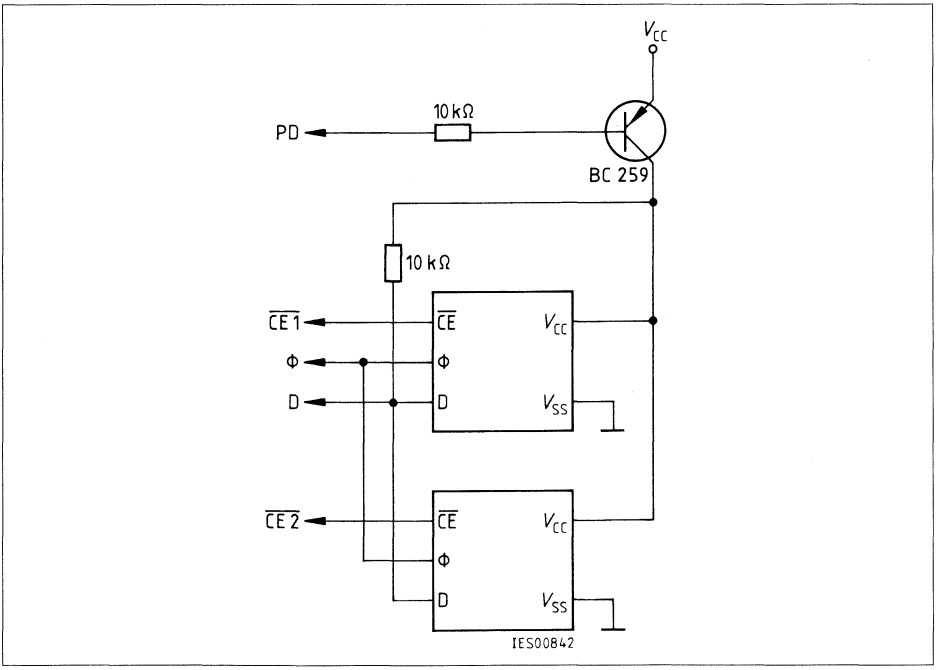


Test Circuit



Application Circuit

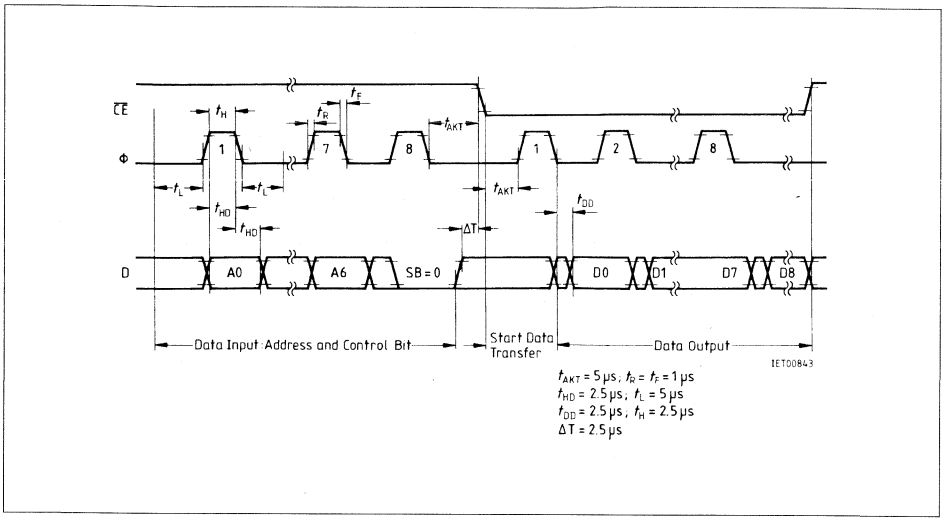


Diagram
Read

13

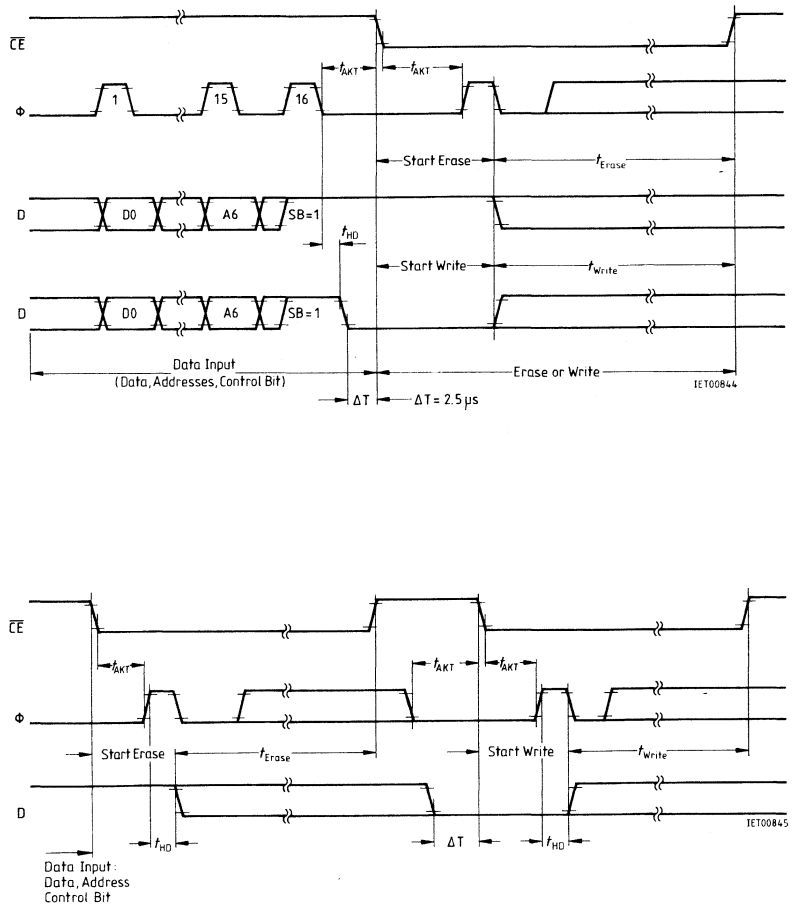


Diagram
Reprogramming

Nonvolatile Memory
2-Kbit E²PROM with I²C Bus Interface

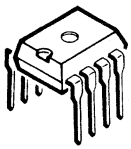
SDE 2526 A2

Preliminary Data

MOS IC

Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 256 × 8-bit organization
- + 5 V supply voltage
- Serial 2-line bus for data input and output (I²C bus)
- Reprogramming mode, typ. 15 ms erase/write cycle
- Reprogramming by means of on-chip control (without external control)
- Data retention longer than 10 years
- More than 10^5 reprogramming cycles per address
- Extended temperature range from – 40 to 110 °C



VPD 05025

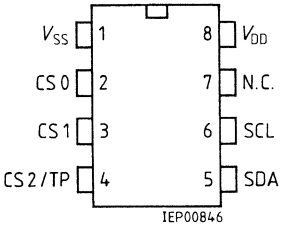
P-DIP-8

VPS05121

P-DSO-8-1

Type	Ordering Code	Package
SDE 2526 A2	Q67100-H9020	P-DIP-8
▼ SDE 2526 A2G	Q67100-H9036	P-DSO-8-1 (SMD)

13



Pin Configuration
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SS}	Ground
2	CS0	Chip select input
3	CS1	Chip select input
4	CS2/TP	Test operation control
5	SDA	Data line } I^2C bus
6	SCL	Clock line } I^2C bus
7	N.C.	Not connected
8	V_{DD}	Supply voltage

Control Word Input Key

CS/E CS/A	Chip select for data input to memory Chip select for data output from memory
WA	Memory word address
DE DA	Data word for memory Data word read out from memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS0, CS1, CS2	Chip select bits
A0 to A7	Memory word address bits

I^2C Bus Interface (Figure 1 and 2)

The I^2C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I^2C bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I^2C bus system, the device can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the 8^{th} transmission pulse and a 9^{th} acknowledge clock pulse, the device sets the SDA line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I^2C bus is summarized in **figure 2** (high-speed mode).

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Control Functions of the I^2C Bus

The device is controlled by the controller (master) via the I^2C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the

data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memories connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three select inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock no. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-impedance and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 255, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 30 ms, or typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-ON Mode and Chip Reset

After the supply voltage V_{DD} has been connected, the data output will be in the high-impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and the stop condition, the internal control logic is reset. In case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Test Mode - Chip Erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". Input CS2/TP, however, is connected from 0 V to + 12 V immediately before the stop condition is generated. The subsequent stop condition initiates the chip erase procedure. The control word has to be entered under the device address 0 (CS0 = L, CS1 = L, CS2 = L). After the full erase has been terminated, input CS2/TP must again be connected to 0 V.

Absolute Maximum Ratings[1)]

Parameter		Symbol	Limit Values	Unit
Supply voltage		V_{DD}	– 0.3 to 6	V
Input voltage		V_I	– 0.3 to 6	V
Storage temperature range		T_{stg}	– 55 to 125	°C
Thermal resistance	P-DIP-8	$R_{th\ JA}$	100	K/W
Junction - air	P-DSO-8-1		170	K/W

Operating Range

Supply voltage	V_{DD}	4.75 to 5.25	V
Ambient temperature	T_A	– 40 to 110	°C

1) does not apply to the input CS2/TP in "test mode - full erasure" operation

DC Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.75	–	5.25	V
Supply current	I_{DD}	–	–	20	mA
Inputs SCL/SDA					
Low level	V_{IL}	–	–	1.5	V
High level	V_{IH}	3.0	–	V_{DD}	V
High current; $V_{IH} = V_{DD\ max}$	I_H	–	–	10	µA
Output SDA					
L-current; V_{QL} = 0.4 V	I_{QL}	–	–	3.0	mA
Leakage current; $V_{QL} = V_{DD\ max}$	I_{QH}	–	–	10	µA
Inputs CSO, CS1, CS2/TP					
L-level	V_{IL}	–	–	0.2	V
H-level	V_{IH}	4.5	–	V_{DD}	V
H-current	I_{IH}	–	–	100	µA
Clock frequency	f_{SCL}	–	–	100	kHz
Reprogramming duration (erase and write)	t_{prog}	–	10	20	ms
Input capacitance	C_I	–	–	10	pF
Full erase duration (test mode full erase)	t_{er}	–	–	20	ms

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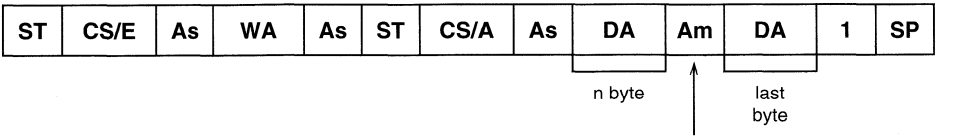
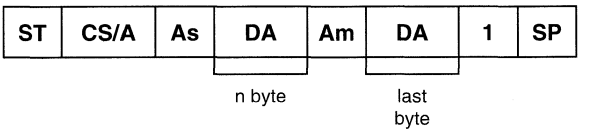
Control Word Input Read

a) complete (with word address input)

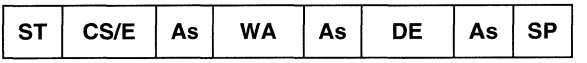


Automatic incrementation of the word address

b) shortened (read out starts with last used word address)



Control Word Input Programming



(Reprogramming starts after this stop condition)

Control Word Table

Clock N	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	through memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	through master

Diagrams

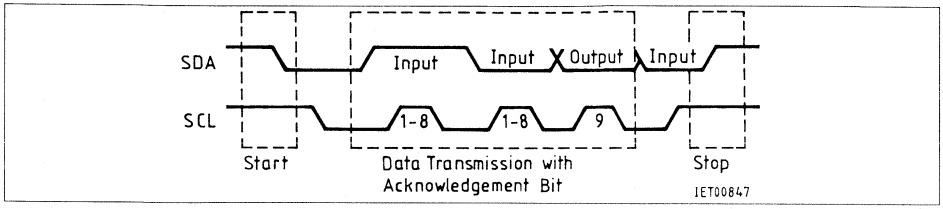


Figure 1
Operational States of the I²C Bus

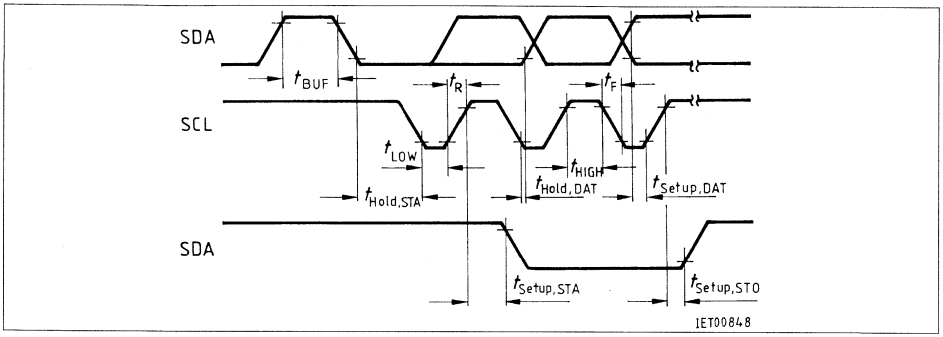


Figure 2
Timing Conditions for the I²C Bus (high-speed mode)

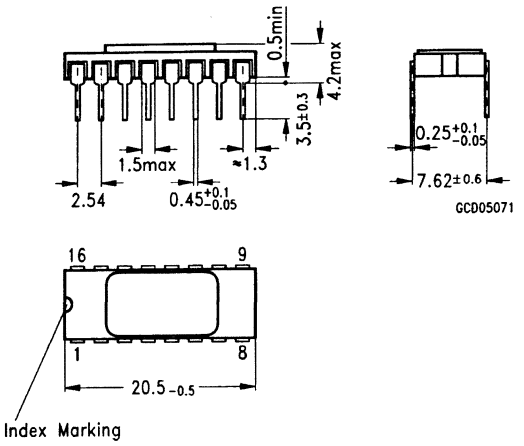
Parameter	Symbol	Limit Values
The minimum time the bus must be free before a new transmission can start	t_{BUF}	$t > t_{LOWmin}$
Start condition hold time	$t_{Hold;\,STA}$	$t > t_{HIGHmin}$
L-clock period	t_{LOWmin}	4, 7 µs
H-clock period	$t_{HIGHmin}$	4 µs
Start condition setup time, only valid for repeated start code	$t_{Setup;\,STA}$	$t > t_{LOWmin}$
Data hold time[1)]	$t_{Hold;\,DAT}$	$t > 0$ µs
Data setup time	$t_{Setup;\,DAT}$	$t > 250$ ns
Rise time of both the SDA and SCL line	t_r	$t < 1$ µs
Fall time of both the SDA and SCL line	t_f	$t < 300$ ns
Stop condition setup time	$t_{Setup;\,STO}$	$t > t_{LOWmin}$

Note
All values refer to V_{IH} and V_{IL} level

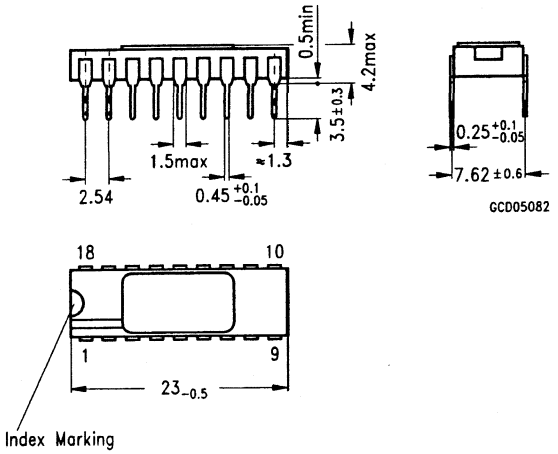
1) Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

13

Ceramic Package, C-DIP-16
(Ceramic Dual In-Line Package)

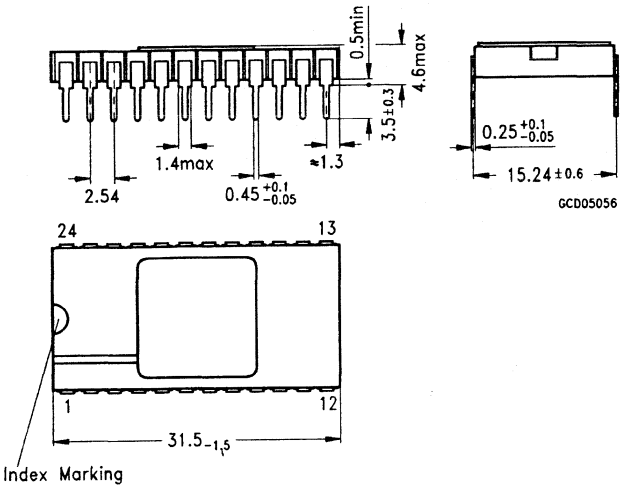


Ceramic Package, C-DIP-18
(Ceramic Dual In-Line Package)

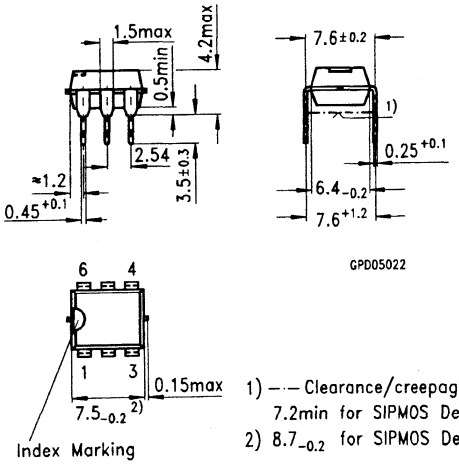


Dimensions in mm

Ceramic Package, C-DIP-24
(Ceramic Dual In-Line Package)



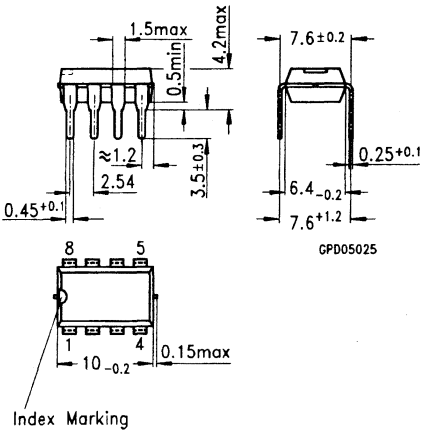
Plastic Package, P-DIP-6-1
(Plastic Dual In-Line Package)



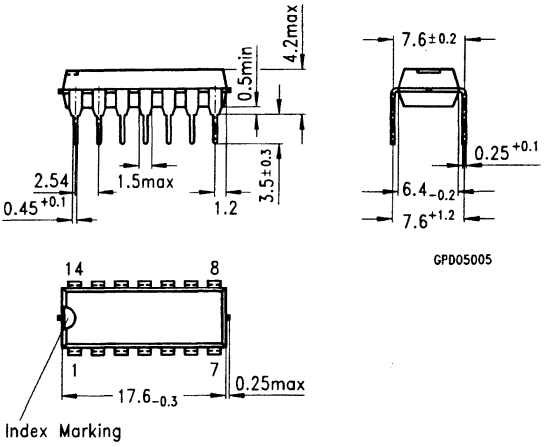
14

Dimensions in mm

Plastic Package, P-DIP-8
(Plastic Dual In-Line Package)

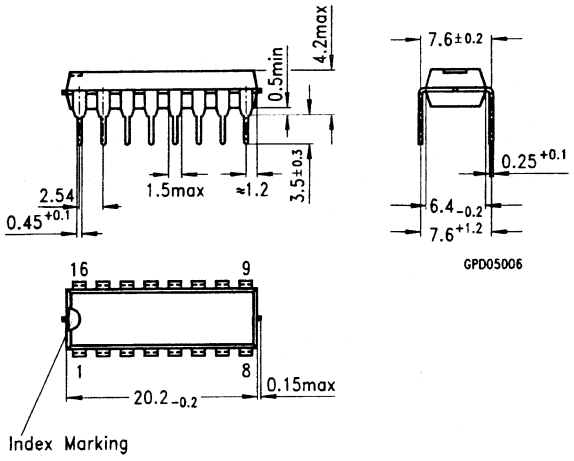


Plastic Package, P-DIP-14-1
(Plastic Dual In-Line Package)

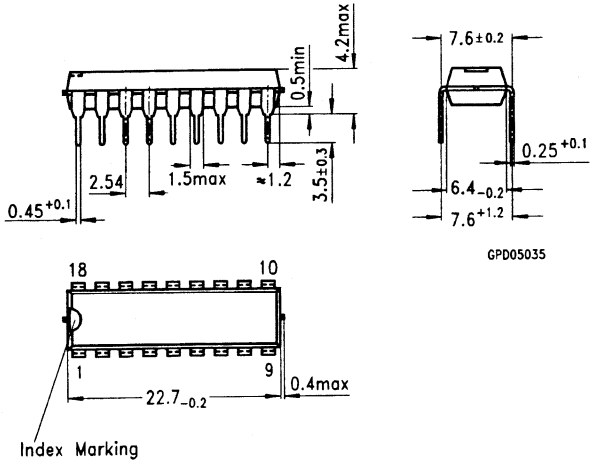


Dimensions in mm

Plastic Package, P-DIP-16
(Plastic Dual In-Line Package)



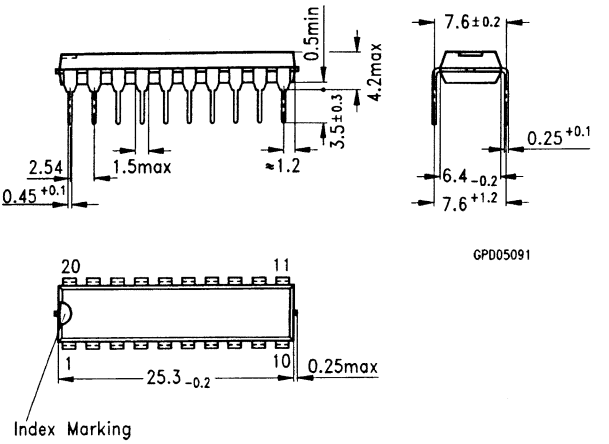
Plastic Package, P-DIP-18-1
(Plastic Dual In-Line Package)



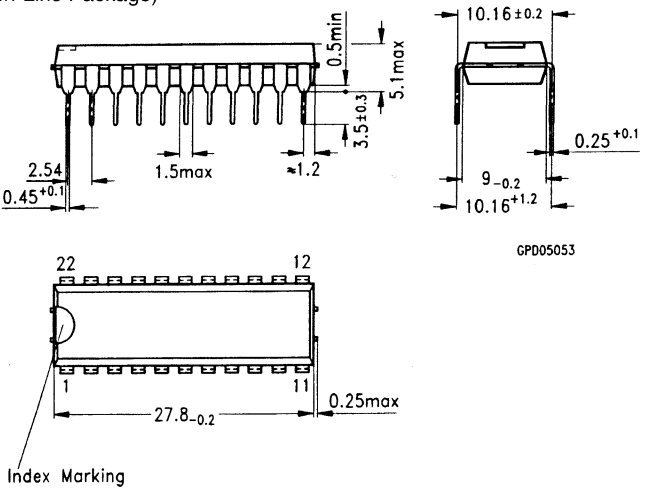
14

Dimensions in mm

Plastic Package, P-DIP-20-1
(Plastic Dual In-Line Package)

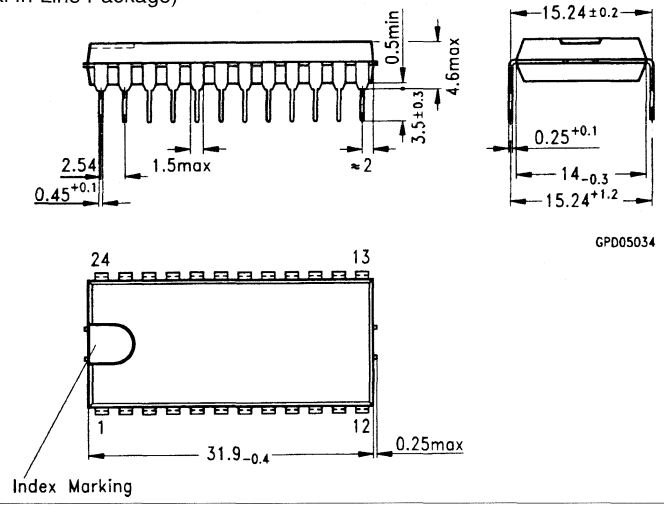


Plastic Package, P-DIP-22
(Plastic Dual In-Line Package)

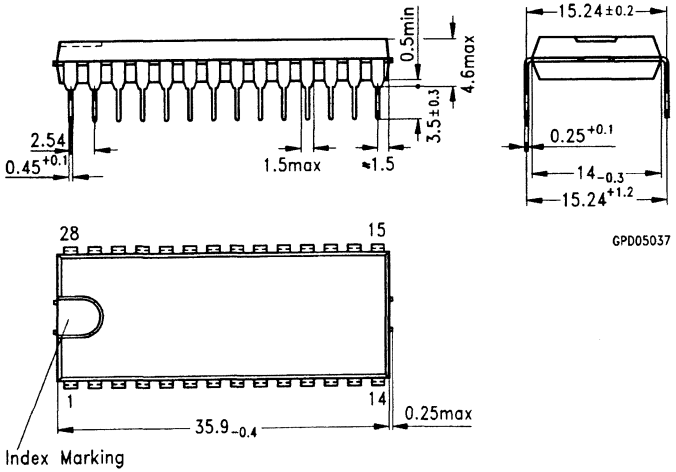


Dimensions in mm

Plastic Package, P-DIP-24
(Plastic Dual In-Line Package)

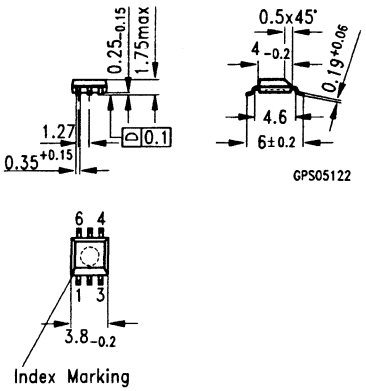


Plastic Package, P-DIP-28
(Plastic Dual In-Line Package)

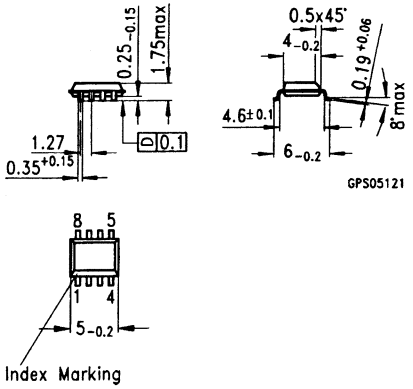


Dimensions in mm

Plastic Package, P-DSO-6 (SMD)
(Plastic Dual Small Outline)



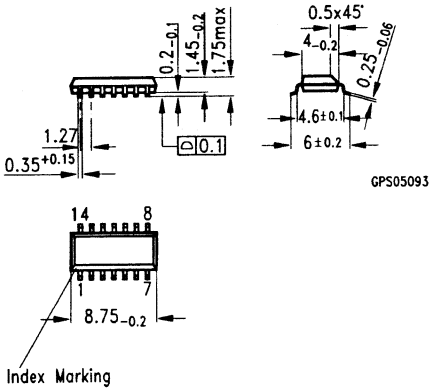
Plastic Package, P-DSO-8-1(SMD)
(Plastic Dual Small Outline)



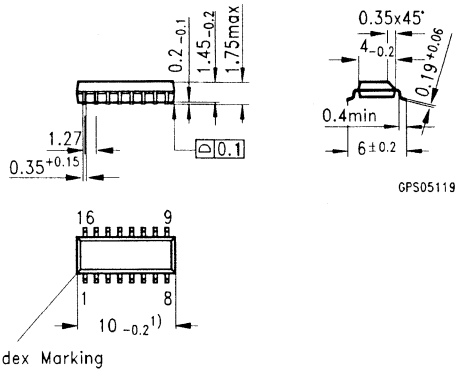
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-DSO-14-1 (SMD)
(Plastic Dual Small Outline)



Plastic Package, P-DSO-16-1 (SMD)
(Plastic Dual Small Outline)



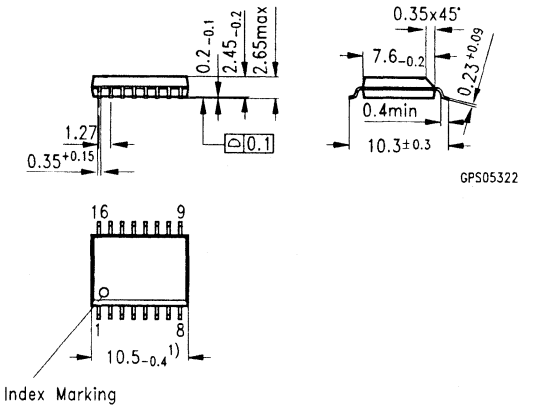
1) Does not include plastic or metal protrusions of 0.15max

SMD = Surface Mounted Device

Dimensions in mm

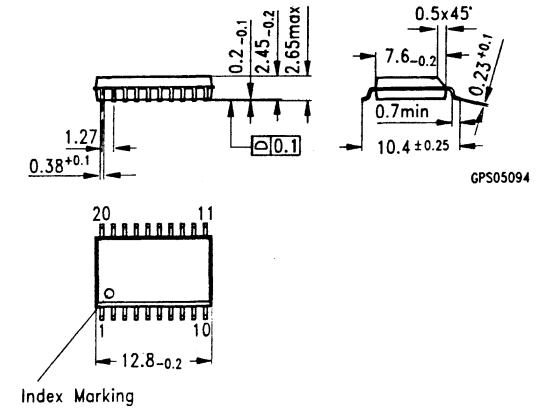
14

Plastic Package, P-DSO-16-3 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15max

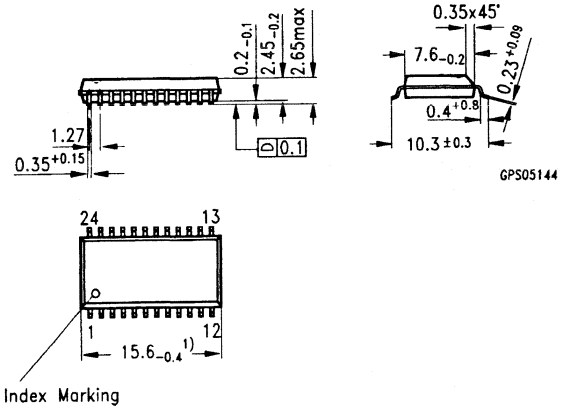
Plastic Package, P-DSO-20-1 (SMD)
(Plastic Dual Small Outline)



SMD = Surface Mounted Device

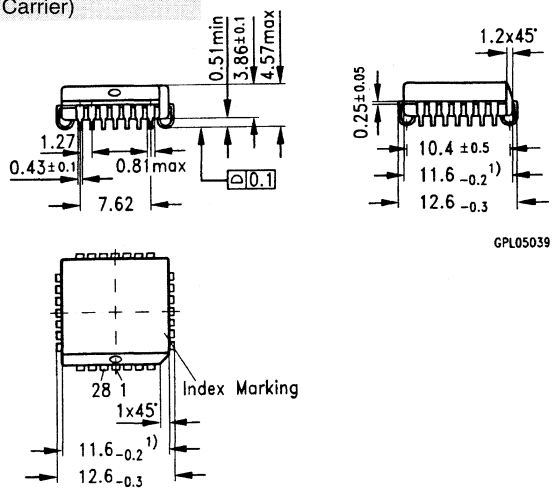
Dimensions in mm

Plastic Package, P-DSO-24-1 (SMD)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15max

Plastic Package, P-LCC-28-2 (SMD)
(Plastic Leaded Chip Carrier)



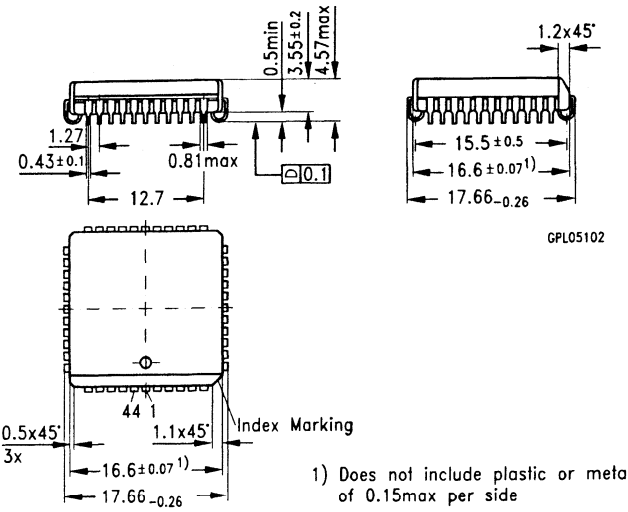
1) Does not include plastic or metal protrusions of 0.2max per side

SMD = Surface Mounted Device

Dimensions in mm

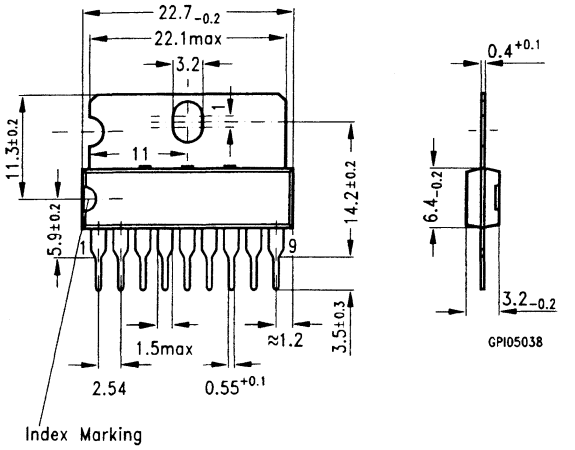
14

Plastic Package, P-LCC-44 (SMD)
(Plastic Leaded Chip Carrier)



1) Does not include plastic or metal protrusions of 0.15max per side

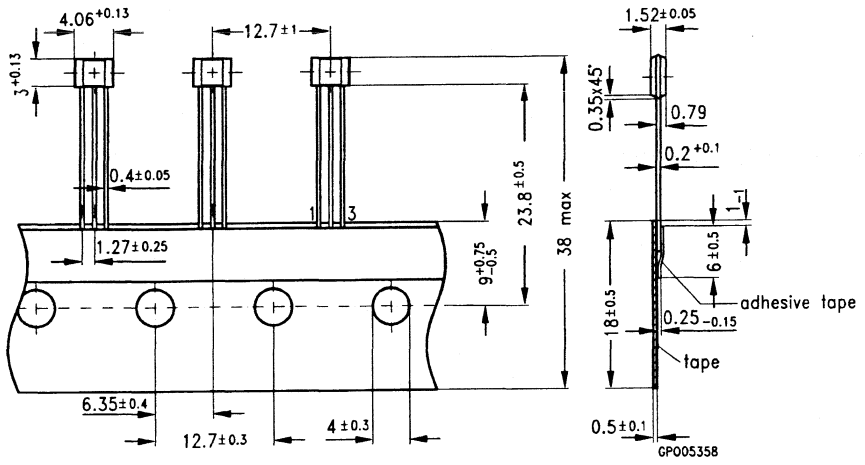
Plastic Package, P-SIP-9
(Plastic Single In-Line Package)



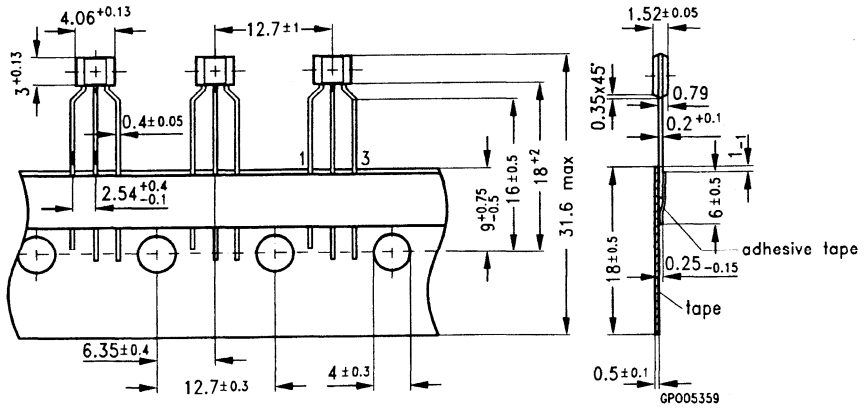
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-SSO-3-2
(Plastic Single Small Outline)



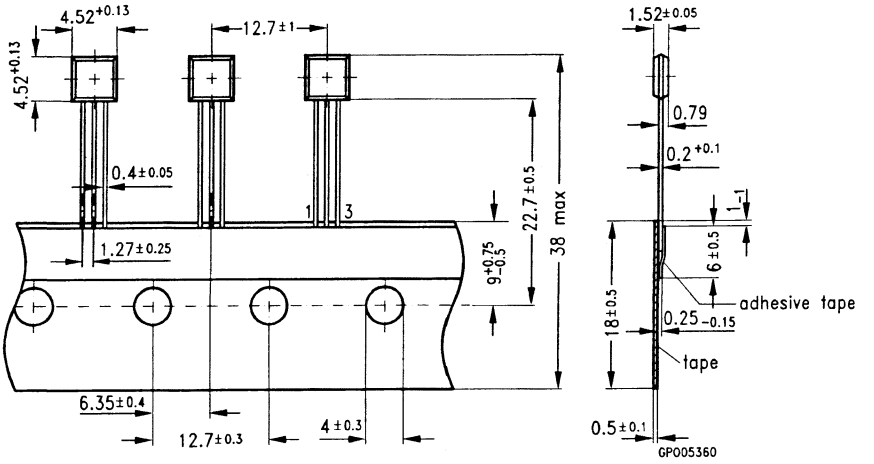
Plastic Package, P-SSO-3-3
(Plastic Single Small Outline)



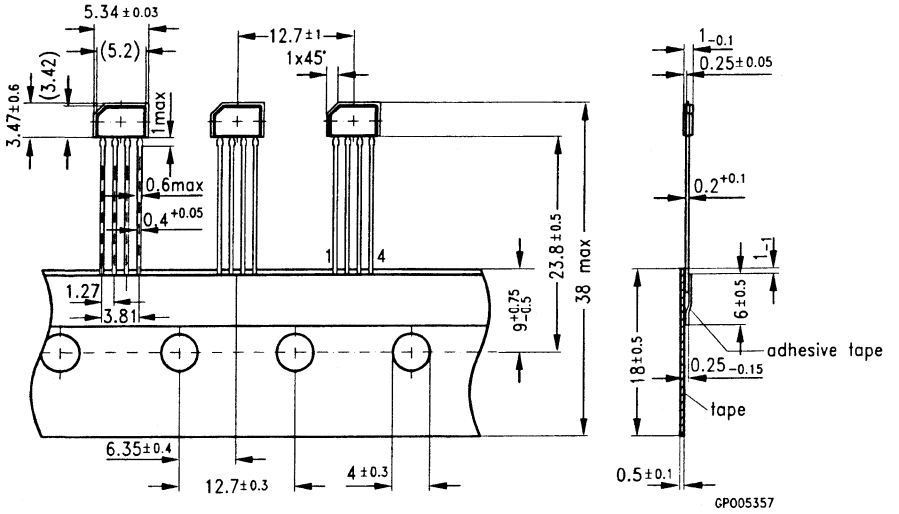
14

Dimensions in mm

Plastic Package, P-SSO-3-4
(Plastic Single Small Outline)

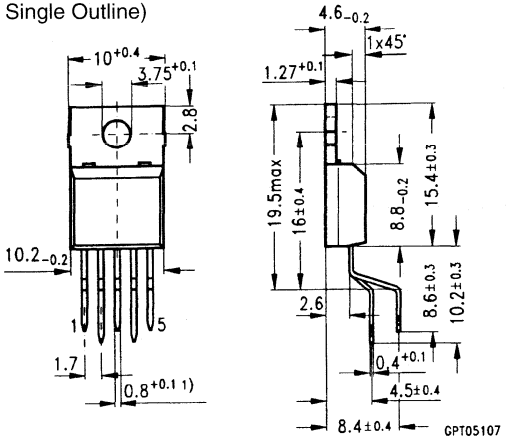


Plastic Package, P-SSO-4
(Plastic Single Small Outline)



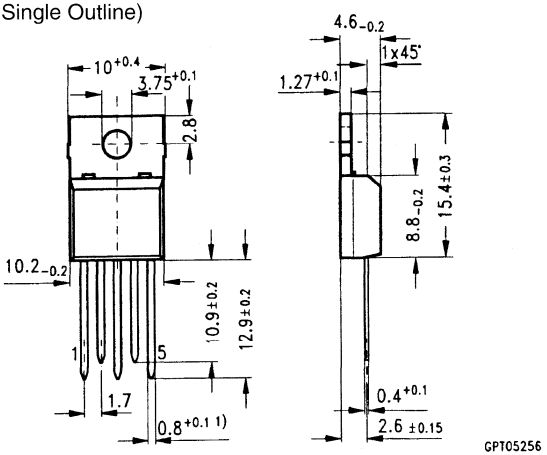
Dimensions in mm

Plastic Package, P-TO220-5-1
(Plastic Transistor Single Outline)



1) $1_{-0.15}$ at dam bar (max 1.8 from body)
1) $1_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

Plastic Package, P-TO220-5-2
(Plastic Transistor Single Outline)

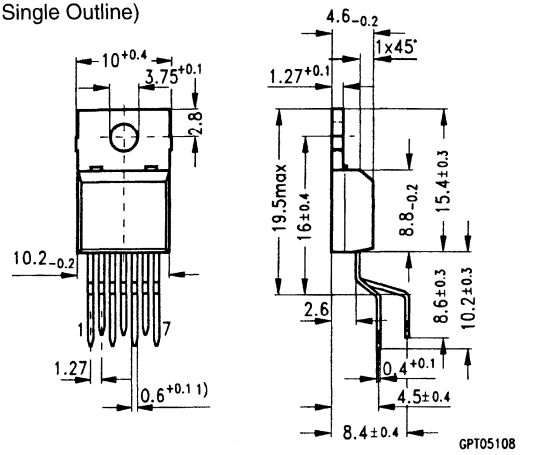


1) $1_{-0.15}$ at dam bar (max 1.8 from body)
1) $1_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

14

Dimensions in mm

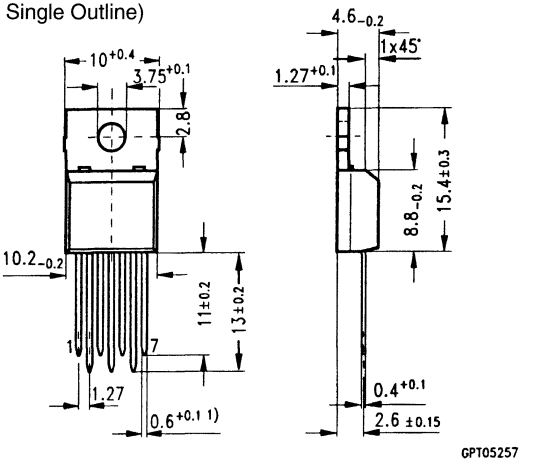
Plastic Package, P-TO220-7-1
(Plastic Transistor Single Outline)



1) $0.75_{-0.15}$ at dam bar (max 1.8 from body)

1) $0.75_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

Plastic Package, P-TO220-7-2
(Plastic Transistor Single Outline)

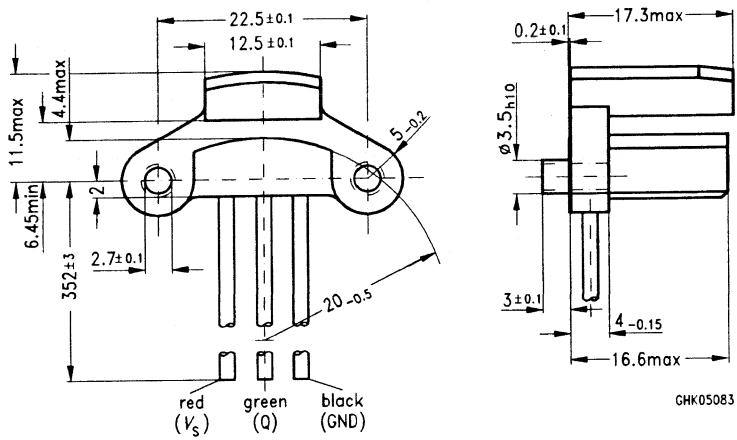


1) $0.75_{-0.15}$ at dam bar (max 1.8 from body)

1) $0.75_{-0.15}$ im Dichtstegbereich (max 1.8 vom Körper)

Dimensions in mm

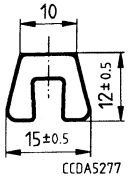
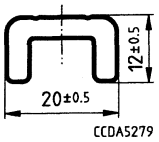
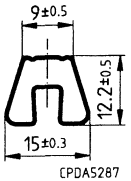
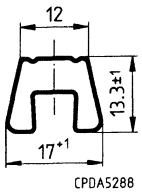
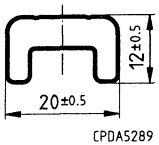
Special Package

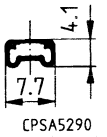
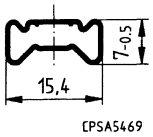
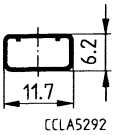
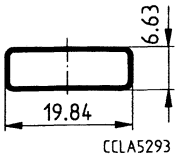
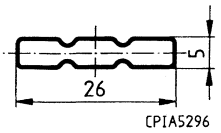


Dimensions in mm

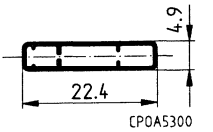
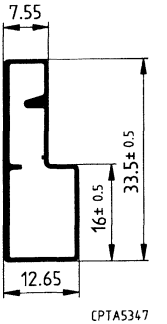
14

Tubes
Length: 528 mm $_{-2}$ conductive

Packages	Piece/Tube [1]	Dimensions
C-DIP-16 C-DIP-18	20 20	 2)
C-DIP-24	15	
P-DIP-6 P-DIP-8 P-DIP-14 P-DIP-16 P-DIP-18 P-DIP-20	50 50 25 25 20 20	
P-DIP-22	15	
P-DIP-24 P-DIP-28	15 14	

Packages	Piece/Tube [1]	Dimensions
P-DSO-6 P-DSO-8 P-DSO-14	100 100 50	
P-DSO-20 P-DSO-24	40 30	
P-LCC-28-2	40	
P-LCC-44	25	
P-SIP-9	20	[2] 

14

Packages	Piece/Tube [1]	Dimensions
P-SSO-3	100	2) 
P-TO220-5 P-TO220-7	50 50	2) 

1) Subject to change
2) Antistatic tube

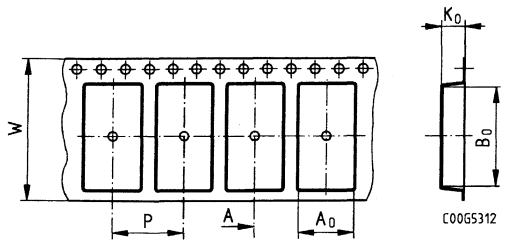
Tape and Reel (DIN IEC 286)

Package	Pieces/Reel	∅ Reel	Tape Width W *)
P-DSO Plastic Dual Small Outline			
P-DSO-6	2500	330	12
P-DSO-8-1			12
P-DSO-14-1			16
P-DSO-16-3	1000		16
P-DSO-20-1			24
P-DSO-24-1			24
P-LCC Plastic Leaded Chip Carrier			
P-LCC-28-2	750	330	24
P-LCC-44	500	360	32
P-TO220 Plastic Transistor Single Outline			
P-TO220-5-2	1000	330	24
P-TO220-7-2			24

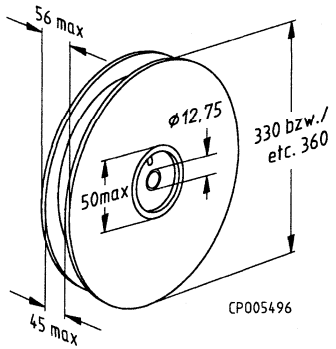
*) For further dimensions, tolerances or variations, please contact your nearest Siemens representative.

Tape and Reel

Tape



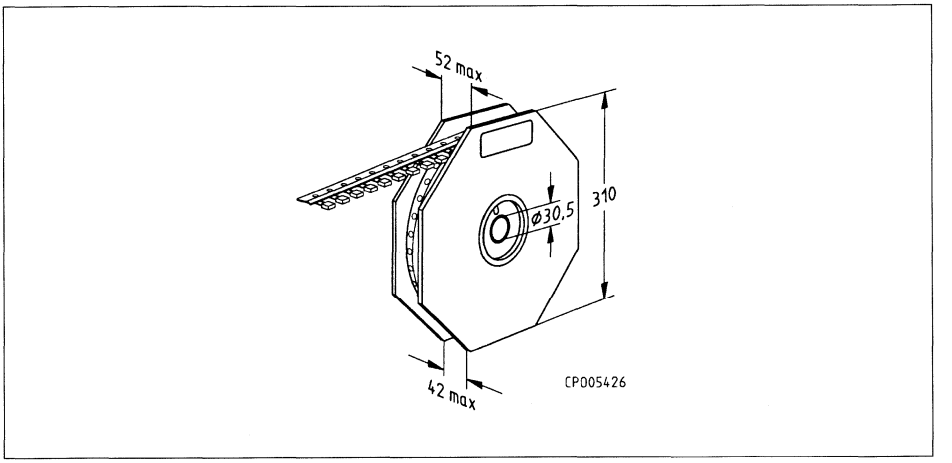
Reel



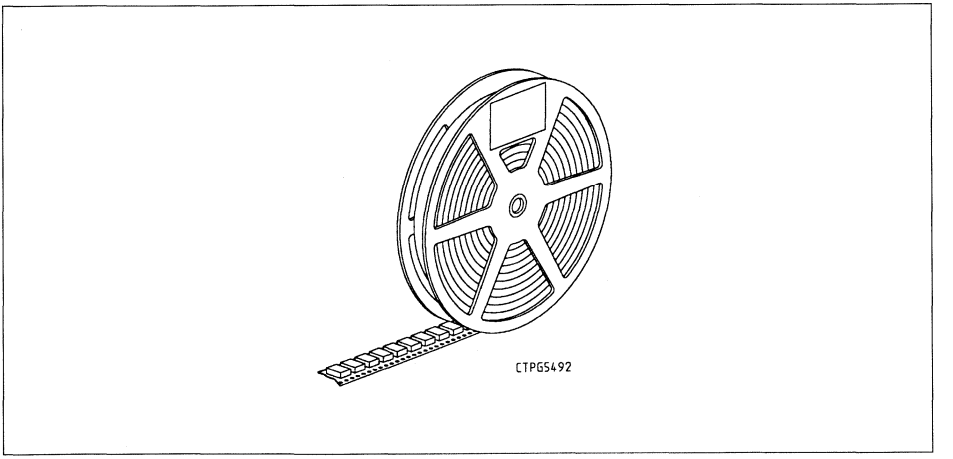
Radial Tape

Package	Pieces/Reel	∅ Reel
P-SSO Plastic Single Small Outline		
P-SSO-3	4000	330
P-SSO-4		

Radial Tape



Reel Packing



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